LMG1020 5-V, 7-A, 5-A Low-Side GaN and MOSFET Driver For 1-ns Pulse Width Applications

1 Features

- Low-Side, Ultra-Fast Gate Driver for GaN and Silicon FETs
- 1 ns Minimum Input Pulse Width
- Up to 60 MHz Operation
- 2.5 ns Typical, 4.5 ns Maximum Propagation Delay
- 400 ps Typical Rise and Fall Time
- 7-A Peak Source and 5-A Peak Sink Currents
- 5-V Supply Voltage
- UVLO and Overtemperature Protection
- 0.8 mm × 1.2 mm WCSP Package

2 Applications

- LiDAR
- Time-of-Flight Laser Drivers
- Facial Recognition
- Class-E Wireless Chargers
- VHF Resonant Power Converters
- GaN-Based Synchronous Rectifier
- Augmented Reality

3 Description

The LMG1020 device is a single, low-side driver designed for driving GaN FETs and logic-level MOSFETs in high-speed applications including LiDAR, time-of-flight, facial recognition, and any power converters involving low side drivers. The design simplicity of the LMG1020 enables extremely fast propagation delays of 2.5 nanoseconds and minimum pulse width of 1 nanosecond. The drive strength is independently adjustable for the pull-up and pull-down edges by connecting external resistors between the gate and OUTH and OUTL, respectively.

The driver features undervoltage lockout (UVLO) and overtemperature protection (OTP) in the event of overload or fault conditions.

0.8-mm × 1.2-mm WCSP package of LMG1020 minimizes gate loop inductance and maximizes power density in high-frequency applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMG1020	WCSP (6)	0.80 mm × 1.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified LiDAR Driver Stage Diagram

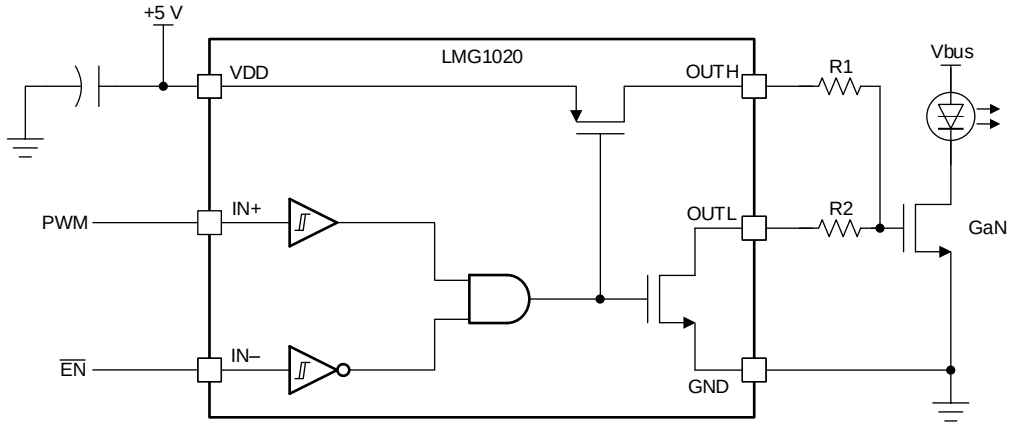


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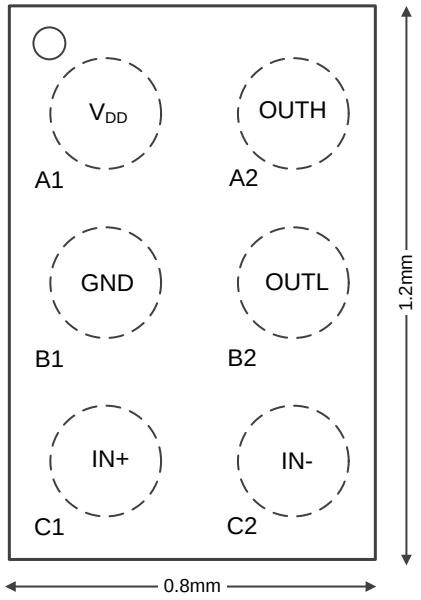
4 Revision History

Changes from Original (June 2018) to Revision B **Page**

- Changed Figure 1 input structure NAND gate to AND gate ... 1

5 Pin Configuration and Functions

YFF Package
6-Ball WCSP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	B1	—	Ground
IN+	C1	I	Positive logic-level input
IN–	C2	I	Negative logic-level input
OUTL	B2	O	Pulldown gate drive output. Connect through an optional resistor to the target transistor's gate
OUTH	A2	O	Pullup gate drive output. Connect through a resistor to the target transistor's gate
VDD	A1	I	Input voltage supply. Decouple through a small size, low inductance capacitor to GND

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage		5.75	V
V_{IN}	IN+, IN- pin voltage	-0.3	V_{DD} + 0.3	V
V_{OUT}	OUTH, OUTL pin voltage	-0.3	5.75	V
T_{STG}	Storage Temperature	-55	150	°C
T_J	Operating Temperature	-40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.75	5	5.4	V
V_{INx}	IN+ or IN- input voltage	0		V_{DD}	V
T_J	Operating Temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		SN1020 YFF (WCSP) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	133.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	38.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
Y_{JB}	Junction-to-board characterization parameter	38.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range (VDD=5V unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Characteristics						
$I_{VDD, Q}$	VDD Quiescent Current	IN_+ = IN_- = 0 V			75	µA
$I_{VDD, op}$	VDD Operating Current(1)	fsw = 30 MHz, 2 Ω, 0.1 pF load		40		mA
		fsw = 30 MHz, 2 Ω, 100 pF load		51		mA
$V_{DD, UVLO}$	Under-voltage Lockout	V_{DD} rising	4.06	4.19	4.33	V
$\Delta V_{DD, UVLO}$	UVLO Hysteresis			85		mV
T_{OTP}	Over temperature shutdown, rising edge threshold			170		°C
ΔT_{OTP}	Over temperature hysteresis			18		°C
Input DC Characteristics						
V_{IH}	IN+, IN- high threshold		1.7		2.6	V
V_{IL}	IN+, IN- low threshold		1.1		1.8	V
V_{HYST}	IN+, IN- hysteresis		0.5		1	V
R_{IN+}	Positive input pull-down resistance	To GND	100	150	250	kΩ
R_{IN-}	Negative input pull-up resistance	to V_{DD}	100	150	250	kΩ
C_{IN}	Input pin capacitance(1)	To GND		1.3		pF
Output DC Characteristics						
V_{OL}	OUTL voltage	I_{OUTL} = 100 mA, IN+= IN- = 0 V			36	mV
V_{DD}-V_{OH}	OUTH voltage	I_{OUTH} = 100 mA, IN+= 5 V, IN- = 0 V			50	mV
I_{OH}	Peak source current(1)	V_{OUTH} = 0 V, IN+= 5 V, IN- = 0 V		7		A
I_{OL}	Peak sink current(1)	V_{OUTL} = 5 V, IN+= IN- = 0 V		5		A

(1) Insured by design

6.6 Switching Characteristics

over operating free-air temperature range (VDD=5V unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{start}	Startup Time, V_{DD} rising above UVLO	IN- = GND, IN+ = V_{DD} , V_{DD} rising to 4.2V to OUTH rising		40	70	µs
$t_{shut-off}$	ULVO falling	IN- = GND, IN+ = VDD , VDD falling below 4.1V to OUTH falling	1	1.9	3.1	µs
$t_{pd, r}$	Propagation delay, turn on	IN- = 0 V, IN+ to OUTH, 100 pF load	1.5	2.5	4.1	ns
$t_{pd, f}$	Propagation delay, turn off	IN- = 0 V, IN+ to OUTL, 100 pF load	1.8	2.6	4.3	ns
Δt_{pd}	Pulse positive distrortion ($t_{pd, f}$ - $t_{pd, r}$)			230	603	ps
t_{rise}	Output rise time	0Ω series 100 pF load(1)		375		ps
t_{fall}	Output fall time	0Ω series 100 pF load(1)		350		ps
t_{min}	Minimum input pulse width	0Ω series 100 pF load(1)		1		ns

(1) rise and fall calulated as a 20% to 80%

6.7 Typical Characteristics

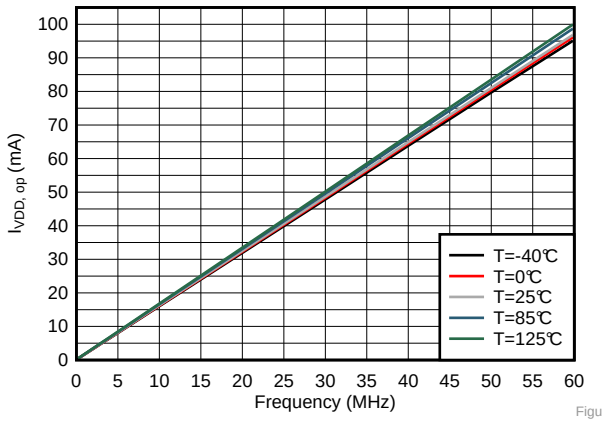


Figure 1. $I_{VDD, op}$ vs Frequency With 2 Ω Series 100 pF Load

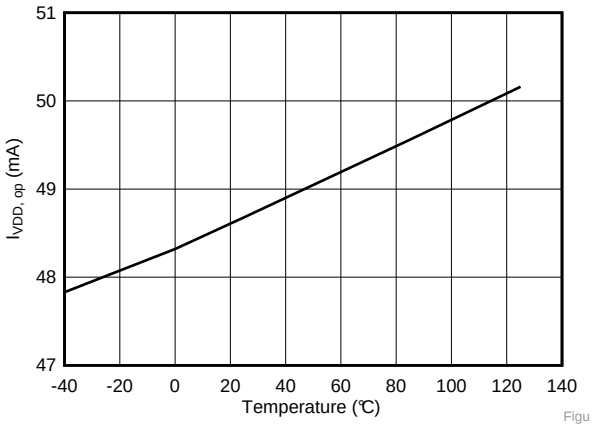


Figure 2. $I_{VDD, op}$ vs Temperature At 30MHz With 2 Ω series 100 pF Load

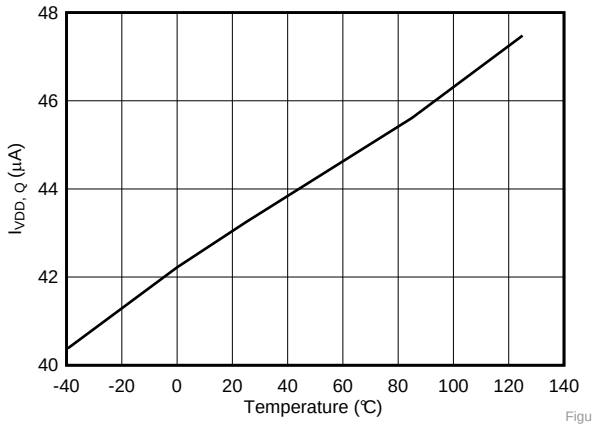


Figure 3. Quiescent Current vs Temperature

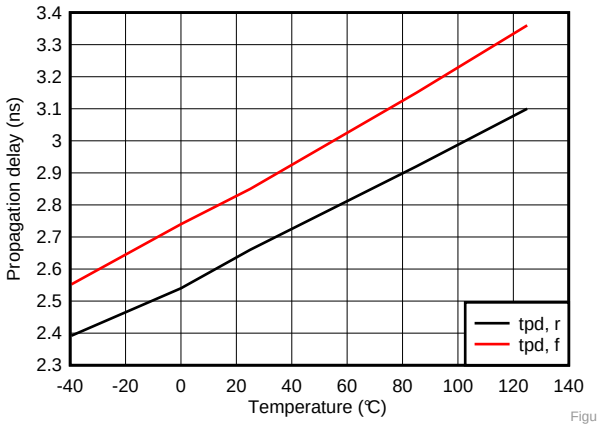


Figure 4. Propagation Delay vs Temperature

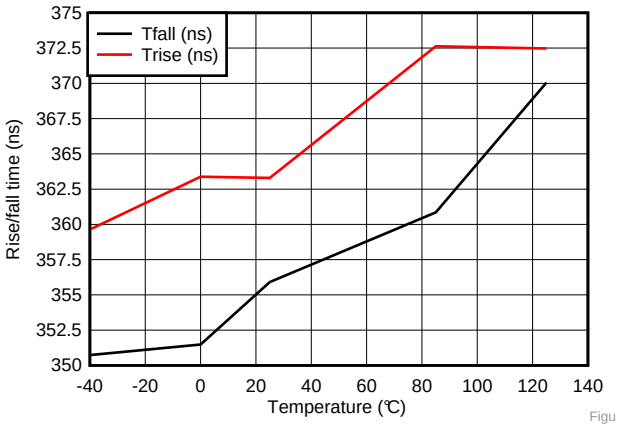


Figure 5. Rise And Fall Time vs Temperature With 0 Ω Series 100 pF Load

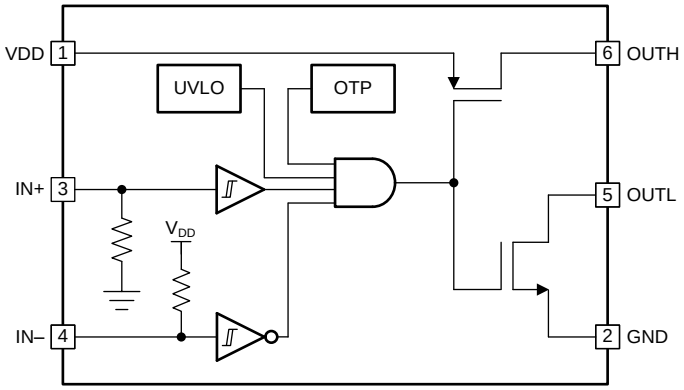
7 Detailed Description

7.1 Overview

LMG1020 is a high-performance low-side 5-V gate driver for GaN and logic-level silicon power transistors. While the LMG1020 is designed for high-speed applications, such as wireless power transmission and LiDAR applications, it is a high-performance solution for any other low-side driving applications.

The LMG1020 is optimized to provide the lowest propagation delay through the driver to the power transistor. LMG1020 is in a small 0.8×1.2mm WCSP ball-grid array package in order to minimize its parasitic inductance. This low inductance design helps achieve high current, low ringing performance in very high frequency operation when driving power FETs.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Stage

The input stage features two Schmitt-triggers at the pins IN+ and IN– to reduce sensitivity to noise on the inputs. IN+ signal and the inverted IN– signal are both sent to an AND gate. IN+ is connected with a pull-down resistor while IN– is connected with a pull-up resistor to prevent unintended turnon. The output signal will follow the difference between IN+ and IN–. Both IN+ and IN– are single ended inputs, and these two pins cannot be used as a differential input pair.

7.3.2 Output Stage

LMG1020 provides 7-A source, 5-A sink (asymmetrical drive) peak-drive current capability, and features a split output configuration. The OUTH and OUTL outputs of the LMG1020 allow the user to use independent resistors connecting to the gate. The two resistors allow the user to independently adjust the turnon and turnoff drive strengths to control slew rate and EMI, and to control ringing on the gate signal. For GaN FETs, controlling ringing is important to reduce stress on the GaN FET and driver. The output stage OUTL is also pulled down in undervoltage condition, which prevents the unintended charge accumulation of device C_{iss}.

7.3.3 V_{DD} and undervoltage lockout

LMG1020 features nominal 5V and maximum 5.25V of supply voltage, and its absolute maximum supply voltage is 5.75 V. In the design, it is recommended to limit the variability of the power supply to be within 5% (0.25V), and the overshoot voltage during switching transient not to exceed the absolute maximum voltage. Refer to Section VDD and Overshoot for more the detailed design guide.

LMG1020 also features internal undervoltage lockout (UVLO) to protect the driver and circuit in case of fault conditions. The UVLO point is setup between 4.1V and 4.2V with a hysteresis of 85mV. This UVLO level is specifically designed to guarantee that GaN power devices can be switched at a low $R_{DS(ON)}$ region. During UVLO condition, the OUTL is pulled down to ground.

Feature Description (continued)

7.3.4 Overtemperature Protection (OTP)

LMG1020 features overtemperature protection (OTP) function by having a rising edge trigger point at around 170°C. With a hysteresis of 20°C, the device can restart to operate when junction temperature is below 150°C.

7.4 Device Functional Modes

Table 1. Truth Table

IN–	IN+	OUTH	OUTL
L	L	OPEN	L
L	H	H	OPEN
H	L	OPEN	L
H	H	OPEN	L

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

To operate GaN transistors at very high switching frequencies and to reduce associated switching losses, a powerful gate driver is employed between the PWM output of controller and the gates of the GaN transistor. Also, gate drivers are indispensable when the outputs of the PWM controller do not meet the voltage or current levels needed to directly drive the gates of the switching devices. With the advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3 V logic signal, which cannot effectively turn on a power switch. A level-shift circuit is needed to boost the 3.3 V signal to the gate-drive voltage (such as 5 V) in order to fully turn on the power device and minimize conduction losses.

Gate drivers effectively provide the buffer-drive functions. Gate drivers also address other needs such as minimizing the effect of high-frequency switching noise (by placing the high-current driver IC physically close to the power switch), reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

The LMG1020 is a 60-MHz low-side gate driver for enhancement mode GaN FETs and Si FETs in a single-ended configuration. The split-gate outputs with strong source and sink capability provides flexibility to adjust the turnon and turnoff strength independently. As a low side driver, LMG1020 can be used in a variety of applications, including different power converters, LiDAR, time-of-flight laser drivers, class-E wireless chargers, synchronous rectifiers, and augmented reality. LMG1020 can also be used as a high frequency low current laser diode driver, or as a signal buffer with very fast rise/fall time.

8.2 Typical Application

The LMG1020 is designed to be used with a single low-side, ground-referenced GaN or logic-level Si FET, as shown in Figure 6. Independent gate drive resistors, R1 and R2, are used to independently control the turnon and turnoff drive strengths, respectively. For fast and strong turnoff, R2 can be shorted and OUTL directly connected to the transistor's gate. For symmetric drive strengths, it is acceptable to short OUTH and OUTL and use a single gate-drive resistor.

TI recommends using at least a 2 Ω resistor at each OUTH and OUTL to avoid voltage overstress due to inductive ringing. Ringing overshoot must not exceed the maximum absolute supply voltage.

For applications requiring smaller resistance values, contact TI E2E for guidance.

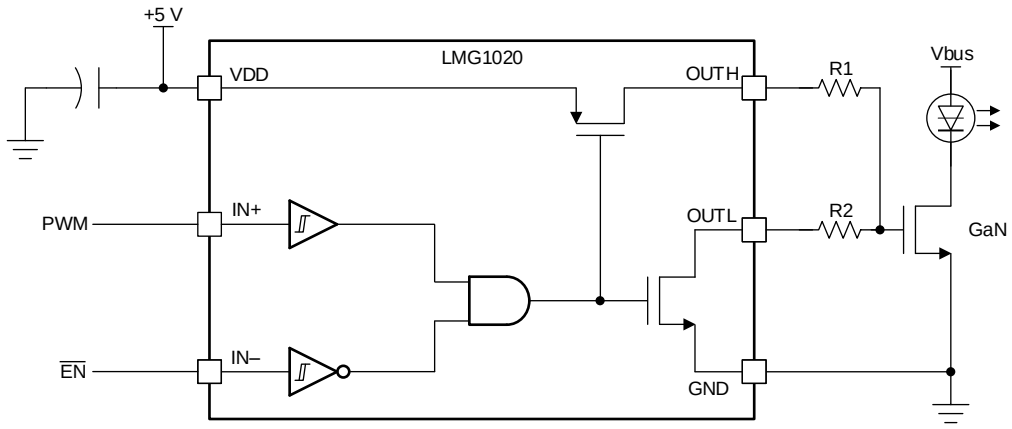


Figure 6. Typical Implementation of a Circuit

Typical Application (continued)

8.2.1 Design Requirements

When designing a multi-MHz (or nano-second pulse) application that incorporates the LMG1020 gate driver and GaN power FETs, some design considerations must be evaluated first to make the most appropriate selection. Among these considerations are layout optimization, circuit voltages, passive components, operating frequency, and controller selection.

8.2.2 Detailed Design Procedure

8.2.2.1 Handling Ground Bounce

For the best switching performance and gate loop with lowest parasitics, it is recommended to connect the ground return pin of LMG1020 as close as possible to the source of the low-side FET in a low inductance manner. However, doing so can cause the ground of LMG1020 to bounce relative to the system or controller ground and lead to erroneous switching logic on the input so as mis-turn on/off on the output.

First of all, LMG1020 has input hysteresis built into the input buffers to help counteract this effect. The maximum di/dt allowed to prevent the input voltage transient from exceeding the input hysteresis is given by Equation 1

$$\frac{di_S}{dt} = \frac{V_{HYST}}{L_{RS}} \quad (1)$$

where

- L_{RS} is the inductance between FET source and ground,
- V_{HYST} is the hysteresis of the input pin,
- and $di_s/\Delta t$ is the maximum allowed current slew rate.

For an assumed parasitic inductance of 0.5 nH and a minimum hysteresis of 0.5 V, the maximum slew rate is 1 A/ns. Many applications would exhibit higher current slew rates, up to the 10 A/ns range, which would make this approach impractical. The stability of this approach can be improved by using the IN– input for the PWM signal and locally tying IN+ to VDD. By using the inverting input, the transient voltage applied to the input pin reinforces the PWM signal in a positive feedback loop. While this approach would reduce the probability of false pulses or oscillation, the transient spikes due to high di/dt may overly stress the inputs to the LMG1020. A current-limiting, 100 Ω resistor can be placed right before the IN– input to limit excessive current spikes in the device.

Secondly, for moderate ground-bounce cases, a simple R-C filter can be built with a simple resistor in series with the inputs. By utilizing the input capacitance of LMG1020, the resistor could be close to its input pin. The addition of a small capacitor on the input as supplement can also be helpful. A small time constant of the R-C filter can can enough to filter out high frequency noises. This solution is acceptable for moderate cases in applications where extra delay is acceptable and the pulse width is not extremely short such as 1ns range.

For more extreme cases, or where no delay is tolerable while pulse width is extremely short, using a common-mode choke provides the best results.

One example application where ground-bounce is particularly challenging is when using a current sense resistor. In configuration A LMG1020 ground is connected to the source of GaN FET, while the controller ground is connected to the other side of the current sense resistor as shown in Figure 7. Due to the fast switching and very fast current slew rates, the high ground potential bounce induced by inductance of the sense resistor can disrupt the operation of the circuit or even damage the part. To prevent this, a common-mode choke can be used for IN+ and IN–, respectively. Resistors can also added to the signal output line before LMG1020 depending on the input signal pulse width to provide additional RC filtering. Figure 9 presents the schematic using approach A with the preferred filtering method. Approach B as Figure 8 places the current sense resistor within the gate drive loop path. In this case, the LMG1020 GND pin is connected to the signal ground, and with good ground plane connection, the ground bounce issue can be less severe than approach A. However, the inductance of the current sense resistor adds common-source inductance to the gate drive loop. The voltage generated across this parasitic inductance will subtract from the gate-drive voltage of the FET, slowing down the turnon and turnoff di/dt of the FET, or even cause mis-turn on and off. Additional gate resistance will have to be added to ensure the loop is stable and ring-free. The slower rise may negate the advantage of the fast switching of the GaN FET and may cause additional losses in the circuit. Therefore, this approach is not recommended.

Typical Application (continued)

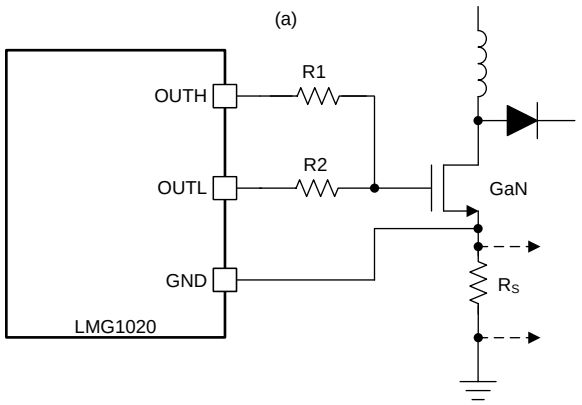


Figure 7. Source Resistor Current Sense A Configuration

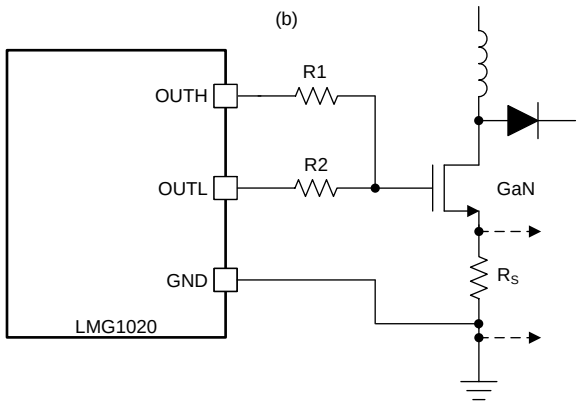


Figure 8. Source Resistor Current Sense B Configuration

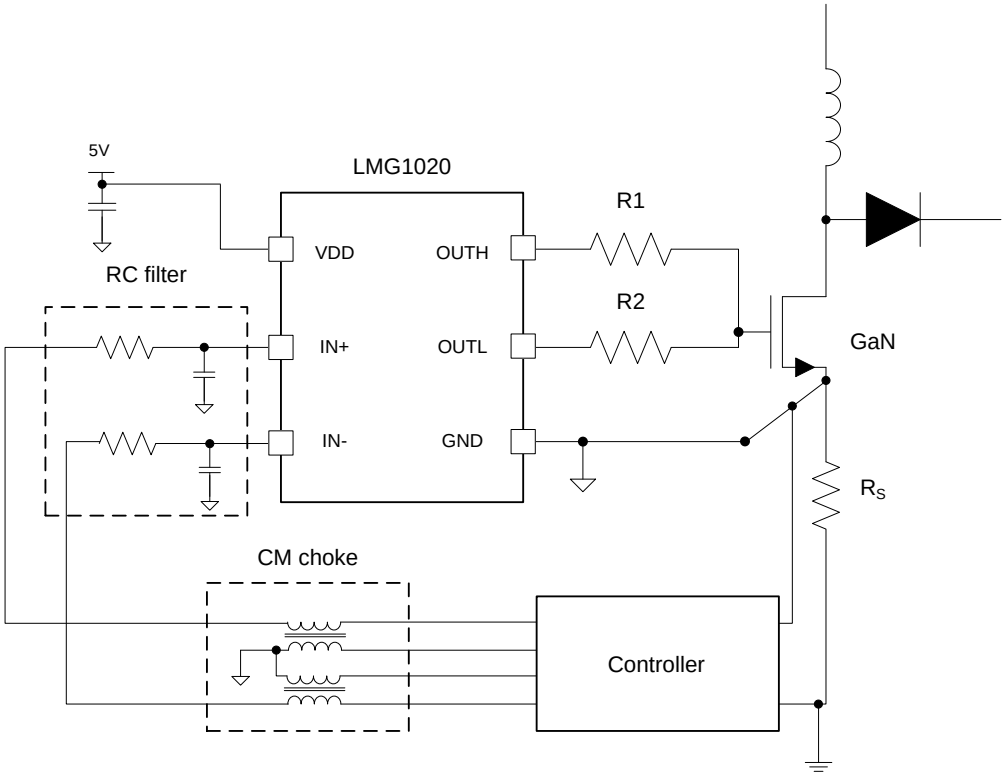


Figure 9. Filtering For Ground Bounce Noise Handling When Using LMG1020

8.2.2.2 Creating Nanosecond Pulse With LMG1020

LMG1020 can be used to drive pulses of nano seconds duration on to a capacitive load. LMG1020 can be driven with a equivalently short pulse on one input pin. However, this takes a sufficiently strong digital driver and careful consideration of the routing parasitics from digital output to input of LMG1020. Two inputs and included AND gate in LMG1020 provide an alternate method to create a short pulse at the LMG1020 output. Starting with both IN+ and IN– at low, taking IN+ high will cause the output to go high. Now if IN– is taken high as well, output will be pulled low. So a digital signal and its delayed version can be applied to IN+ and IN– respectively to create a pulse at the output with width corresponding to the delay between the signals, as shown in Figure 10. The delay

Typical Application (continued)

can be digitally controlled in the nanosecond range. This method alleviates the requirements for driving the input of LMG1020. If a separate delayed version of the digital signal is not available, a RC delay followed by a buffer can be used to derive the second signal. Optionally, if LMG1020 must be driven with a single short duration pulse, that pulse can itself be generated using another LMG1020 by the above method to meet drive requirements.

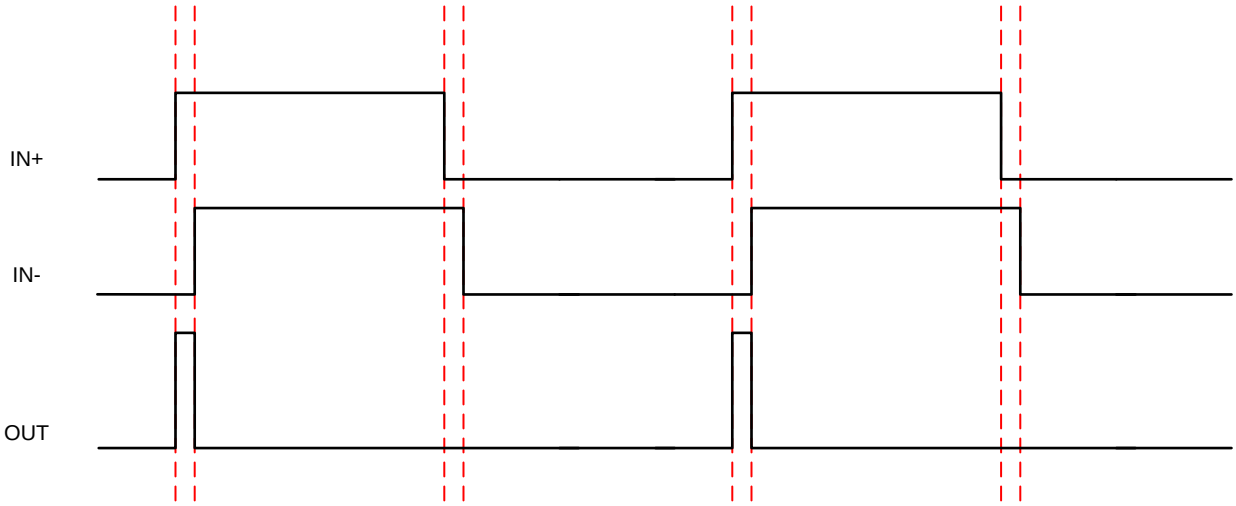


Figure 10. Timing Diagram To Create Short Pulses

8.2.3 VDD and Overshoot

Fast switching with high current is prone to ringing with parasitic inductances, including those on PCB traces. Overshoot associated with such ringing transients need to be evaluated and controlled as a part of the PCB design process to limit device stress. The parameters affecting stress are how high the overshoot is above the absolute maximum specification and the ratio of overshoot duration to the switching time period. Recommended design practice is to limit the overshoots to the absolute maximum pin voltages. This is accomplished with carful PCB layout to minimize parasitic inductances, choice of components with low ESL and addition of series resistance to limit rise times. For large overshoots, limiting the variability of the power supply may be required. For example, 0.5V of overshoot will be permissible with a maximum recommended supply of 5.25 V (5% variability); however, for larger overshoots, a supply with lower variability will be preferred.

8.2.4 Operating at Higher Frequency

With fast rise/fall time, and capability of achieving 1 ns pulse width, depending on the capacitive load condition, the operating frequency of LMG1020 can be increased in a burst manner. In conditions which requires very high frequency pulsing, a pulse train with certain period of pause between each burst can be adopted to avoid overheat of the device. This will help maintain the RMS output current similar as lower frequency operation but boost the transient frequency to very high. In addition, higher decoupling capacitance will be needed to supply high frequency charging of the capacitive load.

Typical Application (continued)

8.2.5 Application Curves

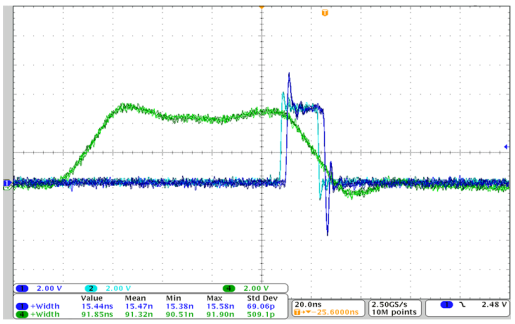


Figure 11. 90 ns Pulse from Function Generator Yielding 15 ns Pulse On The Input (Cyan) And Gate (Blue) After Pulse Shortening

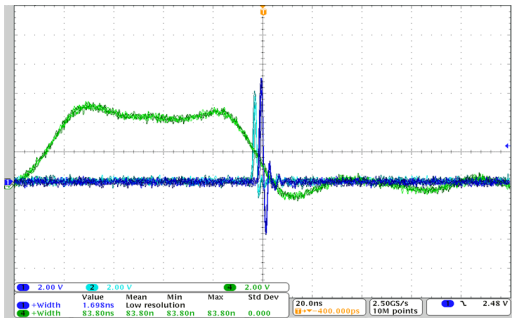


Figure 12. 90 ns Pulse from Function Generator Yielding 1.5 ns Pulse On The Input (Cyan) And Gate (Blue) After Pulse Shortening

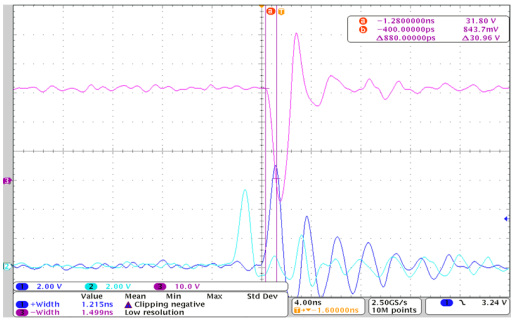


Figure 13. 1.2 ns Gate Pulse Yielding 1.5 ns 30V Into 1 Ω Pulse (500MHz Scope)



Figure 14. V_{DS} for 1.5 ns Pulse With 40V of Bus Voltage

Figure 11 and Figure 12 are the waveforms showing the pulse short pulse generation and input/output pulses. The 90ns long pulse (in green color) and its delayed signal are sent through an AND gate, which outputs a short pulse signal as the input of LMG1020. The output signal (in blue color) follows the input (in cyan color) with certain propagation delay. An output pulse short as 1.5 ns can be obtained as Figure 12.

Figure 13 is taken with a 500MHz oscilloscope and shows typical operation waveforms, including the input logic gating signal (cyan), gate signal (blue), and drain to source signal (pink) of the switching GaN FET. On the drain waveform of the FET, it is possible to see a 20V overshoot. This is due to the inductance in the power loop. Vg seems to be oscillating, but this is caused by pickup noise, which is inevitable even when using a spring ground connection.

Figure 14 shows the waveform of drain to source voltage of a FET driven by LMG1020 with 1.5ns pulse width and 300ps fall time, which drives maximum 60A current at 40V bus voltage.

9 Power Supply Recommendations

A low-ESR/ESL ceramic capacitor must be connected close to the IC, between V_{DD} and GND pins to support the high peak current being drawn from V_{DD} during turnon of the FETs. It is most desirable to place the V_{DD} decoupling capacitor on the same side of the PC board as the driver. The inductance of via holes can impose excessive ringing on the IC pins.

TI recommends the use of a three-terminal capacitor connecting in shunt-through manner to achieve the lowest ESL and best transient performance. This capacitor can be placed as close as possible to the IC, while another capacitor in larger capacitance can be placed closely to the three-terminal cap to supply enough charge but with slightly lower bandwidth. As a general practice, the combination of a 0.1 µF of 0402 or feed-through capacitor (closest to LMG1020) and a 1 µF 0603 capacitor is recommended.

10 Layout

10.1 Layout Guidelines

The layout of the LMG1020 is critical to its performance and functionality. The LMG1020 is available in a WCSP ball-grid array package, which enables low-inductance connection to a BGA-type GaN FET. Figure 15 shows the recommended layout of the LMG1020 with a ball-grid array GaN FET. Figure 16 presents a layout of LMG1020 with a 0.1 µF feed-through capacitor and a larger 1uF capacitor.

A four-layer or higher layer count board is required to reduce the parasitic inductances of the layout to achieve suitable performance. To minimize inductance and board space, resistors and capacitors in the 0201 package are used here. The gate drive power loss must be calculated to ensure an 0201 resistor will be able to handle the power level.

10.1.1 Gate Drive Loop Inductance and Ground Connection

A compact, low-inductance gate-drive loop is essential to achieving fast switching frequencies with the LMG1020. The LMG1020 should be placed as close to the GaN FET as possible, with gate drive resistors R1 and R2 immediately connecting OUTH and OUTL to the FET gate. Large traces must be used to minimize resistance and parasitic inductance.

To minimize gate drive loop inductance, the source return should be on layer 2 of the PCB, immediately under the component (top) layer. Vias immediately adjacent to both the FET source and the LMG1020 GND pin connect to this plane with minimal impedance. Finally, take care to connect the GND plane to the source power plane only at the FET to minimize common-source inductance and to reduce coupling to the ground plane.

10.1.2 Bypass Capacitor

The VDD power terminal of the LMG1020 must by bypassed to ground immediately adjacent to the IC. Because of the fast gate drive of the IC, the placement and value of the bypass capacitor is critical. The bypass capacitor must be place on the top layer, as close as possible to the IC, and connected to both VDD and GND using large power planes. This bypass capacitor has to be at least a 0.1 µF, up to 1 µF, with temperature coefficient X7R or better. Recommended body types are Low Inductance Chip Capacitor (LICC), Inter-Digitated Capacitor (IDC), Feed-through, and LGA. Finally, an additional 1 µF capacitor (not shown in Figure 15) must be placed as close to the IC as practical.

10.2 Layout Example

Figure 15 presents a typical layout of LMG1020 with a 0402 decoupling capacitor C1, which is placed as close as possible to LMG1020. The ground return at GaN FET Kelvin source immediately flows through a via to the closest inner layer, and overlaps with the top layer traces.

Figure 16 presents a layout of LMG1020 with a 0.1 µF feed-through capacitor (C1) and a larger 1uF capacitor (C3) for decoupling. In this design, the feed-through capacitor C1 is placed in a shunt-through manner for lower noise decoupling, and C3 is placed next to C1. 0201 resistors are used at the output of LMG1020, which brings lower parasitic inductance than 0402 package.

Layout Example (continued)

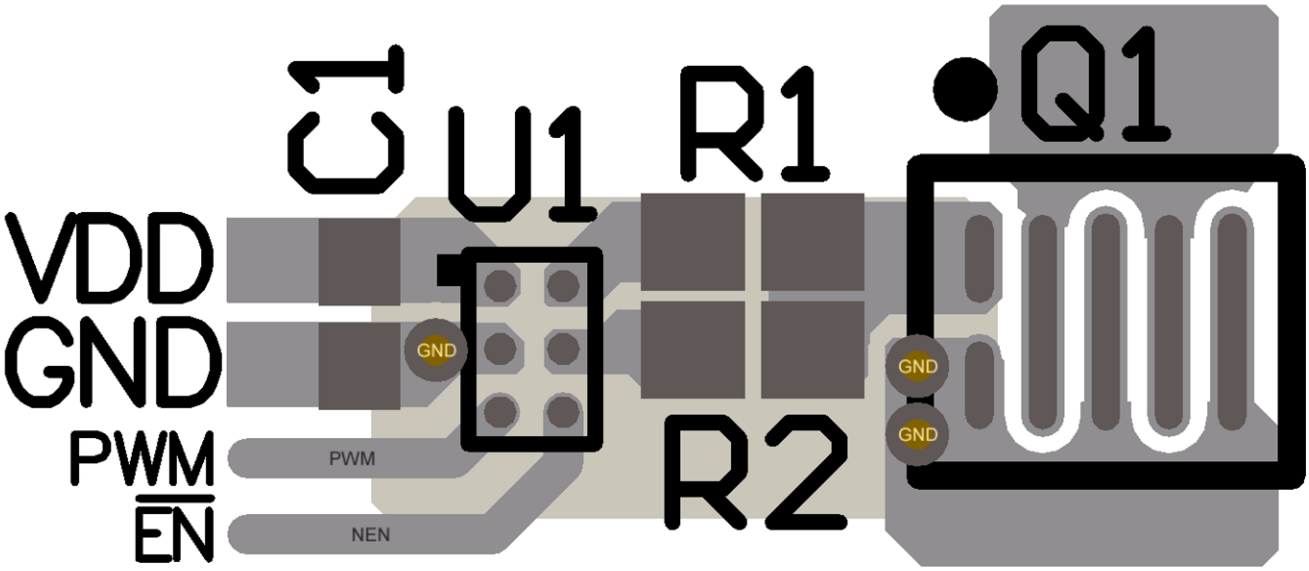


Figure 15. Typical LMG1020 Layout With Ball-Grid GaN FET And 0402 Decoupling Capacitor

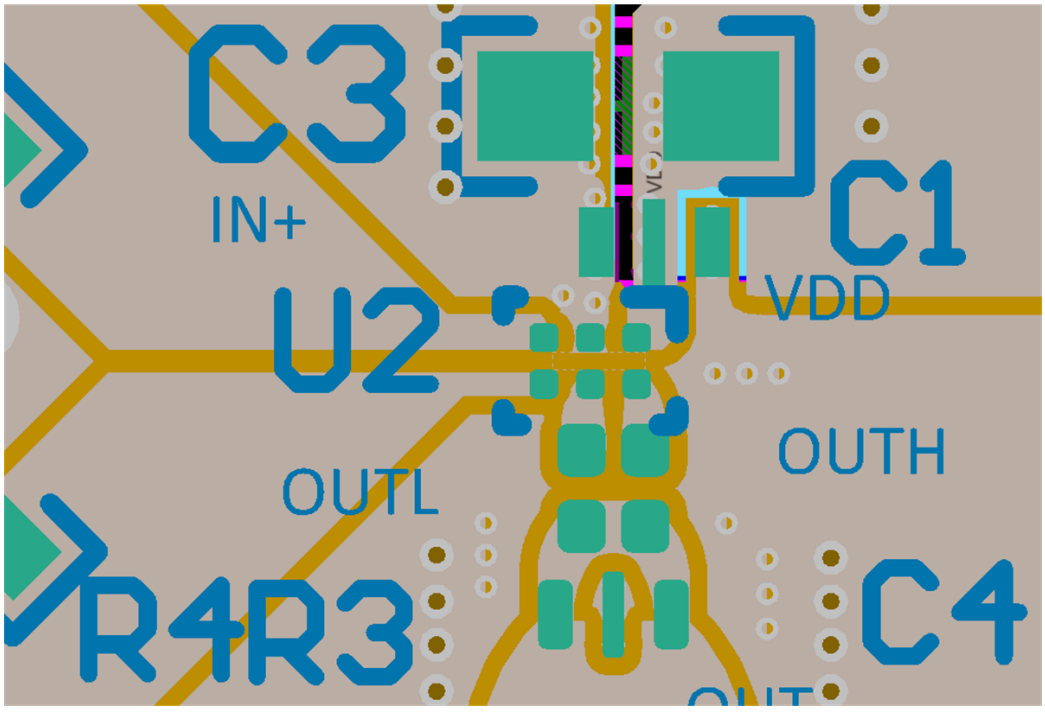


Figure 16. Typical Layout Of LMG1020 And A Feed-Through Decoupling Capacitor With A Capacitor Load

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Using the LMG1020-EVM Nano-second LiDAR EVM* (SNOU150)
- *LMG1020 PSpice Transient Model* (SNOM618)
- *LMG1020 TINA-TI Reference Design* (SNOM619)
- *LMG1020 TINA-TI Transient Spice Model* (SNOM620)
- *LMG1020EVM Altium Design Files* (SNOR025)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMG1020YFFR	ACTIVE	DSBGA	YFF	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	AT	Samples
LMG1020YFFT	ACTIVE	DSBGA	YFF	6	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	AT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

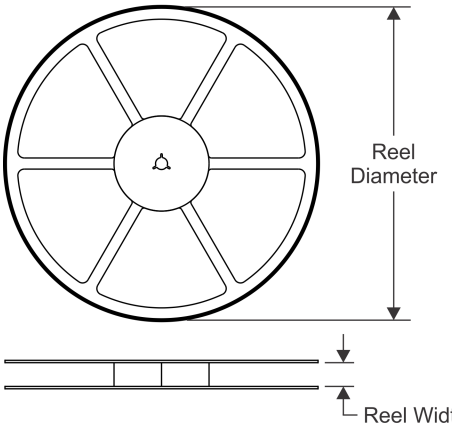
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

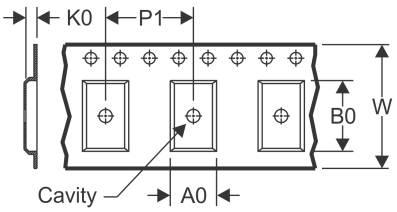
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

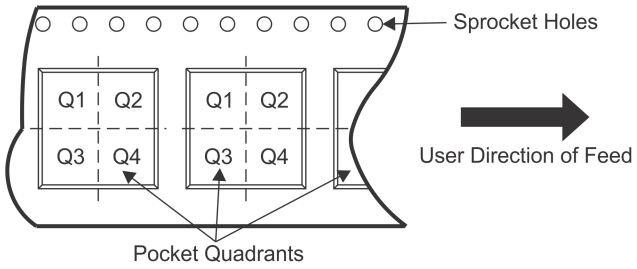


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



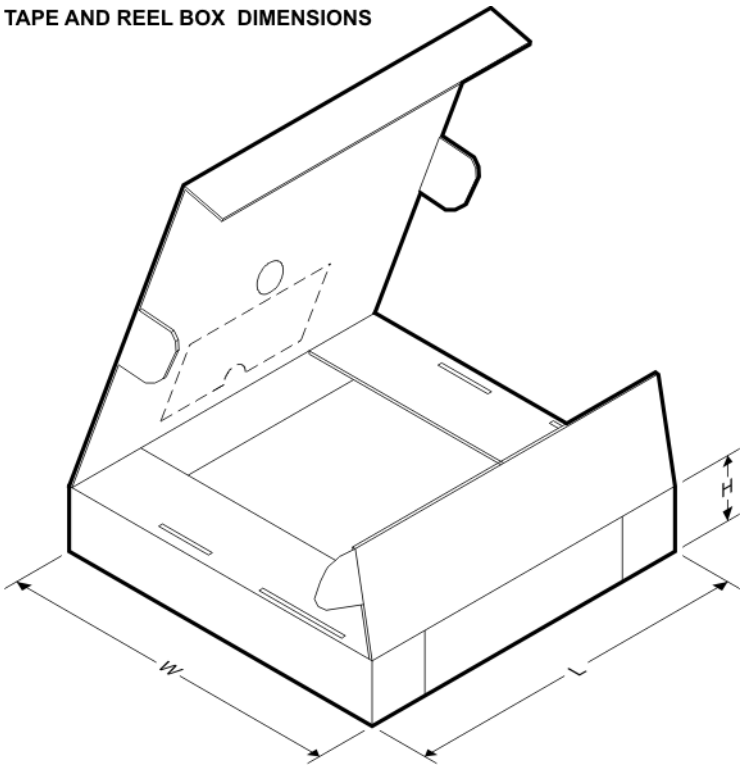
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMG1020YFFR	DSBGA	YFF	6	3000	180.0	8.4	0.96	1.36	0.69	4.0	8.0	Q1
LMG1020YFFT	DSBGA	YFF	6	250	180.0	8.4	0.96	1.36	0.69	4.0	8.0	Q1

PACKAGE MATERIALS INFORMATION

16-Oct-2018

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

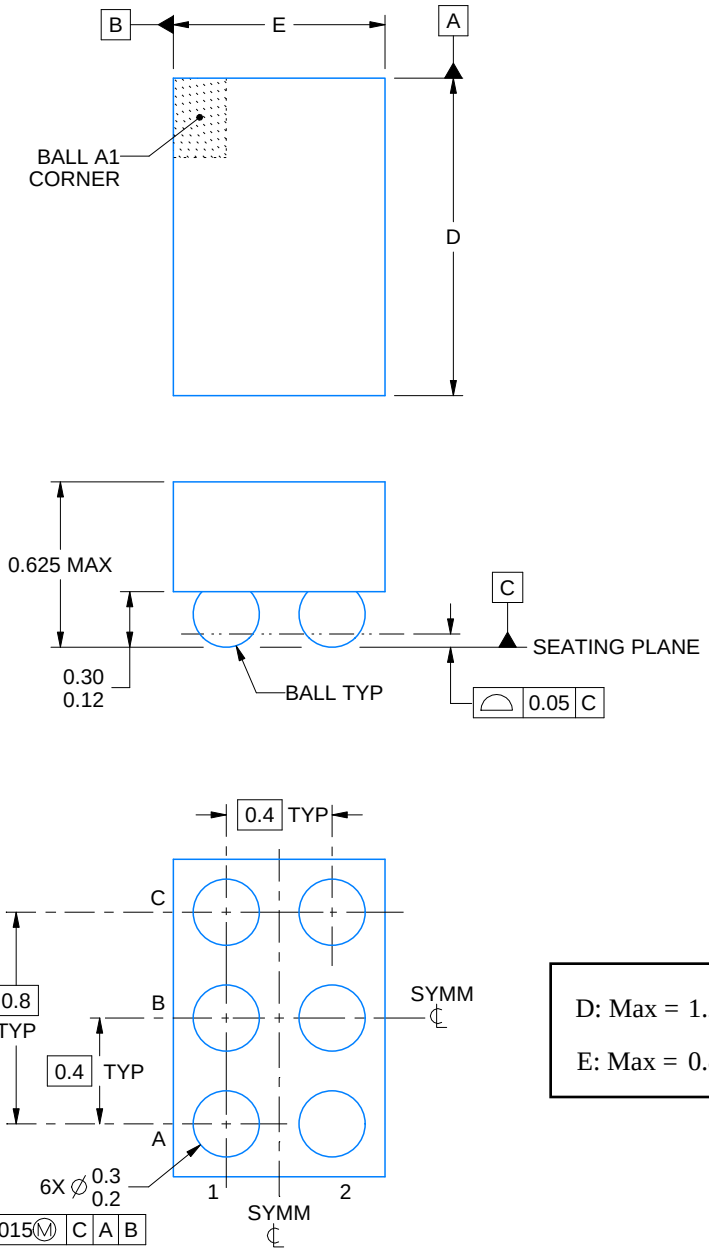
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMG1020YFFR	DSBGA	YFF	6	3000	182.0	182.0	20.0
LMG1020YFFT	DSBGA	YFF	6	250	182.0	182.0	20.0

PACKAGE OUTLINE

YFF0006

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.285 mm, Min =1.225 mm

E: Max = 0.885 mm, Min =0.825 mm

4223785/A 06/2017

NOTES:

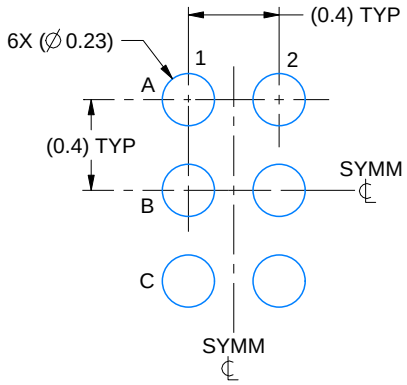
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

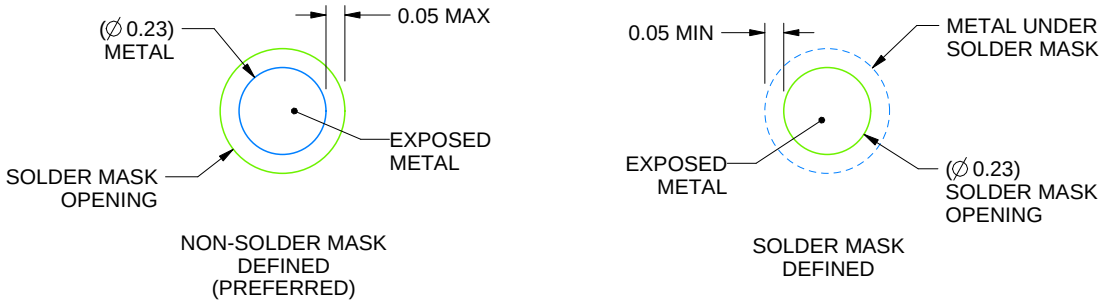
YFF0006

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

4223785/A 06/2017

NOTES: (continued)

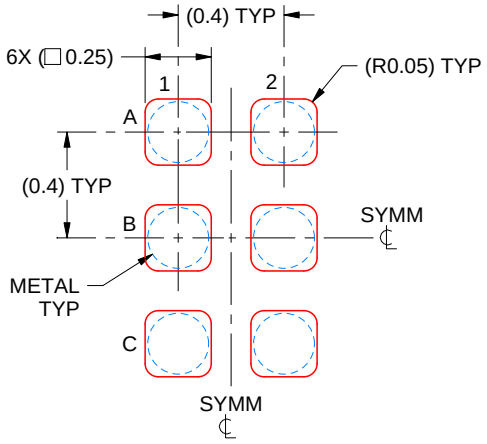
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFF0006

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:35X

4223785/A 06/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.