TPS92692, TPS92692-Q1 High Accuracy LED Controller With Spread Spectrum Frequency Modulation

1 Features

- Wide Input Voltage: 4.5 V to 65 V
- Better than ± 4% LED Current Accuracy over –40°C to 150°C Junction Temperature Range
- Spread Spectrum Frequency Modulation for Improved EMI
- Comprehensive Fault Protection Circuitry with Current Monitor output and Open Drain Fault Flag Indicator
- Internal Analog Voltage to PWM Duty Cycle Generator for stand-alone Dimming Operation
- Compatible with Direct PWM Input with over 1000:1 Dimming Range
- Analog LED Current Adjust Input (IADJ) with over 15:1 Contrast Ratio
- Integrated P-Channel Driver to enable Series FET Dimming and LED Protection
- TPS92692-Q1: Automotive Q100 Grade 1 Qualified

2 Applications

- TPS92692-Q1: Automotive Exterior Lighting Applications
- Driver Monitoring Systems (DMS)
- LED General Lighting Applications
- Exit Signs and Emergency Lighting

3 Description

The TPS92692 and TPS92692-Q1 are high accuracy peak current mode based controllers designed to support step-up/down LED driver topologies. The device incorporates a rail-to-rail current amplifier to measure LED current and spread spectrum frequency modulation technique for improved EMI performance.

This high performance LED controller can independently modulate LED current using either analog or PWM dimming techniques. Linear analog dimming response with over 15:1 range is obtained by varying the voltage across the high impedance analog adjust (IADJ) input. PWM dimming of LED current is achieved by directly modulating the DIM/PWM input pin with the desired duty cycle or by enabling the internal PWM generator circuit. The PWM generator translates the DC voltage at DIM/PWM pin to corresponding duty cycle by comparing it to the internal triangle wave generator. The optional PDRV gate driver output can be used to drive an external P-Channel series MOSFET.

The TPS92692 and TPS92692-Q1 devices support continuous LED status check through the current monitor (IMON) output. The devices also include an open drain fault indicator output to indicate LED overcurrent, output overvoltage and output undervoltage conditions.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS92692-Q1	HTSSOP (20)	5.10 mm × 6.60 mm
TPS92692		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Typical Boost LED Driver

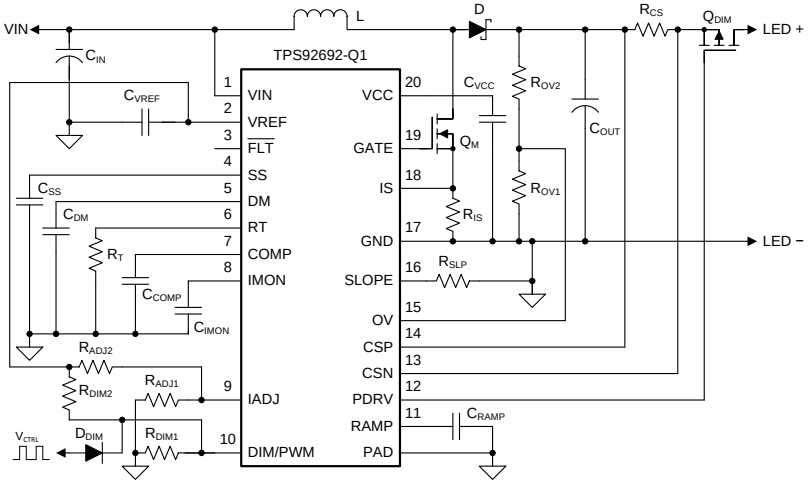


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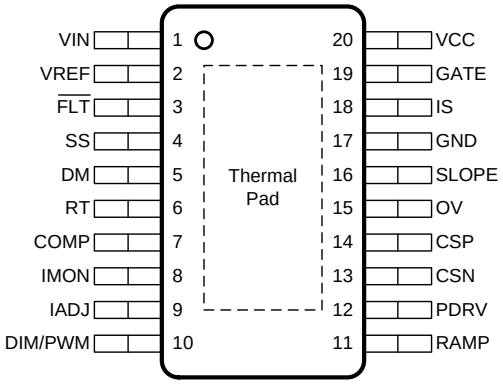
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5 Revision History

DATE	REVISION	NOTES
March 2017	*	Initial release.

6 Pin Configuration and Functions

PWP Package
20-Pin HTSSOP with PowerPAD™
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
COMP	7	I/O	Transconductance error amplifier output. Connect compensation network to achieve desired closed-loop response.
CSN	13	I	Current sense amplifier negative input (–). Connect directly to the negative node of LED current sense resistor, R_{CS}.
CSP	14	I	Current sense amplifier positive input (+). Connect directly to the positive node of LED current sense resistor, R_{CS}.
DIM/PWM	10	I	External analog to PWM dimming command or direct PWM dimming input. The external analog dimming command between 1 V and 3 V is compared to the internal PWM generator triangle waveform to set LED current duty cycle between 0% and 100%. With PWM generator disabled, a direct PWM dimming command can be applied to control the LED current duty cycle and frequency. The analog or PWM command is used to generate an internal PWM signal that controls the GATE and PDRV outputs. Setting the internal PWM signal to logic level low, turns off switching, idles the oscillator, disconnects the COMP pin, and sets PDRV to V_{CSP}. Connect to VREF when not used for PWM dimming.
DM	5	I/O	Triangle wave spread spectrum modulation frequency, f_m, programming pin. Connect a capacitor to GND to set the spread spectrum modulating frequency. Connect directly to GND to disable spread spectrum modulation of switching frequency.
$\overline{\text{FLT}}$	3	O	Open-drain fault indicator. Connect to VREF with a resistor to create active low fault signal output. Internal LED short circuit protection and auto-restart timer can enabled by directly connecting the pin to SS input.
GATE	19	O	N-channel MOSFET gate driver output. Connect to gate of external main switching N-channel MOSFET.
GND	17	—	Analog and Power ground connection pin. Connect to circuit ground to complete return path.
IADJ	9	I	LED current reference input. Connect this pin to VCC with a 100-kΩ series resistor to set the internal reference voltage to 2.42 V and the current sense threshold, $V_{(CSP-CSN)}$ to 170.7 mV. The pin can be modulated by an external voltage source from 140 mV to 2.25 V to implement analog dimming.
IMON	8	O	LED current report pin. The LED current sensed by CSP/CSN input is reported as $V_{IMON} = 14 \times I_{LED} \times R_{CS}$. Bypass with a 1-nF ceramic capacitor connected to GND.
IS	18	I	Switch current sense input. Connect to the switch sense resistor, R_{IS} to set the switch current limit threshold based on the internal 250 mV reference.
OV	15	I	Output voltage input. Connect a resistor divider from output voltage to GND to set output overvoltage and under-voltage protection thresholds.
PDRV	12	O	Series dimming P-channel FET gate driver output. Connect to gate of external P-channel MOSFET to implement series FET PWM dimming and fault disconnect.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
RAMP	11	I/O	Programming input for internal PWM generator. Connect a capacitor to GND to set the triangle wave frequency for PWM generator circuit. Connect a 249-kΩ resistor to GND to disable the PWM generator and to set a fixed reference for direct external PWM dimming input. Do not allow this pin to float.
RT	6	I/O	Oscillator frequency programming pin. Connect a resistor to GND to set the switching frequency. The internal oscillator can be synchronized by coupling an external clock pulse through a series capacitor with a value of 100 nF.
SLOPE	16	I/O	Slope compensation input. Connect a resistor to GND to set the desired slope compensation ramp based on inductor value, input and output voltages.
SS	4	I/O	Soft-start programming pin. Connect a capacitor to GND to extend the start-up time. Switching can be disabled by shorting this pin to GND.
VCC	20	—	VCC (7.5 V) bias supply pin. Locally decouple to GND using a ceramic capacitor (with a value between 2.2-µF and 4.7-µF). Locate close to the controller.
VIN	1	—	Input supply for the internal regulators. Bypass with a low-pass filter using a series 10-Ω resistor and 10- nF capacitor connected to GND. Locate the capacitor close to the controller.
VREF	2	—	VREF (5 V) bias supply pin. Locally decouple to GND using a ceramic capacitor (with a value between 2.2-µF and 4.7-µF) located close to the controller.
Thermal Pad		—	The GND pin must be connected to the exposed thermal pad for proper operation. This PowerPAD must be connected to PCB ground plane using multiple vias for good thermal performance.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Input voltage	VIN, CSP, CSN	–0.3	65	V
	DIM/PWM	–0.3	14	V
	IS, RT, $\overline{FLT}$	–0.3	8.8	V
	OV, SS, RAMP, DM, SLOPE, VREF, IADJ	–0.3	5.5	V
	CSP to CSN(3)	–0.3	0.3	V
Output voltage(4)	VCC, GATE	–0.3	8.8	V
	PDRV	V_{CSP} – 8.8	V_{CSP}	V
	COMP	–0.3	5.0	V
Source current	IMON	—	100	µA
	GATE (pulsed < 20 ns)	—	500	mA
	PDRV (pulsed < 10 µs)	—	50	mA
Sink current	GATE (pulsed < 20 ns)	—	500	mA
	PDRV (pulsed < 10 µs)	—	50	mA
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}			165	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND unless otherwise noted
(3) Continuous sustaining voltage
(4) All output pins are not specified to have an external voltage applied.

7.2 ESD Ratings

				VALUE	UNIT
TPS92692-Q1 IN PWP (HTSSOP) PACKAGE					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002, all pins[1]		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins except 1, 10, 11, and 20	±500	
			Pins 1, 10, 11, and 20	±750	
TPS92692 IN PWP (HTSSOP) PACKAGE					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[2]		±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins[3]		±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Supply input voltage	6.5	14	65	V
VIN, crank	Supply input, battery crank voltage	4.5			V
V_{CSP}, V_{CSN}	Current sense common mode	6.5		60	V
f_{SW}	Switching frequency	80		800	kHz
f_m	Spread spectrum modulation frequency	0.1		12	kHz
f_{RAMP}	Internal PWM ramp generator frequency	100		2000	Hz
V_{IADJ}	Current reference voltage	0.14		$V_{IADJ(CLAMP)}$	V
T_A	Operating ambient temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC[1]		TPS92692 PWP (HTSSOP) 20 PINS	TPS92692-Q1 PWP (HTSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.8	40.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.1	26.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.2	22.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.0	22.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.3	2.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

–40°C ≤ T_J ≤ 150°C, V_{IN} = 14 V, V_{IADJ} = 2.1 V, V_{RAMP} = 500 mV, $V_{DIM/PWM}$ = 3 V, V_{OV} = 500 mV, C_{VCC} = 1 µF, C_{VREF} = 1 µF, C_{COMP} = 2.2 nF, R_{CS} = 100 mΩ, R_T = 20 kΩ, no load on GATE and PDRV (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE (VIN)						
$I_{IN(STBY)}$	Input stand-by current	V_{PWM} = 0 V		1.8	2.5	mA
$I_{IN(SW)}$	Input switching current	V_{CC} = 7.5 V, C_{GATE} = 1 nF		5.1	6.6	mA
BIAS SUPPLY (VCC)						
$V_{CC(REG)}$	Regulation voltage	No load	7.0	7.5	8.0	V
$V_{CC(UVLO)}$	Supply undervoltage protection	VCC rising threshold, V_{IN} = 8 V		4.5	4.9	V
		VCC falling threshold, V_{IN} = 8 V	3.7	4.1		V
		Hysteresis		400		mV
$I_{CC(LIMIT)}$	Supply current limit	V_{CC} = 0 V	30	36	46	mA
V_{DO}	LDO dropout voltage	I_{CC} = 20 mA, V_{IN} = 5 V		300		mV
REFERENCE VOLTAGE (VREF)						
VREF	Reference voltage	No load	4.77	4.96	5.15	V
$I_{REF(LIMIT)}$	Current limit	V_{REF} = 0 V	30	36	46	mA
OSCILLATOR (RT)						
f_{SW}	Switching frequency	R_T = 40 kΩ	175	200	225	kHz
		R_T = 20 kΩ	341	390	439	kHz
V_{RT}	RT output voltage			1		V
V_{SYNC}	SYNC rising threshold	V_{RT} rising		2.5	3.1	V
	SYNC falling threshold	V_{RT} falling	1.8	2		V
$t_{SYNC(MIN)}$	Minimum SYNC clock pulse width			100		ns
SPREAD SPECTRUM FREQUENCY MODULATION (DM)						
I_{DM}	Triangle wave generator sink current			10		µA
	Triangle wave generator source current			10		µA
$V_{DM(TR)}$	Triangle wave voltage peak (High)			1.15		V
	Triangle wave voltage valley (Low)			850		mV
$V_{DM(EN)}$	Spread spectrum modulation enable threshold			700		mV
$V_{DM(CLAMP)}$	Internal clamp voltage	V_{PWM} = 0 V, R_{RAMP} = 200 kΩ		1.25		V
GATE DRIVER (GATE)						
R_{GH}	Gate driver high side resistance	I_{GATE} = –10 mA		5.4	11.2	Ω
R_{GL}	Gate driver low side resistance	I_{GATE} = 10 mA		4.3	10.5	Ω
CURRENT SENSE (IS)						
$V_{IS(LIMIT)}$	Current limit threshold	$V_{DIM/PWM}$ = 5 V, R_{RAMP} = 249 kΩ	230.6	250	270	mV
		$V_{DIM/PWM}$ = 0 V, R_{RAMP} = 249 kΩ	665	700	735	mV
$t_{IS(BLANK)}$	Leading edge blanking time		88	118	158	ns
$t_{IS(FAULT)}$	Current limit fault time			35		µs
$t_{ILMT(DLY)}$	IS to GATE propagation delay	V_{IS} pulsed from 0 V to 1 V		78		ns

(1) All voltages are with respect to GND unless otherwise noted

Electrical Characteristics (continued)

–40°C ≤ T_J ≤ 150°C, V_{IN} = 14 V, V_{IADJ} = 2.1 V, V_{RAMP} = 500 mV, $V_{DIM/PWM}$ = 3 V, V_{OV} = 500 mV, C_{VCC} = 1 µF, C_{VREF} = 1 µF, C_{COMP} = 2.2 nF, R_{CS} = 100 mΩ, R_T = 20 kΩ, no load on GATE and PDRV (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM COMPARATOR AND SLOPE COMPENSATION (SLOPE)						
D_{MAX}	Maximum duty cycle			90		%
V_{SLOPE}	Adaptive slope compensation	V_{CSP} = 24 V		410		mV
$V_{SLOPE(MIN)}$	Minimum slope compensation output voltage	V_{CSP} = 0 V		72		mV
V_{LV}	IS to COMP level shift voltage	No slope compensation added	1.42	1.60	1.82	V
I_{LV}	IS level shift bias current	No slope compensation added		17		µA
CURRENT SENSE AMPLIFIER (CSP, CSN)						
$V_{(CSP-CSN)}$	Current sense thresholds	V_{CSP} = 14 V, V_{IADJ} = 3 V	163.4	170.7	177.6	mV
		V_{CSP} = 14 V, V_{IADJ} = 1.4 V	95.83	100.5	103.85	mV
$CS_{(BW)}$	Current sense unity gain bandwidth			500		kHz
G_{CS}	Current sense amplifier gain	G = $V_{IADJ}/V_{(CSP-CSN)}$		14		
$K_{(OCP)}$	Ratio of over-current detection threshold to analog adjust voltage	K $_{(OCP)}$ = $V_{(OCP-THR)}/V_{IADJ}$	1.46	1.5	1.61	
$I_{CSP(BIAS)}$	CSP bias current	V_{CSN} = 14.1 V, V_{CSP} = 14 V		107		µA
$I_{CSN(BIAS)}$	CSN bias current	V_{CSN} = 14.1 V, V_{CSP} = 14 V		110		µA
FAULT INDICATOR ($\overline{FLT}$)						
$R_{(FLT)}$	Open-drain pull down resistance			241		Ω
$t_{(FAULT_TMR)}$	Fault timer		24	36	48	ms
CURRENT MONITOR (IMON)						
$I_{IMON(SRC)}$	IMON source current	$V_{(CSP-CSN)}$ = 150 mV, V_{IMON} = 0 V			144	µA
$V_{IMON(CLP)}$	IMON output voltage clamp		3.2	3.7	4.2	V
$V_{IMON(OS)}$	IMON buffer offset voltage		–7.2	0	8.5	mV
ANALOG ADJUST (IADJ)						
$V_{IADJ(CLP)}$	IADJ internal clamp voltage	I_{IADJ} = 1 µA	2.29	2.40	2.55	V
$I_{IADJ(BIAS)}$	IADJ input bias current	V_{IADJ} < 2.2 V		10.5		nA
$R_{IADJ(LMT)}$	IADJ current limiting series resistor	V_{IADJ} > 2.6 V		12		kΩ
ERROR AMPLIFIER (COMP)						
g_M	Transconductance			121		µA/V
$I_{COMP(SRC)}$	COMP current source capacity	V_{IADJ} = 1.4 V, $V_{(CSP-CSN)}$ = 0 V		130		µA
$I_{COMP(SINK)}$	COMP current sink capacity	V_{IADJ} = 0 V, $V_{(CSP-CSN)}$ = 0.1 V		130		µA
$EA_{(BW)}$	Error amplifier bandwidth	Gain = –3 dB		5		MHz
$V_{COMP(RST)}$	COMP pin reset voltage			100		mV
$R_{COMP(DCH)}$	COMP discharge FET resistance			246		Ω
SOFT-START (SS)						
I_{SS}	Soft-start source current		7	10	12.8	µA
$V_{SS(UVP_EN)}$	Soft-start voltage threshold to enable output under-voltage protection			2.4		V
$V_{SS(RST)}$	Soft-start pin reset voltage			50		mV
$R_{SS(DCH)}$	SS discharge FET resistance			240		Ω
OUTPUT VOLTAGE INPUT (OV)						
$V_{OVP(THR)}$	Overvoltage protection threshold		1.195	1.228	1.262	V
$V_{UVP(THR)}$	Undervoltage protection threshold		81.7	100	115.1	mV
$t_{(UVP-BLANK)}$	Undervoltage protection blanking period			4		µs
$I_{OVP(HYS)}$	OVP hysteresis current		12	20	27.5	µA

Electrical Characteristics (continued)

–40°C ≤ T_J ≤ 150°C, V_{IN} = 14 V, V_{IADJ} = 2.1 V, V_{RAMP} = 500 mV, $V_{DIM/PWM}$ = 3 V, V_{OV} = 500 mV, C_{VCC} = 1 µF, C_{VREF} = 1 µF, C_{COMP} = 2.2 nF, R_{CS} = 100 mΩ, R_T = 20 kΩ, no load on GATE and PDRV (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL PWM RAMP GENERATOR (RAMP)						
I_{RAMP}	Ramp generator source current		7.75	10	12.73	µA
	Ramp generator sink current		8.24	10	12.41	µA
V_{RAMP}	Ramp signal peak (high)			3		V
	Ramp signal valley (low)			1		V
PWM INPUT (DIM/PWM)						
$V_{PWM(HIGH)}$	Schmitt trigger logic level (high threshold)	V_{RAMP} = 2.0 V		2.0	2.2	V
$V_{PWM(LOW)}$	Schmitt trigger logic level (low threshold)	V_{RAMP} = 2.0 V	1.8	2.0		V
$R_{PWM(PD)}$	PWM pull-down resistance			10		MΩ
$t_{DLY(RISE)}$	PWM rising to PDRV delay	C_{PDRV} = 1 nF		294		ns
$t_{DLY(FALL)}$	PWM falling to PDRV delay	C_{PDRV} = 1 nF		326		ns
SERIES P-CHANNEL PWM FET GATE DRIVE OUTPUT (PDRV)						
$V_{PDRV(OFF)}$	P-channel gate driver off-state voltage	V_{CSP} = 14 V		14		V
$V_{PDRV(ON)}$	P-channel gate driver on-state voltage	V_{CSP} = 14 V		7.4		V
$I_{PDRV(SRC)}$	PDRV sink current	Pulsed		50		mA
$R_{PDRV(L)}$	PDRV driver pull up resistance			82		Ω
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature			175		°C
$T_{SD(HYS)}$	Thermal shutdown hysteresis			25		°C

7.6 Typical Characteristics

T_A = 25°C, V_{IN} = 14 V, V_{IADJ} = 2.2 V, C_{VCC} = 1 µF, C_{COMP} = 2.2 nF, R_{CS} = 100 mΩ, R_T = 20 kΩ, V_{PWM} = 5 V, no load on GATE and PDRV (unless otherwise noted)

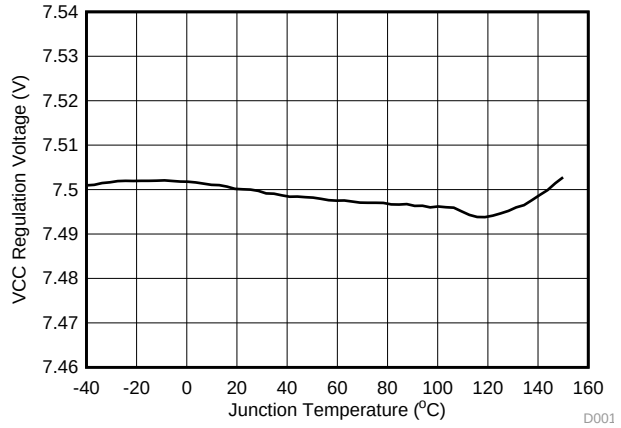


Figure 1. VCC Regulation Voltage vs Junction Temperature

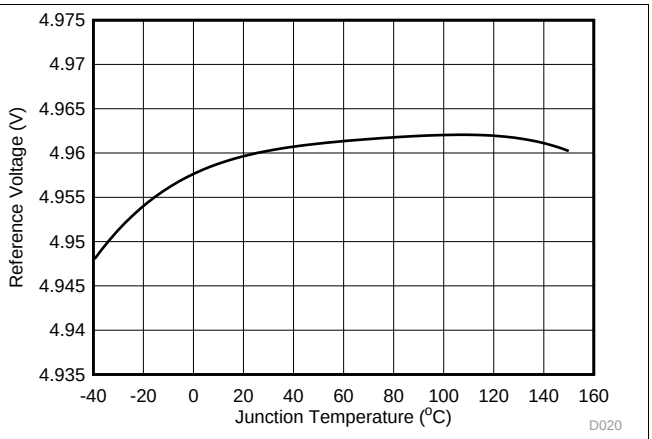
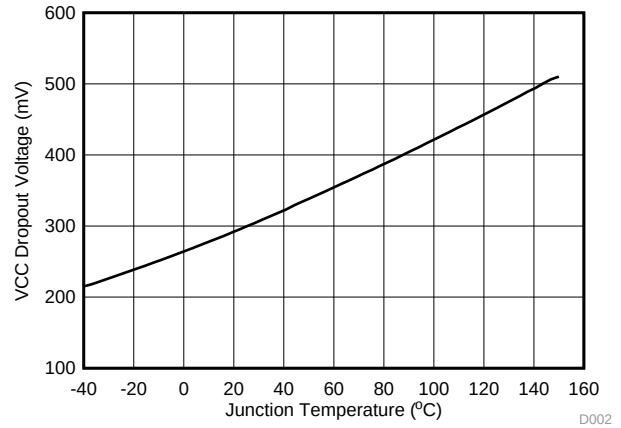


Figure 2. VREF Reference Voltage vs Junction Temperature



V_{IN} = 5 V, I_{VCC}= 20 mA

Figure 3. VCC Dropout Voltage vs Junction Temperature

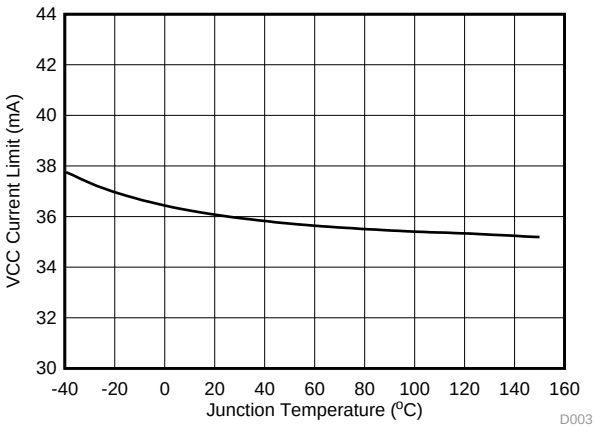


Figure 4. VCC Current Limit vs Junction Temperature

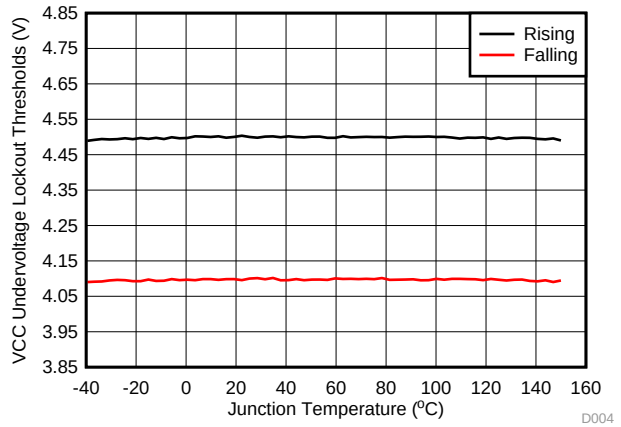


Figure 5. VCC UVLO Threshold vs Junction Temperature

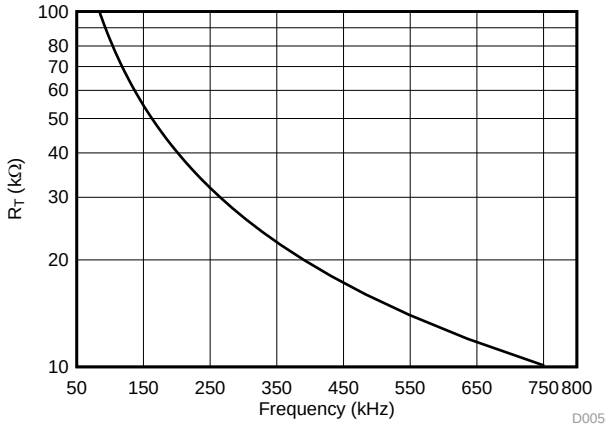
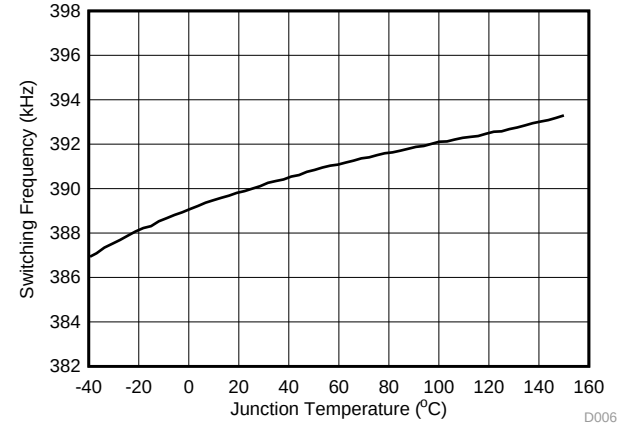


Figure 6. Timing Resistance (RT) vs Switching Frequency

Typical Characteristics (continued)

T_A = 25°C, V_{IN} = 14 V, V_{IADJ} = 2.2 V, C_{VCC} = 1 µF, C_{COMP} = 2.2 nF, R_{CS} = 100 mΩ, R_T = 20 kΩ, V_{PWM} = 5 V, no load on GATE and PDRV (unless otherwise noted)



R_T= 20 kΩ

Figure 7. Switching Frequency vs Junction Temperature

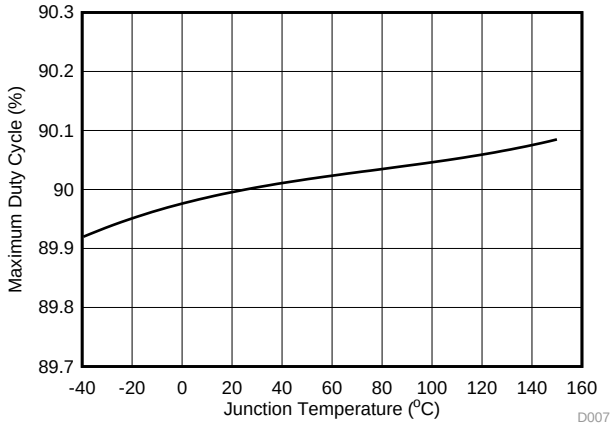


Figure 8. Maximum Duty Cycle vs Junction Temperature

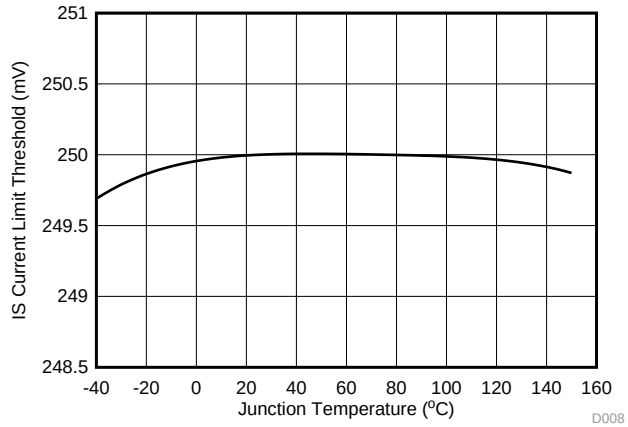


Figure 9. Current Limit Threshold vs Junction Temperature

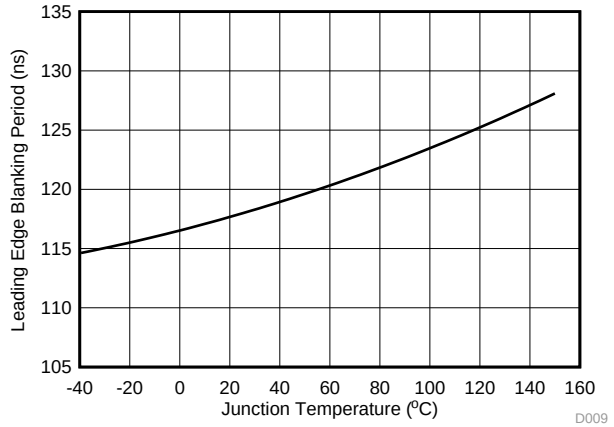
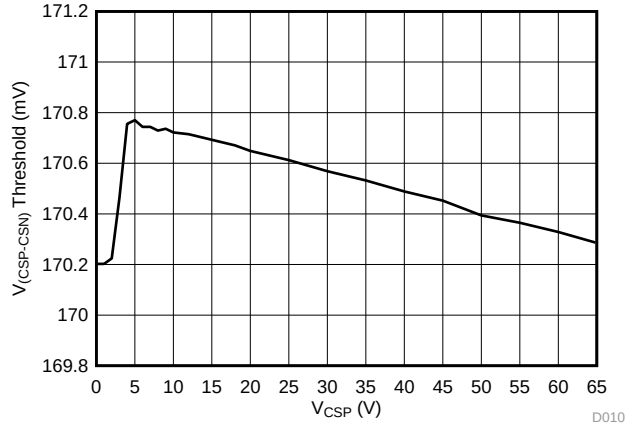
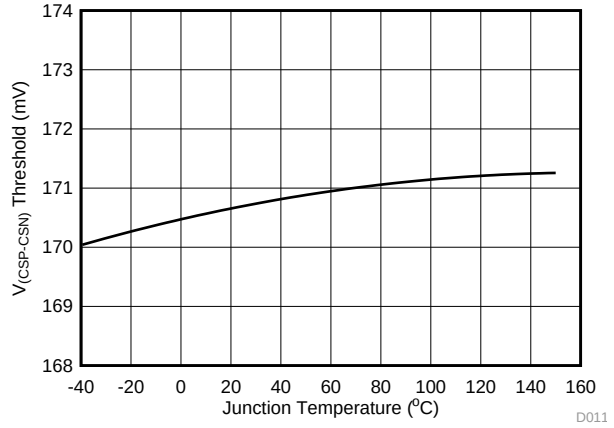


Figure 10. Leading Edge Blanking Period vs Junction Temperature



V_{IADJ}> 2.6 V

Figure 11. $V_{(CSP-CSN)}$ Threshold vs V_{CSP} Voltage

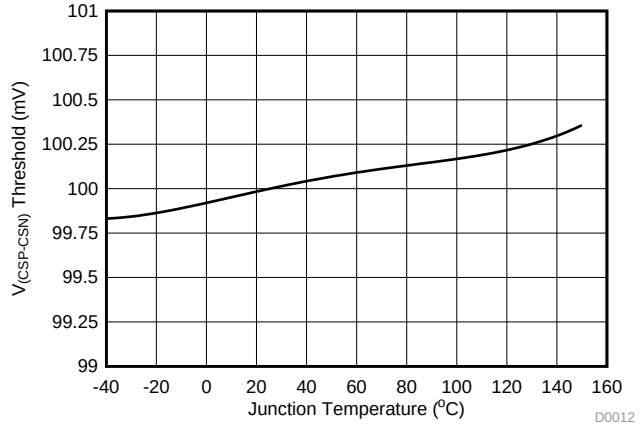


V_{IADJ}> 2.6 V

Figure 12. $V_{(CSP-CSN)}$ Threshold vs Junction Temperature

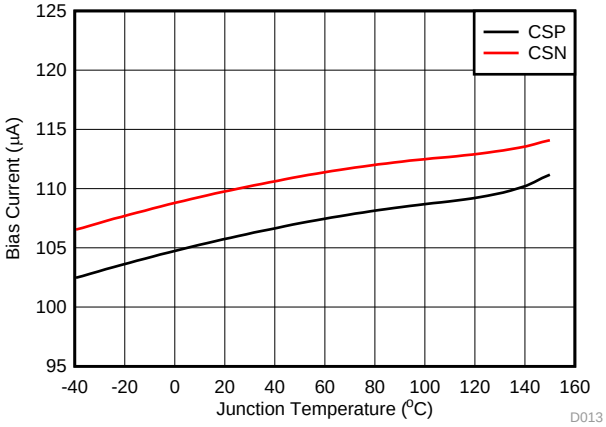
Typical Characteristics (continued)

T_A = 25°C, V_{IN} = 14 V, V_{IADJ} = 2.2 V, C_{VCC} = 1 µF, C_{COMP} = 2.2 nF, R_{CS} = 100 mΩ, R_T = 20 kΩ, V_{PWM} = 5 V, no load on GATE and PDRV (unless otherwise noted)



V_{IADJ}= 1.4 V

Figure 13. $V_{(CSP-CSN)}$ Threshold vs Junction Temperature



V_{CSP}= V_{CSN} = 14 V

Figure 14. CSP/CSN Input Bias Current vs Junction Temperature

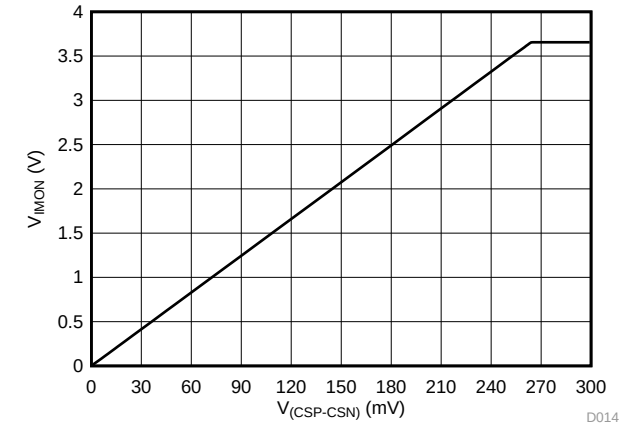


Figure 15. V_{IMON} vs $V_{(CSP-CSN)}$

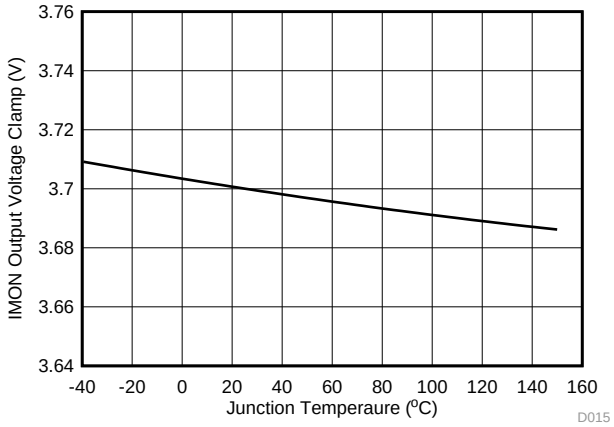


Figure 16. $V_{IMON(CLP)}$ vs Junction Temperature

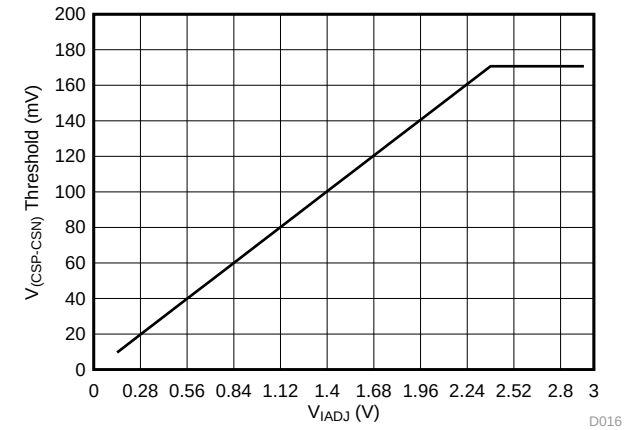


Figure 17. $V_{(CSP-CSN)}$ Threshold vs V_{IADJ}

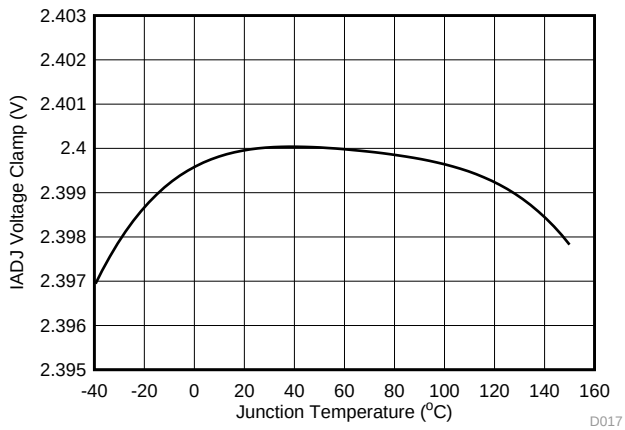


Figure 18. V_{IADJ} Voltage Clamp vs Junction Temperature

Typical Characteristics (continued)

T_A = 25°C, V_{IN} = 14 V, V_{IADJ} = 2.2 V, C_{VCC} = 1 µF, C_{COMP} = 2.2 nF, R_{CS} = 100 mΩ, R_T = 20 kΩ, V_{PWM} = 5 V, no load on GATE and PDRV (unless otherwise noted)

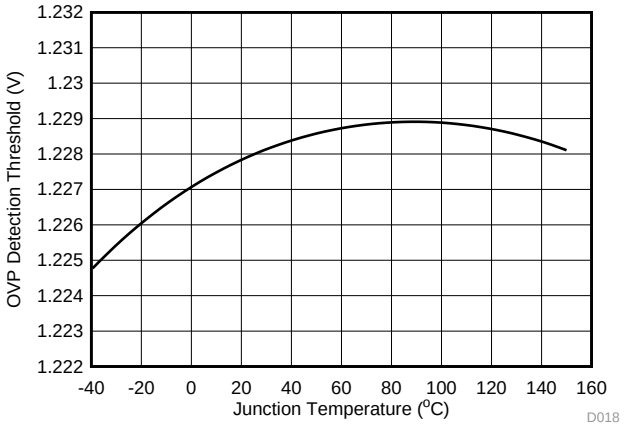


Figure 19. OVP Detection Threshold vs Junction Temperature

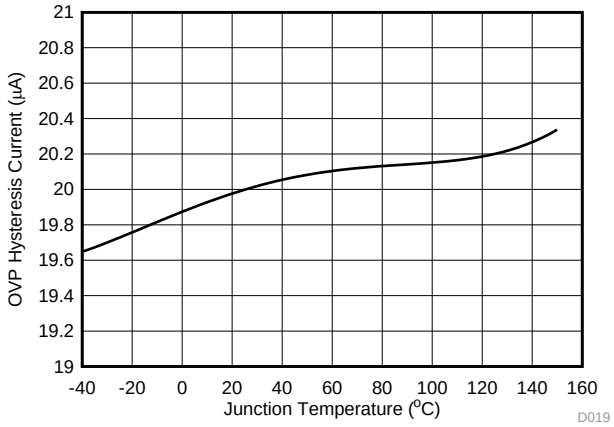


Figure 20. OVP Hysteresis Current vs Junction Temperature

8 Detailed Description

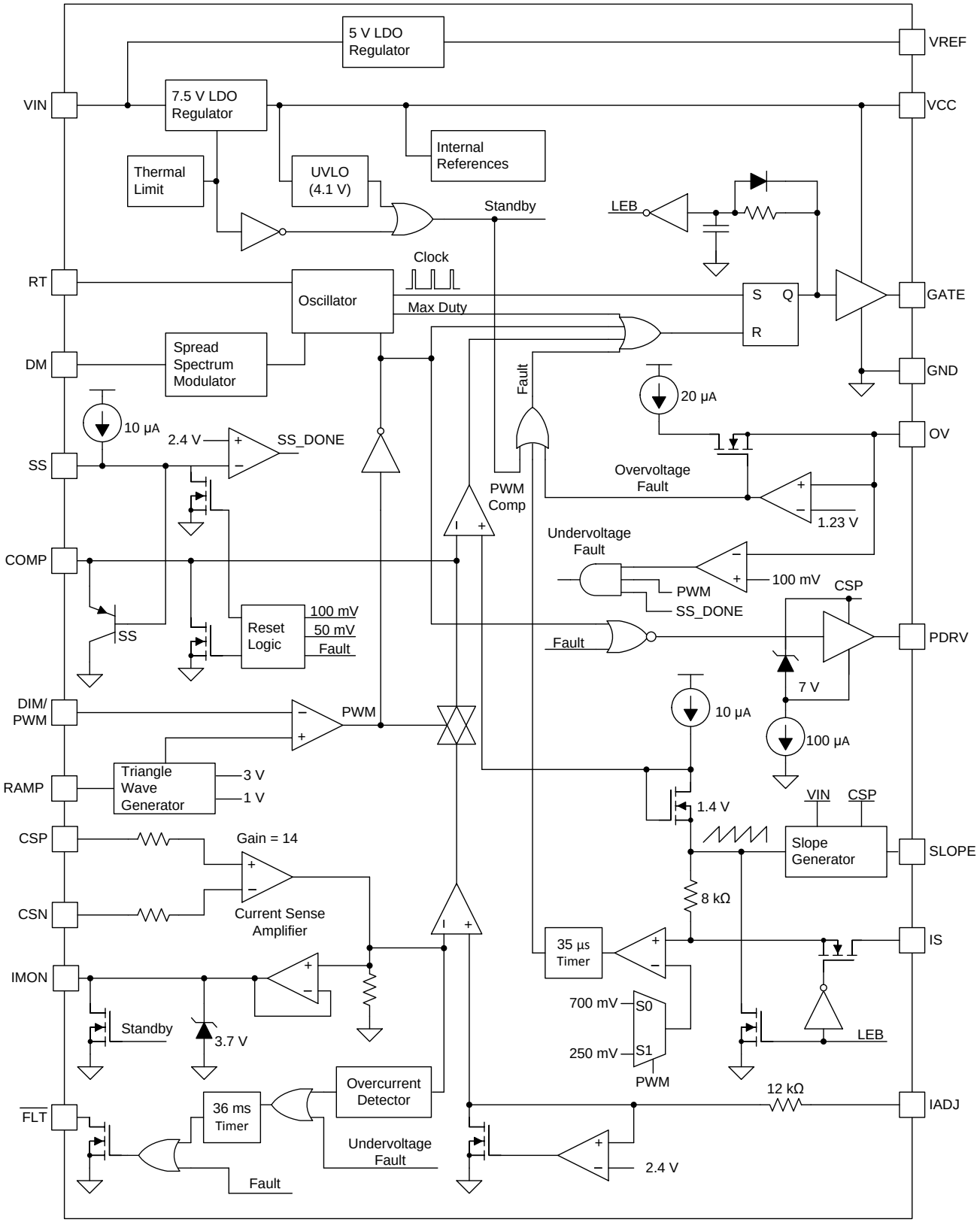
8.1 Overview

The TPS92692 and TPS92692-Q1 devices feature all of the functions necessary to implement a compact LED driver based on step-up or step-down power converter topologies. The devices implement a fixed-frequency, peak current mode control technique to achieve constant output current and fast transient response. The integrated low offset, rail-to-rail current sense amplifier provides the flexibility required to power a single string consisting of 1 to 20 series connected LEDs while maintaining better than 4% current accuracy over the operating temperature range. The LED current regulation threshold is set by the analog adjust input, IADJ and can be externally programmed to implement analog dimming with over 15:1 linear dimming range. The high impedance IADJ input simplifies LED current binning and thermal protection.

The TPS92692 and TPS92692-Q1 devices incorporate an internal PWM generator that can be programmed to implement pulse width modulation (PWM) dimming of LED current. The PWM duty cycle can be varied from 0% to 100% by modulating the analog voltage on DIM/PWM input from 1 V to 3 V. The PWM dimming frequency is externally programmable and is set by the capacitor connected to RAMP input. As an alternative, the TPS92692 and TPS92692-Q1 devices can also be configured to implement direct PWM dimming based on the duty cycle of external PWM signal by connecting a 249-kΩ resistor across RAMP pin and GND. The internal PWM signal controls the GATE and PDRV outputs which control the external n-channel switching FET and p-channel dimming FET connected in series with LED string, respectively.

The current monitor output, IMON, reports the instantaneous status of LED current measured by the rail-to-rail current sense amplifier. This feature indicates instantaneous current as a result of LED short circuit and cable harness failure, independent of LED driver topology. An open-drain fault indicator is also provided to report faults including cycle-by-cycle current limit, output overvoltage, and output undervoltage conditions. LED driver protection with auto-restart (hiccup) mode is enabled by connecting the fault pin ($\overline{\text{FLT}}$) to the SS pin. Other protection features include VCC undervoltage protection and thermal shutdown. A remote signal can force the device in to shutdown by pulling down on the SS pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Internal Regulator and Undervoltage Lockout (UVLO)

The device incorporates a 65-V input voltage rated linear regulators to generate the 7.5 V (typ) V_{CC} bias supply, the 5 V (typ) V_{REF} reference supply and other internal reference voltages. The device monitors the V_{CC} output to implement UVLO protection. Operation is enabled when V_{CC} exceeds the 4.5-V (typ) threshold and is disabled when V_{CC} drops below the 4.1-V (typ) threshold. The UVLO comparator provides 400 mV of hysteresis to avoid chatter during transitions. The UVLO thresholds are internally fixed and cannot be adjusted. An internal current limit circuit is implemented to protect the device during VCC pin short-circuit conditions. The V_{CC} supply powers the internal circuitry and the N-channel gate driver output, GATE. Place a bypass capacitor in the range of 2.2 µF to 4.7 µF across the V_{CC} output and GND to ensure proper operation. The regulator operates in dropout when input voltage V_{IN} falls below 7.5 V forcing V_{CC} to be lower than V_{IN} by 300 mV for a 20-mA supply current. The V_{CC} is a regulated output of the internal regulator and is not recommended to be driven from an external power supply.

The V_{REF} supply is internally used to generate voltage thresholds for the RAMP generator circuit and to power some digital circuits. This supply can be used in conjunction with a resistor divider to set voltage levels for the IADJ pin and DIM/PWM pin to set LED current and PWM dimming duty cycle. It can also be used to bias external circuitry requiring a reference supply. The supply current is internally limited to protect the device from output overload and short-circuit conditions. Place a bypass capacitor in the range of 2.2 µF to 4.7 µF across the VREF output to GND to ensure proper operation.

The TPS92692 and TPS92692-Q1 devices incorporate features that simplify compliance with the CISPR and automotive EMI requirements. The devices have optional spread spectrum frequency modulation circuit that can be externally configured to reduce peak and average conducted and radiated EMI. The internal programmable oscillator has a range of 80 kHz to 800 kHz and can be tuned based on the EMI requirements. The devices are available in HTSSOP-20 package with an exposed pad to aid in thermal dissipation.

8.3.2 Oscillator

The switching frequency is programmable by a single external resistor connected between the RT pin and GND. To set a desired frequency, f_{SW} (Hz), the resistor value can be calculated from Equation 1.

$$R_T \quad \frac{1.432 \times 10^{10}}{(f_{SW})^{1.047}} \ (\Omega) \tag{1}$$

Figure 6 shows a graph of switching frequency versus resistance, R_T. TI recommends a switching frequency setting between 80 kHz and 700 kHz for optimal performance over input and output voltage operating range and for best efficiency. Operation at higher switching frequencies requires careful selection of N-channel MOSFET characteristics as well as detailed analysis of switching losses.

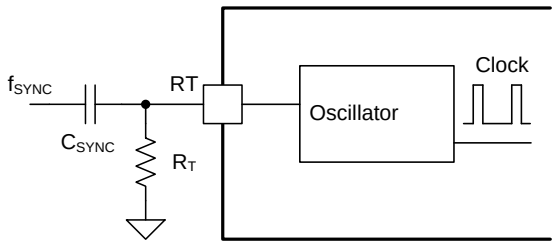


Figure 21. Oscillator Synchronization Through AC Coupling

The internal oscillator can be synchronized by AC coupling an external clock pulse to RT pin as shown in Figure 21. The positive going synchronization clock at the RT pin must exceed the RT sync threshold and the negative going synchronization clock at the RT pin must exceed the RT sync falling threshold to trip the internal synchronization pulse detector. TI recommends that the frequency of the external synchronization pulse is within ±20% of the internal oscillator frequency programmed by the R_T resistor. TI recommends a minimum coupling capacitor of 100 nF and a typical pulse width of 100 ns for proper synchronization. In the case where external synchronization clock is lost the internal oscillator takes control of the switching rate based on the R_T resistor to maintain output current regulation. The R_T resistor is always required whether the oscillator is free running or externally synchronized.

Feature Description (continued)

8.3.3 Spread Spectrum Frequency Modulation

The TPS92692 and TPS92692-Q1 devices provide a frequency dithering option that is enabled by connecting a capacitor from the DM pin to GND. A triangle waveform centered at 1 V is generated across the C_{DM} capacitor. The triangle waveform modulates the oscillator frequency by ± 15% of the nominal frequency set by an external timing resistor, R_T. The C_{DM} capacitance value sets the rate of the low frequency modulation. To achieve maximum attenuation in average EMI scan set modulation frequency ranging from 100 Hz to 1.2 kHz. The low modulating frequency has little impact on the quasi-peak EMI scan. Set the modulation frequency to 10 KHz or higher to achieve attenuation for quasi-peak EMI measurements. The modulation frequency higher than the receiver resolution bandwidth (RBW) of 9 kHz only impacts the quasi-peak EMI scan and has little impact on the average measurement. The device simplifies EMI compliance by providing the means to tune the modulation frequency based on measured EMI signature. Equation 2 calculates the C_{DM} capacitance required to set the modulation frequency, f_{MOD} (Hz).

$$C_{DM} \quad \frac{10\ \mu A}{2 \times f_{MOD} \times 0.3\ V}\ (F) \tag{2}$$

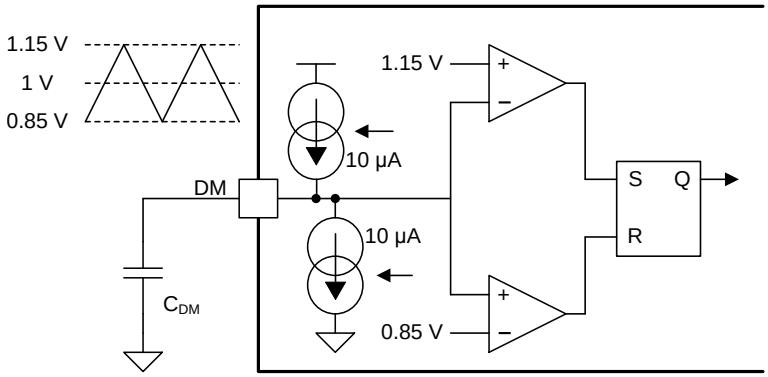


Figure 22. Frequency Dither Operation

Connect the DM pin to GND to disable frequency dither circuit operation. Internal frequency dithering is not supported when the devices are synchronized based on an external clock signal.

8.3.4 Gate Driver

The TPS92692 and TPS92692-Q1 devices contain a N-channel gate driver that switches the output V_{GATE} between V_{CC} and GND. A peak source and sink current of 500 mA allows controlled slew-rate of the MOSFET gate and drain node voltages, limiting the conducted and radiated EMI generated by switching.

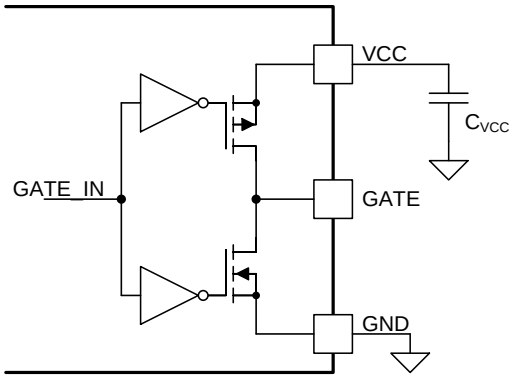


Figure 23. Push-Pull N-Channel Gate Driver Circuit

Feature Description (continued)

The gate driver supply current $I_{CC(GATE)}$ depends on the total gate drive charge (Q_G) of the MOSFET and the operating frequency of the converter, f_{SW}, $I_{CC(GATE)} = Q_G \times f_{SW}$. Choose a MOSFET with a low gate charge specification to limit the junction temperature rise and switch transition losses.

It is important to consider the MOSFET threshold voltage when operating in the dropout region when the input voltage, V_{IN}, is below the V_{CC} regulation level. TI recommends a logic level device with a threshold voltage below 5 V when the device is required to operate at an input voltage less than 7 V.

8.3.5 Rail-to-Rail Current Sense Amplifier

The internal rail-to-rail current sense amplifier measures the average LED current based on the differential voltage drop between the CSP and CSN inputs over a common mode range of 0 V to 65 V. The differential voltage, $V_{(CSP-CSN)}$, is amplified by a voltage-gain factor of 14 and is connected to the negative input of the transconductance error amplifier. Accurate LED current feedback is achieved by limiting the cumulative input offset voltage, (represented by the sum of the voltage-gain error, the intrinsic current sense offset voltage, and the transconductance error amplifier offset voltage) to less than 5 mV over the recommended common-mode voltage, and temperature range.

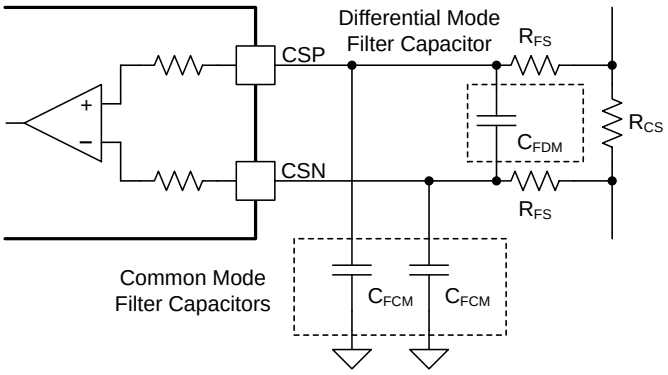


Figure 24. Current Sense Amplifier Input Filter Options

An optional common-mode or differential mode low-pass filter implementation, as shown in Figure 24, can be used to smooth out the effects of large output current ripple and switching current spikes caused by diode reverse recovery. TI recommends a filter resistance in the range of 10 Ω to 100 Ω to limit the additional offset caused by amplifier bias current mismatch to achieve the best accuracy and line regulation.

8.3.6 Transconductance Error Amplifier

The internal transconductance amplifier generates an error signal proportional to the difference between the LED current sense feedback voltage and the external IADJ input voltage. The output of the error amplifier is connected to an external compensation network to achieve closed-loop LED current regulation. In most LED driver applications a simple integral compensation circuit consisting of a capacitor connected from COMP output to GND provides a stable response over wide range of operating conditions. TI recommends a capacitor value between 10 nF and 100 nF as a good starting point. To achieve higher closed-loop bandwidth a proportional-integral compensator, consisting of a series resistor and a capacitor network connected across the COMP output and GND, is required. Based on the converter topology, tune the compensation network to achieve a minimum of 60° of phase margin and 10 dB of gain margin. The *Application and Implementation* section includes a summarized detailed design procedure.

Feature Description (continued)

8.3.7 Switch Current Sense

The IS input pin monitors the main MOSFET current to implement peak current mode control. The GATE output duty cycle is derived by comparing the peak switch current, measured by the R_{IS} resistor, to the internal COMP voltage threshold. An internal slope signal, V_{SL}, generated by slope compensation circuit is added to the measured sense voltage, V_{IS}, to prevent subharmonic oscillations for duty cycles greater than 50%. An internal blanking circuit prevents MOSFET switching current spike propagation and premature termination of duty cycle by internally shunting the IS input for 150 ns after the beginning of the new switching period. For additional noise suppression connect an external low-pass RC filter with resistor values ranging from 100 Ω to 500 Ω and a 1000 pF capacitor. The external RC filter ensures proper operation when operating in the dropout region (V_{IN} less than 7 V).

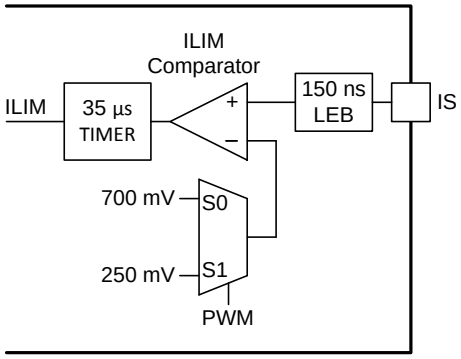


Figure 25. Switch Current Limit Circuit

Cycle-by-cycle current limit is accomplished by a redundant internal comparator. The current limit threshold is set based on the status of internal PWM signal. The current limit threshold is set to 250 mV (typ) when PWM signal is high and to 700 mV (typ) when PWM signal is low. The transition between the two thresholds work in conjunction with slope compensation and the error amplifier circuit to allow for higher inductor current immediately after the PWM transition and to improve LED current transient response during PWM dimming. Refer to the *DIM/PWM Input* section for details on PWM Dimming operation.

The device immediately terminates the GATE and PDRV output when the IS input voltage, V_{IS}, exceeds the threshold value. Upon a current limit event, the SS and COMP pin are internally grounded to reset the state of the controller. The GATE output is enabled after the expiration of the 35-µs internal fault timer and a new start-up sequence is initiated through the SS pin. Equation 3 calculates the peak inductor current in the current limit.

$$I_{L(PK)} = \frac{250mV}{R_{IS}} \text{ (A)} \tag{3}$$

8.3.8 Slope Compensation

Peak current mode based regulators are subject to sub-harmonic oscillations for duty cycle greater than 50%. To avoid this instability problem, the control scheme is modified by the addition of an artificial ramp to the sensed switch current waveform. The slope of the artificial ramp required is dependent on the input voltage, V_{IN}, output voltage, V_O, inductor, L, and switch current sense resistor, R_{IS}. The devices incorporate an adaptive slope compensation technique that modifies the slope of the artificial ramp generated based on the input voltage, V_{IN} and output voltage measured at CSP pin, V_{CSP}, thus greatly simplifying the design for common LED driver topologies, such as boost, buck-boost, and boost-to-battery. The magnitude of the internal ramp signal can be calculated as follows:

$$V_{SL} \quad 278 \times 10^6 \times D \times \frac{\left(0.494 \times \left(V_{CSP} - V_O\right) + 1\right)}{f_{SW} \times R_{SLP}} \tag{4}$$

where

- D is the converter duty cycle

Feature Description (continued)

The resistor, R_{SLOPE} provides the flexibility to set the slope of the internal artificial ramp based on the inductance value, L and the LED driver topology. The *Application and Implementation* section includes detailed calculations for the resistor, R_{SLOPE}, based on the LED driver topology. The SLOPE pin cannot be left floating.

8.3.9 Analog Adjust Input

The voltage across the LED current sense resistor, $V_{(CSP–CSN)}$, is regulated to the analog adjust input voltage, V_{IADJ}, scaled by the current sense amplifier voltage gain of 14. The LED current can be linearly adjusted by varying the voltage on IADJ pin from 140 mV to 2.25 V using either a resistor divider from V_{REF} or a voltage source. The IADJ pin can be connected to V_{REF} through an external resistor to set LED current based on the 2.4-V internal reference voltage. This device offers different methods to set the IADJ voltage. Figure 27 shows how the IADJ input can be used in conjunction with a NTC resistor to implement thermal foldback protection. A PWM signal in conjunction with first- or second-order low-pass filter can be used to program the IADJ voltage as shown in Figure 28).

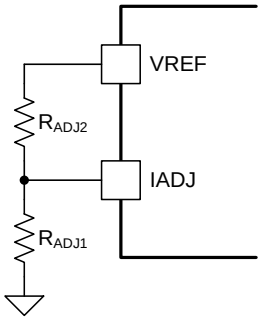


Figure 26. Static Reference Setting Resistor Divider From VCC

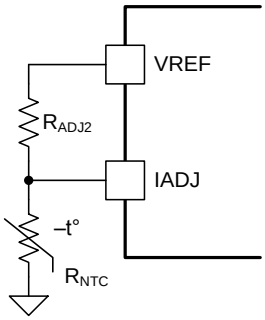


Figure 27. Thermal Fold-back Circuit Using External NTC Resistor

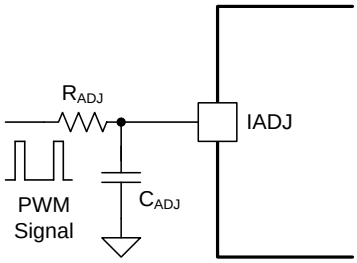


Figure 28. Analog Dimming Achieved By Low-pass Filtering External PWM Signal

8.3.10 DIM/PWM Input

The TPS92692 and TPS92692-Q1 devices incorporate a PWM generator circuit to facilitate analog voltage to PWM duty cycle translation. The dimming frequency is set by connecting a capacitor from RAMP pin to GND. The dimming frequency, f_{DIM}, can be calculated as follows:

$$f_{DIM} \quad \frac{10\ \mu A}{2 \times 2\ V \times C_{DIM}}\ (Hz) \tag{5}$$

The internal PWM signal can be varied from 0% to 100% by setting the DIM/PWM pin voltage between 1 V and 3 V. Equation 6 describes the relationship between DIM/PWM pin voltage, V_{DIM} and internal PWM duty cycle, $D_{PWM(INT)}$.

$$D_{PWM(INT)} \quad \frac{V_{DIM} - 1}{2} \tag{6}$$

For improved dimming accuracy, use the VREF pin and a resistor divider to set the DIM/PWM pin voltage, V_{DIM}, and the corresponding duty cycle. The device can be configured to step the duty cycle between 100% and the programmed value by diode connecting the external control signal, V_{CTRL}, to the DIM/PWM pin, as shown in Figure 29. The external control signal, of amplitude 3-V, is usually generated by the command module and is based on the light output required by the application.

Feature Description (continued)

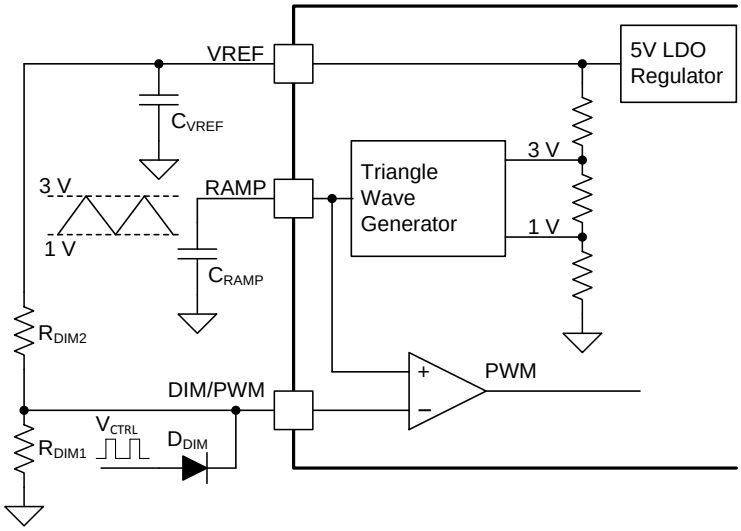


Figure 29. PWM Dimming Using Internal PWM Generator

The devices can be configured to be compatible with external PWM signal, $V_{PWM(EXT)}$, where the LED current is modulated based on the duty cycle, $D_{PWM(EXT)}$. To enable direct PWM, it is required to disable the internal triangle wave generator by connecting a 249-kΩ resistor from RAMP pin to GND. In this case, the internal comparator threshold is set to 2.49-V and the internal PWM duty cycle, $D_{PWM(INT)}$, is controlled by the external PWM command. The RAMP pin cannot be left floating.

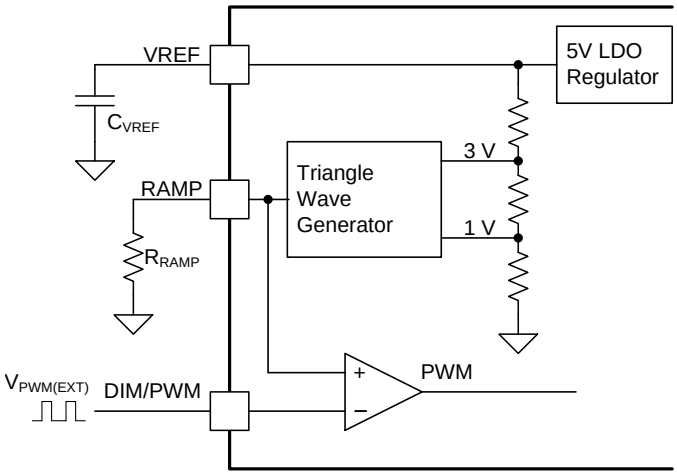


Figure 30. Direct PWM Dimming

The internal PWM signal, V_{PWM} controls the GATE and PDRV outputs. Forcing V_{PWM} in a logic low state turns off switching, parks the oscillator, disconnects the COMP pin, and sets the PDRV output to V_{CSP} in order to maintain the charge on the compensation network and output capacitors. On the rising edge of the PWM voltage (V_{PWM} set to logic level high), the GATE and PDRV outputs are enabled to ramp the inductor current to the previous steady-state value. The COMP pin is connected and the error amplifier and oscillator are enabled only when the switch current sense voltage V_{IS} exceeds the COMP voltage, V_{COMP}, thus immediately forcing the converter into steady-state operation with minimum LED current overshoot. When dimming is not required, connect the DIM/PWM pin to the V_{CC} pin. An internal pull-down resistor sets the input to logic-low and disables the device when the pin is disconnected or left floating.

Feature Description (continued)

8.3.11 Series P-Channel FET Dimming Gate Driver Output

The PDRV output is a function of the internal PWM signal and is capable of sinking and sourcing up to 50 mA of peak current to control a high-side series connected P-channel dimming FET. The PDRV switches between V_{CSP} and (V_{CSP}– 7 V) based on the status of PWM signal to completely turn-off and turn-on the external P-channel dimming FET. The series dimming FET is required to achieve high contrast ratio as it ensures fast rise and fall times of the LED current in response to the PWM input. Without any dimming FET, the rise and fall times are limited by the inductor slew rate and the closed-loop bandwidth of the system. Leave the PDRV pin unconnected if not used.

8.3.12 Soft-Start

The soft-start feature helps the regulator gradually reach the steady-state operating point, thus reducing startup stresses and surges. The devices clamp the COMP pin to the SS pin, separated by a diode, until LED current nears the regulation threshold. The internal 10-µA soft-start current source gradually increases the voltage on an external soft-start capacitor C_{SS} connected to the SS pin. This results in a gradual rise of the COMP voltage from GND.

The internal 10-µA current source turns on when VCC exceeds the UVLO threshold. At the beginning of the soft-start sequence, the SS pull-down switch is active and is released when the voltage V_{SS} drops below 50 mV. The SS pin can also be pulled down by an external switch to stop switching. When the SS pin is externally driven to enable switching, the slew-rate on the COMP pin is controlled by the compensation capacitor. In this case, the startup duration and LED current transient is controlled by tunning the compensation network. It is essential to ensure that the softstart duration is longer than the time required to charge the output capacitor when selecting the soft-start capacitor, C_{SS} and the compensation capacitor, C_{COMP}.

8.3.13 Current Monitor Output

The IMON pin voltage represents the LED current measured by the rail-to-rail current sense amplifier across the external current shunt resistor. The linear relationship between the IMON voltage and LED current includes the amplifier gain-factor of 14 (see *Feature Description* section). The IMON output can be connected to an external microcontroller or comparator to facilitate LED open, short, or cable harness fault detection and mitigation. The IMON voltage is internally clamped to 3.7 V.

8.3.14 Output Overvoltage Protection

The TPS92692 and TPS92692-Q1 devices include a dedicated OV pin which can be used for either input or output overvoltage protection. This pin features a precision 1.228 V (typ) threshold with 20-µA (typ) of hysteresis current. The overvoltage threshold limit is set by a resistor divider network from the input or output terminal to GND. When the OV pin voltage exceeds the reference threshold, the GATE pin is immediately pulled low, the PDRV output is disabled, and the SS and COMP capacitors are discharged. The GATE and PDRV outputs are enabled and a new startup sequence is initiated after the voltage drops below the hysteresis threshold set by the 20-µA source current and the external resistor divider.

8.3.15 Output Short-circuit Protection

The device monitors the output of the current sense amplifier and the output voltage via OV pin to determine LED Short-circuit fault. The device signals an output overcurrent fault when the voltage across the current sense amplifier, ($V_{(CSP-CSN)}$), exceeds the regulation set point based on the IADJ pin voltage, V_{IADJ}. The overcurrent fault threshold is calculated as follows:

$$V_{((CSP-CSN),OCP)} \quad 1.5 \times \frac{V_{IADJ}}{14} \tag{7}$$

The device also indicates a short-circuit condition when the voltage across the OV pin and GND falls below 100 mV. In this case, the output voltage, V_O, is below the undervoltage fault threshold determined based on the resistor divider connected to the OV pin.

$$V_{O(UV)} \quad 0.1 \times \frac{R_{OV1} + R_{OV2}}{R_{OV1}} \tag{8}$$

Feature Description (continued)

The devices indicate a fault by forcing the open-drain fault indicator $\overline{FLT}$ pin to GND and initiating a 36-ms timer. The devices do not internally initiate any protection action and continue to operate until externally disabled by pulling SS pin to GND. This provides maximum design flexibility to enable user defined fault protection by using either the fault indicator output, $\overline{FLT}$, or the analog IMON output based on the LED driver topology and end application.

The undervoltage fault detection circuit is internally disable based on the SS pin voltage and internal PWM status. The fault blanking circuit is designed to prevent false undervoltage detection during the startup sequence and PWM dimming operation.

8.3.16 Thermal Protection

Internal thermal shutdown circuitry is implemented to protect the controller in the event the maximum junction temperature is exceeded. When activated, typically at 175°C, the controller is forced into a shutdown mode, disabling the internal regulator. This feature is designed to prevent overheating and damage to the device.

8.3.17 Fault Indicator ($\overline{FLT}$)

The devices include an open-drain output to indicate fault conditions. The $\overline{FLT}$ pin goes low under the following conditions:

- Overvoltage across the LED string (V_{OV}> 1.24 V)
- Under voltage across the LED string (V_{OV}< 100 mV)
- Overcurrent across the LED string ($14 \times V_{(CSP-CSN)} > 1.5 \times V_{IADJ}$)
- Cycle-by-cycle switch current limit condition (V_{IS} > 250 mV)

The $\overline{FLT}$ pin goes high when the fault conditions ends or when the internal 36-ms timer expires. The status of the $\overline{FLT}$ under different fault conditions is summarized in the *Device Functional Modes* section.

8.4 Device Functional Modes

The following table summarizes the device behavior under fault condition.

Table 1. Fault Descriptions

FAULT	DETECTION	ACTION
Input undervoltage (UVLO)	$V_{CC(RISE)}$ < 4.5 V $V_{CC(FALL)}$ < 4.1 V	The device enters the standby state when the VCC voltage falls below the UVLO threshold. In standby state, GATE and PDRV outputs are disabled and the SS and COMP capacitors are discharged. $\overline{FLT}$ pin remains in high-impedance state.
Switch current limit	V_{IS} > 250 mV	Cycle-by-cycle current limit is activated when the IS pin voltage exceeds 250 mV. The GATE and PDRV outputs are disabled, the SS and COMP pin capacitors are discharged and $\overline{FLT}$ pin is forced to ground. An internal 35-µs timer is activated. Soft-start sequence is initiated after expiration of the 35 µs timer period.
Thermal protection	T_J > 175°C	Internal thermal shutdown circuitry is activated when the junction temperature exceeds 175 °C. The controller is forced into a shutdown mode, disabling the internal regulators. A startup sequence is initiated when the junction temperature falls below 155˚C. The $\overline{FLT}$ pin remains in a high-impedance state.
Programmable output overvoltage protection	V_{OV} > 1.228 V	When the OV pin voltage exceeds 1.228 V, GATE and PDRV outputs are disabled, SS and COMP capacitors are discharged, and the $\overline{FLT}$ pin is forced to GND. A soft-start sequence is initiated once the output voltage drops below the hysteresis threshold set by the 20 µA current source.
Fixed LED Overcurrent protection	$V_{(CSP-CSN)} > V_{((CSP-CSN),OCP)}$	The $\overline{FLT}$ pin is forced to ground for 36-ms when the LED current exceeds 1.5 times the regulation set point. The $\overline{FLT}$ pin is released after timer expires. Under sustained short-circuit condition, the $\overline{FLT}$ pin transitions between a high-impedance state and ground until the fault is cleared. Device continues to operate while in this condition.
Output undervoltage protection	V_{OV} < 100 mV	The $\overline{FLT}$ pin is forced to ground for 36-ms when OV pin voltage drops below 100 mV. The $\overline{FLT}$ pin is released after timer expires. Under sustained short-circuit condition, the $\overline{FLT}$ pin transitions between the high-impedance state and ground until fault is cleared. Device continues to operate while in this condition.
Programmable LED overcurrent protection	$V_{IMON} > V_{IADJ}$	Current monitor output (IMON) can be used to externally program current limit. The IMON output can be connected to an external microcontroller or comparator to facilitate LED open, short, or cable harness fault detection.

Device Functional Modes (continued)

Table 1. Fault Descriptions (continued)

FAULT	DETECTION	ACTION
COMP pin short to ground	V_{COMP} < 1.6 V	Switching is disabled when COMP voltage falls below 1.6 V. The $\overline{FLT}$ pin remains a in high-impedance state.
VREF pin short to ground	V_{REF} < 2.0 V	The device enters standby when the VCC voltage falls below the UVLO threshold. In the standby state, GATE and PDRV outputs are disabled and the SS and COMP capacitors are discharged. The $\overline{FLT}$ pin will remain in a high-impedance state.

8.4.1 Hiccup Mode Short-circuit Protection

Connecting the $\overline{FLT}$ pin to the SS pin enables hiccup mode operation under output short-circuit conditions.

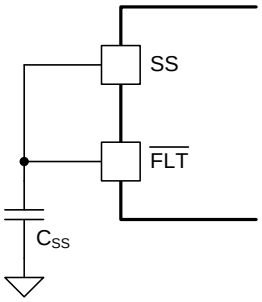


Figure 31. Hiccup Mode Short-Circuit Protection

On detection of output short-circuit fault, the $\overline{FLT}$ pin forces the SS pin to GND (V_{SS} < 50 mV) and disables GATE and PDRV outputs for 36-ms. Upon timer expiration, the $\overline{FLT}$ pin is released and a new soft start sequence is initiated. Under sustained fault conditions the device operates in hiccup mode, attempting to recover after every 36-ms period.

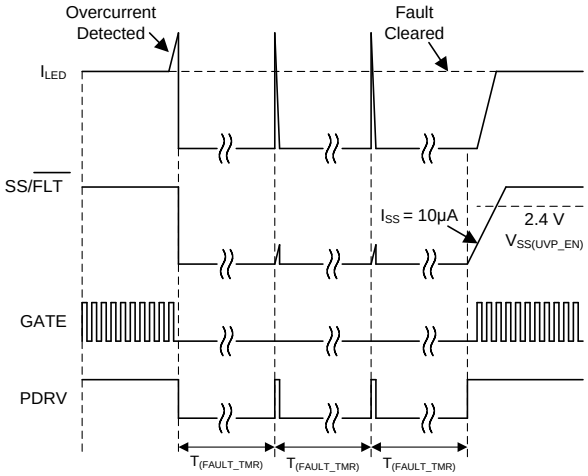


Figure 32. Output Overcurrent Fault Protection

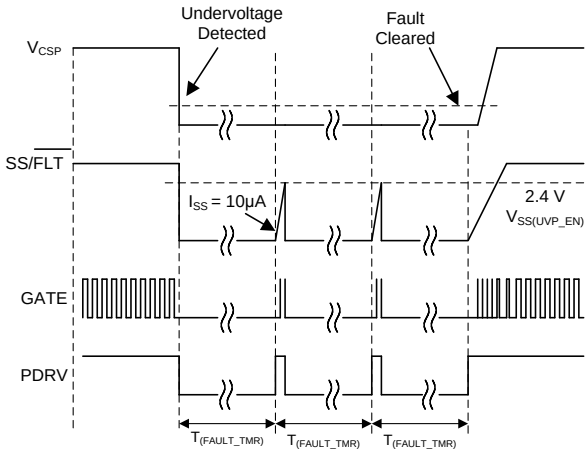


Figure 33. Output Undervoltage Fault Protection

8.4.2 Fault Indication Mode

The $\overline{FLT}$ pin output can be setup to indicate fault status to a microcontroller and aid in fault diagnostics and protection. In case of a fault, the $\overline{FLT}$ pin is forced low when biased through an external resistor connected either to reference voltage output, VREF, or an external bias supply. When connected to VREF, the $\overline{FLT}$ pin is driven low when the device enters standby mode during UVLO, thermal shutdown, or VREF short-circuit conditions. The *Fault Indicator ($\overline{FLT}$)* section lists fault diagnostics and system level faults.

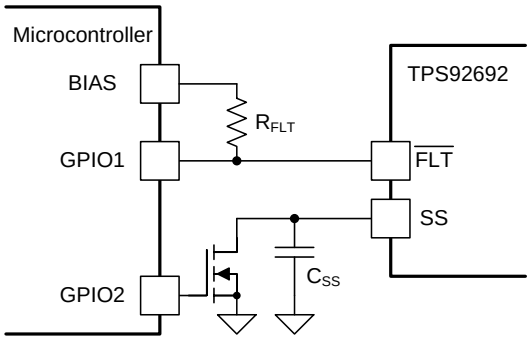


Figure 34. $\overline{FLT}$ Pin Interface With Microcontroller

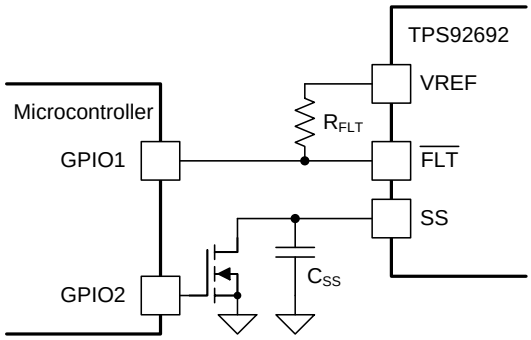


Figure 35. $\overline{FLT}$ Pin Interface With Microcontroller

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS92692 and TPS92692-Q1 controllers are suitable for implementing step-up or step-down LED driver topologies including boost, buck-boost, SEPIC, and flyback. Use the following design procedure to select component values for the TPS92692-Q1 device. This section presents a simplified discussion of the design process for the boost and buck-boost converter. The expressions derived for the buck-boost topology can be altered to select components for a 1:1 coupled-inductor SEPIC converter. The design procedure can be easily adapted for flyback and similar converter topologies.

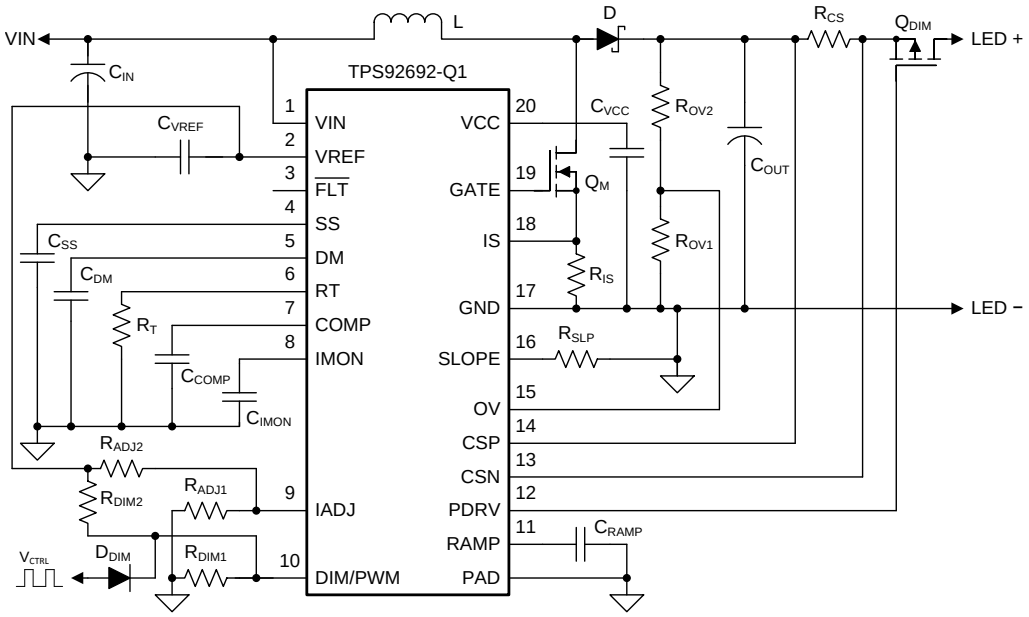


Figure 36. Boost LED Driver

Application Information (continued)

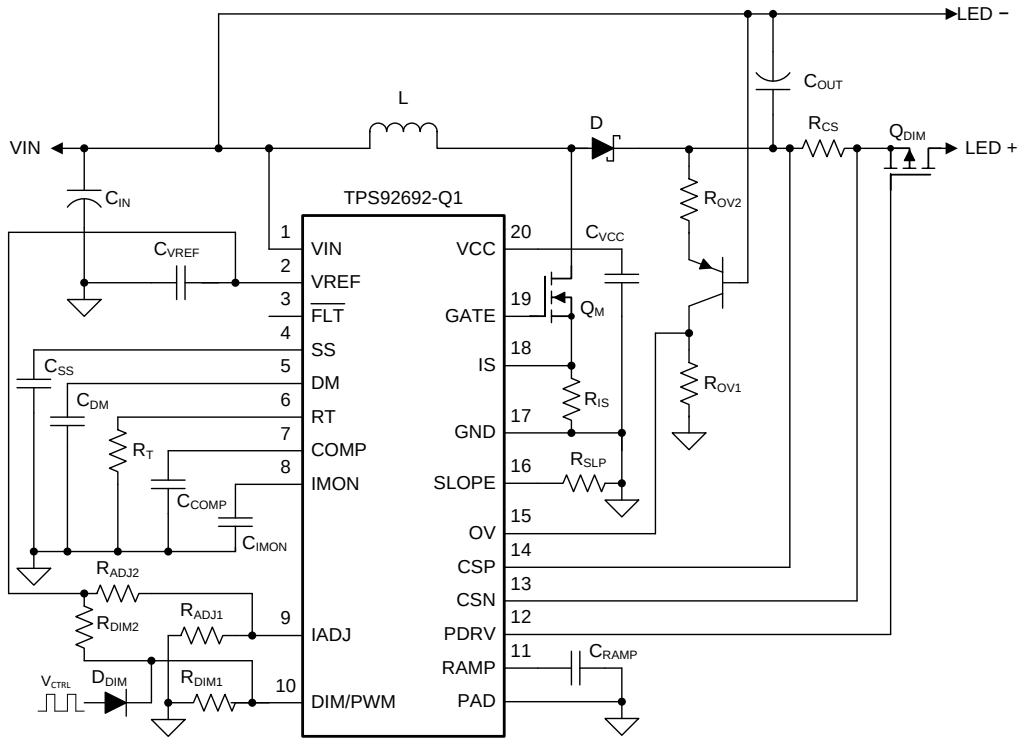


Figure 37. Buck-Boost LED Driver

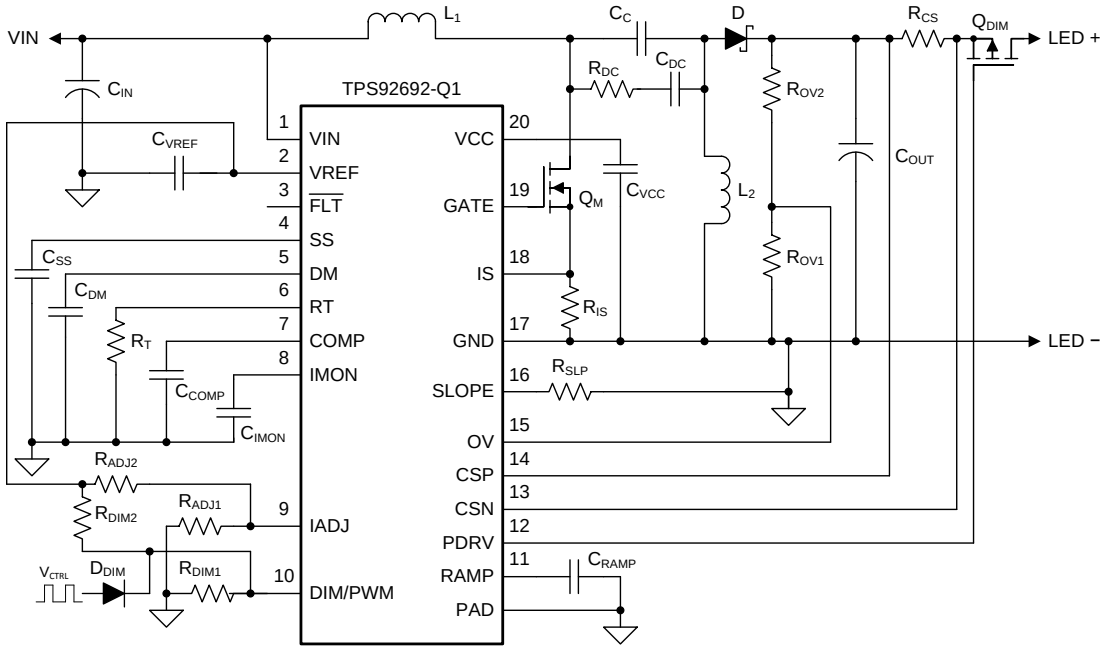


Figure 38. SEPIC LED Driver

Application Information (continued)

9.1.1 Duty Cycle Considerations

The switch duty cycle, D, defines the converter operation and is a function of the input and output voltages. In steady state, the duty cycle is derived using expression:

Boost:

$$D \quad \frac{V_O - V_{IN}}{V_O} \tag{9}$$

Buck-Boost:

$$D \quad \frac{V_O}{V_{IN} + V_O} \tag{10}$$

The minimum duty cycle, D_{MIN}, and maximum duty cycle, D_{MAX}, are calculated by substituting maximum input voltage, $V_{IN(MAX)}$, and the minimum input voltage, $V_{IN(MIN)}$, respectively in the previous expressions. The minimum duty cycle achievable by the device is determined by the leading edge blanking period and the switching frequency. The maximum duty cycle is limited by the internal oscillator to 90% (typ) to allow for minimum off-time. It is necessary for the operating duty cycle to be within the operating limits of the device to ensure closed-loop LED current regulation over the specified input and output voltage range.

9.1.2 Inductor Selection

The choice of inductor sets the continuous conduction mode (CCM) and discontinuous conduction mode (DCM) boundary condition. Therefore, one approach of selecting the inductor value is by deriving the relationship between the output power corresponding to CCM-DCM boundary condition, $P_{O(BDRY)}$ and inductance, L. This approach ensures CCM operation in battery-powered LED driver applications that are required to support different LED string configurations with a wide range of programmable LED current set points. The CCM-DCM boundary condition can be estimated either based on the lowest LED current and the lowest output voltage requirements for a given application or as a fraction of maximum output power, $P_{O(MAX)}$.

$$P_{O(BDRY)} \leq I_{LED(MIN)} \times V_{O(MIN)} \tag{11}$$

$$\frac{P_{O(MAX)}}{4} \leq P_{O(BDRY)} \leq \frac{P_{O(MAX)}}{2} \tag{12}$$

Boost:

$$L \quad \frac{V_{IN(MAX)}^2}{2 \times P_{O(BDRY)} \times f_{SW}} \times \left(1 - \frac{V_{IN(MAX)}}{V_{O(MAX)}}\right) \tag{13}$$

Buck-Boost:

$$L \quad \frac{1}{2 \times P_{O(BDRY)} \times f_{SW} \times \left(\frac{1}{V_{O(MAX)}} + \frac{1}{V_{IN(MAX)}}\right)^2} \tag{14}$$

Select inductor with saturation current rating greater than the peak inductor current, $I_{L(PK)}$, at the maximum operating temperature.

Boost:

$$i_{L(PK)} \quad \frac{P_{O(MAX)}}{V_{IN(MIN)}} + \frac{V_{IN(MIN)}}{2 \times L \times f_{SW} \times V_{O(MAX)}} \times \left(1 - \frac{V_{IN(MIN)}}{V_{O(MAX)}}\right) \tag{15}$$

Buck-Boost:

$$I_{L(PK)} \quad P_{O(MAX)} \times \left(\frac{1}{V_{O(MIN)}} + \frac{1}{V_{IN(MIN)}}\right) + \frac{V_{O(MIN)} \times V_{IN(MIN)}}{2 \times L \times f_{SW} \times \left(V_{O(MIN)} + V_{IN(MIN)}\right)} \tag{16}$$

Application Information (continued)

9.1.3 Output Capacitor Selection

The output capacitors are required to attenuate the discontinuous or large ripple current generated by switching and achieve the desired peak-to-peak LED current ripple, $\Delta i_{LED(PP)}$. The capacitor value depends on the total series resistance of the LED string, r_D and the switching frequency, f_{SW}.The capacitance required for the target LED ripple current can be calculated based on following equations.

Boost:

$$C_{OUT} \quad \frac{P_{O(MAX)}}{\Delta i_{LED(PP)} \times r_{D(MIN)} \times f_{SW} \times V_{O(MAX)}} \times \left(1 - \frac{V_{IN(MIN)}}{V_{O(MAX)}}\right) \tag{17}$$

Buck-Boost:

$$C_{OUT} \quad \frac{P_{O(MAX)}}{\Delta i_{LED(PP)} \times f_{SW} \times r_{D(MIN)} \times \left(V_{O(MIN)} + V_{IN(MIN)}\right)} \tag{18}$$

When choosing the output capacitors, it is important to consider the ESR and the ESL characteristics as they directly impact the LED current ripple. Ceramic capacitors are the best choice due to their low ESR, high ripple current rating, long lifetime, and good temperature performance. When selecting ceramic capacitors, it is important to consider the derating factors associated with higher temperature and DC bias operating conditions. TI recommends an X7R dielectric with voltage rating greater than maximum LED stack voltage. An aluminum electrolytic capacitor can be used in parallel with ceramic capacitors to provide bulk energy storage. The aluminum capacitors must have necessary RMS current and temperature ratings to ensure prolonged operating lifetime. The minimum allowable RMS output capacitor current rating, $I_{COUT(RMS)}$, can be approximated:

Boost and Buck-Boost:

$$I_{COUT(RMS)} \quad I_{LED} \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}} \tag{19}$$

9.1.4 Input Capacitor Selection

The input capacitors, C_{IN}, smooth the input voltage ripple and store energy to supply input current during input voltage or PWM dimming transients. The series inductor in the Boost and SEPIC topologies provides continuous input current and requires a smaller input capacitor to achieve desired input ripple voltage, $\Delta v_{IN(PP)}$. The Buck-Boost and Flyback topologies have discontinuous input current and require a larger capacitor to achieve the same input voltage ripple. Based on the switching frequency, f_{SW}, and the maximum duty cycle, D_{MAX}, the input capacitor value can be calculated as follows:

Boost:

$$C_{IN} \quad \frac{V_{IN(MIN)}}{8 \times L \times f_{SW}^2 \times \Delta v_{IN(PP)}} \times \left(1 - \frac{V_{IN(MIN)}}{V_{O(MAX)}}\right) \tag{20}$$

Buck-Boost:

$$C_{IN} \quad \frac{P_{O(MAX)}}{f_{SW} \times \Delta v_{IN(PP)} \times \left(V_{O(MIN)} + V_{IN(MIN)}\right)} \tag{21}$$

X7R dielectric-based ceramic capacitors are the best choice due to their low ESR, high ripple current rating, and good temperature performance. For applications using PWM dimming, TI recommends an aluminum electrolytic capacitor in addition to ceramic capacitors to minimize the voltage deviation due to large input current transients generated in conjunction with the rising and falling edges of the LED current.

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Application Information (continued)

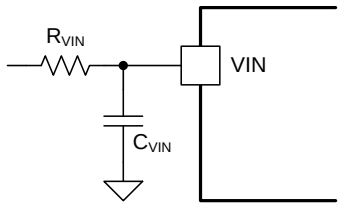


Figure 39. VIN Filter

Decouple VIN pin with a 0.1-µF ceramic capacitor, placed as close as possible to the device and a series 10-Ω resistor to create a 150-kHz low-pass filter.

9.1.5 Main Power MOSFET Selection

The power MOSFET is required to sustain the maximum switch node voltage, V_{SW}, and switch RMS current derived based on the converter topology. TI recommends a drain voltage V_{DS} rating of at least 10% greater than the maximum switch node voltage to ensure safe operation. The MOSFET drain-to-source breakdown voltage, V_{DS}, is calculated using the following expressions.

Boost:

$$V_{DS} = 1.1 \times V_{O(OV)} \tag{22}$$

Buck-Boost:

$$V_{DS} = 1.1 \times \left(V_{O(OV)} + V_{IN(MAX)} \right) \tag{23}$$

The voltage, $V_{O(OV)}$, is the overvoltage protection threshold and the worst-case output voltage under fault conditions. The worst case MOSFET RMS current for Boost and Buck-Boost topology is dependent on maximum output power, $P_{O(MAX)}$, and is calculated as follows:

$$I_{Q(RMS)} \quad \frac{P_{O(MAX)}}{V_{IN(MIN)}} \times \sqrt{\left(1 + \frac{V_{IN(MIN)}}{V_{O(MIN)}} \right)} \tag{24}$$

Select a MOSFET with low total gate charge, Q_g, to minimize gate drive and switching losses. The MOSFET R_{DS} resistance is usually a less critical parameter because the switch conduction losses are not a significant part of the total converter losses at high operating frequencies. The switching and conduction losses are calculated as follows:

$$P_{COND} = R_{DS} \times I^2_{Q(RMS)} \tag{25}$$

$$P_{SW} \quad \frac{I_L \times V^2_{SW} \times C_{RSS} \times f_{SW}}{I_{GATE}} \tag{26}$$

C_{RSS} is the MOSFET reverse transfer capacitance. I_L is the average inductor current. I_{GATE} is gate drive output current, typically 500 mA. The MOSFET power rating and package is selected based on the total calculated loss, the ambient operating temperature, and maximum allowable temperature rise.

9.1.6 Rectifier Diode Selection

A Schottky diode (when used as a rectifier) provides the best efficiency due to its low forward voltage drop and near-zero reverse recovery time. TI recommends a diode with a reverse breakdown voltage, $V_{D(BR)}$, greater than or equal to MOSFET drain-to-source voltage, V_{DS}, for reliable performance. It is important to understand the leakage current characteristics of the Schottky diode, especially at high operating temperatures because it impacts the overall converter operation and efficiency.

Use Equation 27 to calculate the current through the diode, I_D.

$$I_D = I_{LED(MAX)} \tag{27}$$

Application Information (continued)

The diode power rating and package is selected based on the calculated current, the ambient temperature and the maximum allowable temperature rise.

9.1.7 LED Current Programming

The LED current is set by the external current sense resistor, R_{CS}, and the analog adjust voltage, V_{IADJ}. The current sense resistor is placed in series with the LED load. The CSP and CSN inputs of the internal rail-to-rail current sense amplifier are connected to the R_{CS} resistor to enable closed-loop regulation. When V_{IADJ} > 2.5 V, the internal 2.4-V reference sets the $V_{(CSP-CSN)}$ threshold to 170.7 mV and the LED current is regulated to:

$$I_{LED} \quad \frac{170.7\ mV}{R_{CS}} \tag{28}$$

The LED current can be programmed by varying V_{IADJ} between 140 mV to 2.25 V. The LED current can be calculated using:

$$I_{LED} \quad \frac{V_{IADJ}}{14 \times R_{CS}} \tag{29}$$

TI recommends a low-pass common-mode filter consisting of 10-Ω resistors in series with CSP and CSN inputs and 0.01-µF capacitors to ground to minimize the impact of voltage ripple and noise on LED current accuracy (see *Figure 24* section). A 0.1-µF capacitor across CSP and CSN is included to filter high-frequency differential noise.

9.1.8 Switch Current Sense Resistor

The switch current sense resistor, R_{IS}, is used to implement peak current mode control and to set the peak switch current limit. The value of R_{IS} is selected to protect the main switching MOSFET under fault conditions. The R_{IS} can be calculated based on peak inductor current, $i_{L(PK)}$, and switch current limit threshold, $V_{IS(LIMIT)}$.

$$R_{IS} \quad \frac{V_{IS(LIMIT)}}{I_{L(PK)}} \tag{30}$$

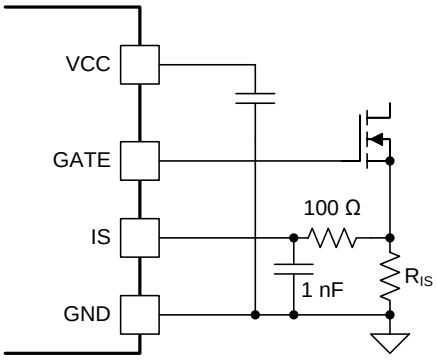


Figure 40. IS Input Filter

The use of a 1-nF and 100-Ω low-pass filter is optional. If used, the recommended resistor value is less than 500 Ω in order to limit its influence on the internal slope compensation signal.

9.1.9 Slope Compensation

The magnitude of internal artificial ramp, V_{SL}, is set by slope resistor R_{SLP}. The device compensates for the changes in input voltage, V_{IN} and output voltage sensed by CSP pin, V_{CSP} to achieve stable inner current loop operation over wide range of operating conditions. The value of R_{SLP} is determined by the inductor, L and the switch current sense resistor, R_{IS} and is independent of input and output voltage for Boost, Boost-to-Battery and Buck-Boost topologies.

$$R_{SL} \quad 274.4 \times 10^{6} \times \frac{L}{R_{IS}} \ (\Omega) \tag{31}$$

Application Information (continued)

9.1.10 Feedback Compensation

The open-loop response is the product of the modulator transfer function (shown in Equation 32) and the feedback transfer function. Using a first-order approximation, the modulator transfer function can be modeled as a single pole created by the output capacitor, and in the boost and buck-boost topologies, a right half-plane zero created by the inductor, where both have a dependence on the LED string dynamic resistance, r_D. The ESR of the output capacitor is neglected in the analysis. The small-signal modulator model also includes a DC gain factor that is dependent on the duty cycle, output voltage, and LED current.

$$\frac{\hat{i}_{LED}}{\hat{v}_{COMP}} \quad G_0 \times \frac{\left(1 - \frac{s}{\omega_Z}\right)}{\left(1 + \frac{s}{\omega_P}\right)} \tag{32}$$

The *Table 2* summarizes the expression for the small-signal model parameters.

Table 2. Small-Signal Model Parameters

	DC GAIN (G_0)	POLE FREQUENCY (ω_P)	ZERO FREQUENCY (ω_Z)
Boost	$\frac{(1-D)\times V_O}{R_{IS}\times\left(V_O+\left(r_D\times I_{LED}\right)\right)}$	$\frac{V_O+\left(r_D\times I_{LED}\right)}{V_O\times r_D\times C_{OUT}}$	$\frac{V_O\times(1-D)^2}{L\times I_{LED}}$
Buck-Boost	$\frac{(1-D)\times V_O}{R_{IS}\times\left(V_O+\left(D\times r_D\times I_{LED}\right)\right)}$	$\frac{V_O+\left(D\times r_D\times I_{LED}\right)}{V_O\times r_D\times C_{OUT}}$	$\frac{V_O\times(1-D)^2}{D\times L\times I_{LED}}$

The feedback transfer function includes the current sense resistor and the loop compensation of the transconductance amplifier. A compensation network at the output of the error amplifier is used to configure loop gain and phase characteristics. A simple capacitor, C_{COMP}, from COMP to GND (as shown in Figure 41) provides integral compensation and creates a pole at the origin. Alternatively, a network of R_{COMP}, C_{COMP}, and C_{HF}, shown in Figure 42, can be used to implement proportional and integral (PI) compensation to create a pole at the origin, a low-frequency zero, and a high-frequency pole.

The feedback transfer function is defined as follows.

Feedback transfer function with integral compensation:

$$-\frac{\hat{v}_{COMP}}{\hat{i}_{LED}} \quad \frac{14\times g_M\times R_{CS}}{s\times C_{COMP}} \tag{33}$$

Feedback transfer function with proportional integral compensation:

$$-\frac{\hat{v}_{COMP}}{\hat{i}_{LED}} = \frac{14\times g_M\times R_{CS}}{s\times\left(C_{COMP}+C_{HF}\right)}\frac{\left(1+s\times R_{COMP}\times C_{COMP}\right)}{\left(1+s\times R_{COMP}\times\left(\frac{C_{COMP}\times C_{HF}}{C_{COMP}+C_{HF}}\right)\right)} \tag{34}$$

The pole at the origin minimizes output steady-state error. High bandwidth is achieved with the PI compensator by placing the low-frequency zero an order of magnitude less than the crossover frequency. Use the following expressions to calculate the compensation network.

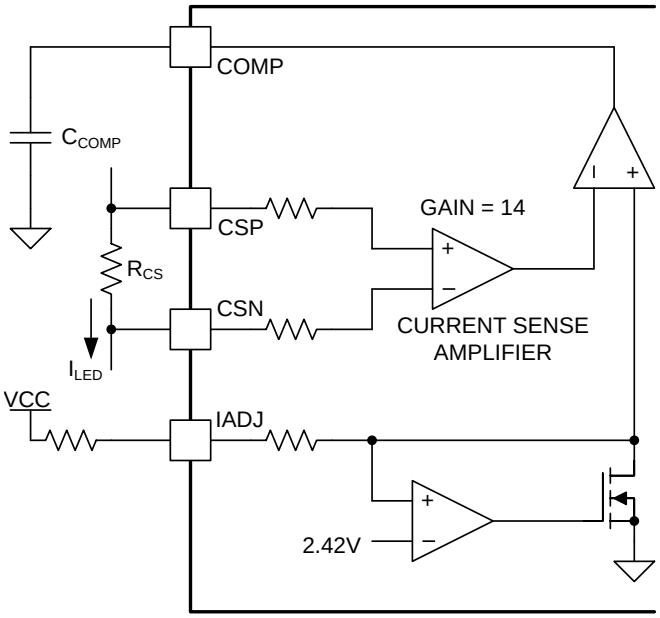


Figure 41. Integral Compensator

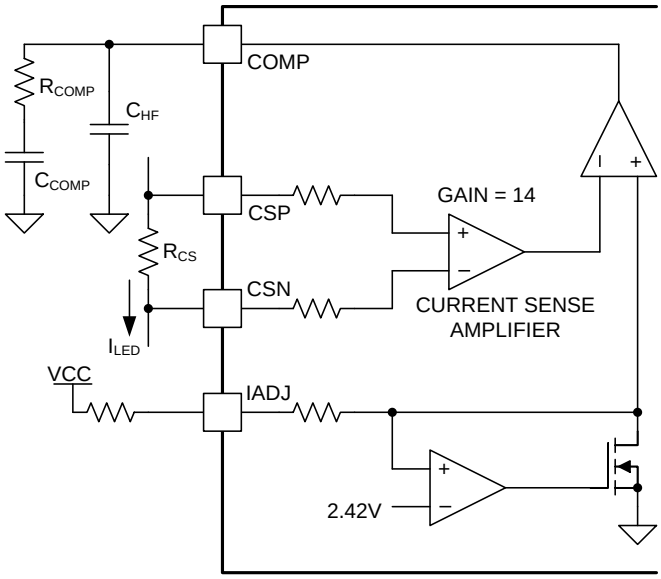


Figure 42. Proportional Integral Compensator

Boost and Buck-Boost with integral compensator:

$$C_{COMP} \quad \frac{8.75 \times 10^{-3} \times R_{CS}}{\omega_P} \tag{35}$$

Boost and Buck-Boost with proportional integral compensator:

$$C_{COMP} \quad 8.75 \times 10^{-3} \times \left(\frac{R_{CS} \times G_0}{\omega_Z} \right) \tag{36}$$

$$C_{HF} \quad \frac{C_{COMP}}{100} \tag{37}$$

$$R_{COMP} \quad \frac{1}{\omega_P \times C_{COMP}} \tag{38}$$

The loop response is verified by applying step input voltage transients. The goal is to minimize LED current overshoot and undershoot with a damped response. Additional tuning of the compensation network may be necessary to optimize PWM dimming performance.

9.1.11 Soft-Start

The soft-start time (t_{SS}) is the time required for the LED current to reach the target set point. The required soft-start time is programmed using a capacitor, C_{SS}, from SS pin to GND, and is based on the LED current, output capacitor, and output voltage.

$$C_{SS} \quad 12.5 \times 10^{-6} \times t_{SS} \tag{39}$$

9.1.12 Overvoltage and Undervoltage Protection

The overvoltage threshold is programmed using a resistor divider, R_{OV2} and R_{OV1}, from the output voltage, V_O, to GND for Boost and SEPIC topologies, as shown in Figure 36 and Figure 38. If the LEDs are referenced to a potential other than GND, as in the Buck-Boost, the output voltage is sensed and translated to ground by using a PNP transistor and level-shift resistors, as shown in Figure 37. The overvoltage turn-off threshold, $V_{O(OV)}$, is:

Boost:

$$V_{O(OV)} \quad V_{OVP(THR)} \times \left(\frac{R_{OV1} + R_{OV2}}{R_{OV1}} \right) \tag{40}$$

Buck and Buck-Boost:

$$V_{O(OV)} \quad V_{OVP(THR)} \times \frac{R_{OV2}}{R_{OV1}} + 0.7 \tag{41}$$

The overvoltage hysteresis, $V_{OV(HYS)}$ is:

$$V_{OV(HYS)} = I_{OVP(HYS)} \times R_{OV2} \tag{42}$$

The corresponding undervoltage fault threshold, $V_{O(UV)}$ is:

$$V_{O(UV)} \quad 0.1 \times \frac{R_{OV1} + R_{OV2}}{R_{OV1}} \tag{43}$$

9.1.13 Analog to PWM Dimming Considerations

The analog to PWM duty cycle translation is based on the internal PWM generator, configured by connecting a capacitor across RAMP pin and GND, as shown in Figure 29. The minimum PWM duty cycle is programmed by setting the voltage on DIM/PWM pin, V_{DIM} using a resistor divider from VREF pin to GND.

$$V_{DIM} = 1 + 2 \times D_{DIM(MIN)} \tag{44}$$

$$R_{DIM2} \quad \left(\frac{V_{REF} - V_{DIM}}{V_{DIM}} \right) \times R_{DIM1} \tag{45}$$

The device is designed to support a minimum PWM duty cycle of 4% with better than 5% accuracy from DIM/PWM input to PDRV output in this operating mode. To avoid excess loading of the VREF LDO output, TI recommends a resistor network with sum of resistors R_{DIM1} and R_{DIM2} greater than 10 kΩ. A bypass capacitor of 0.1-µF prevents noise coupling and improves performs for low dimming values.

9.1.14 Direct PWM Dimming Considerations

The device can be configured to implement dimming function based on external PWM command by disabling the internal ramp generator, as explained in *DIM/PWM Input* section. The internal comparator reference is set to 2.49 V by connecting a 249-kΩ resistor, R_{RAMP}, from the RAMP pin to GND. The internal PWM duty cycle is controlled by an external 5-V or 3.3-V signal, generated by a command module or a microcontroller.

9.1.15 Series P-Channel MOSFET Selection

When PWM dimming, the device requires another P-channel MOSFET placed in series with the LED load. Select a P-channel MOSFET with gate-to-source voltage rating of 10-V or higher and with a drain-to-source breakdown voltage rating greater than the output voltage. Ensure that the drain current rating of the P-channel MOSFET exceeds the programmed LED current by at least 10%.

It is important to consider the FET input capacitance and on-resistance as it impacts the accuracy and efficiency of the LED driver. TI recommends a FET with lower input capacitance and gate charge to minimize the errors caused by rise and fall times when PWM dimming at low duty cycles.

9.2 Typical Applications

9.2.1 Typical Boost LED Driver

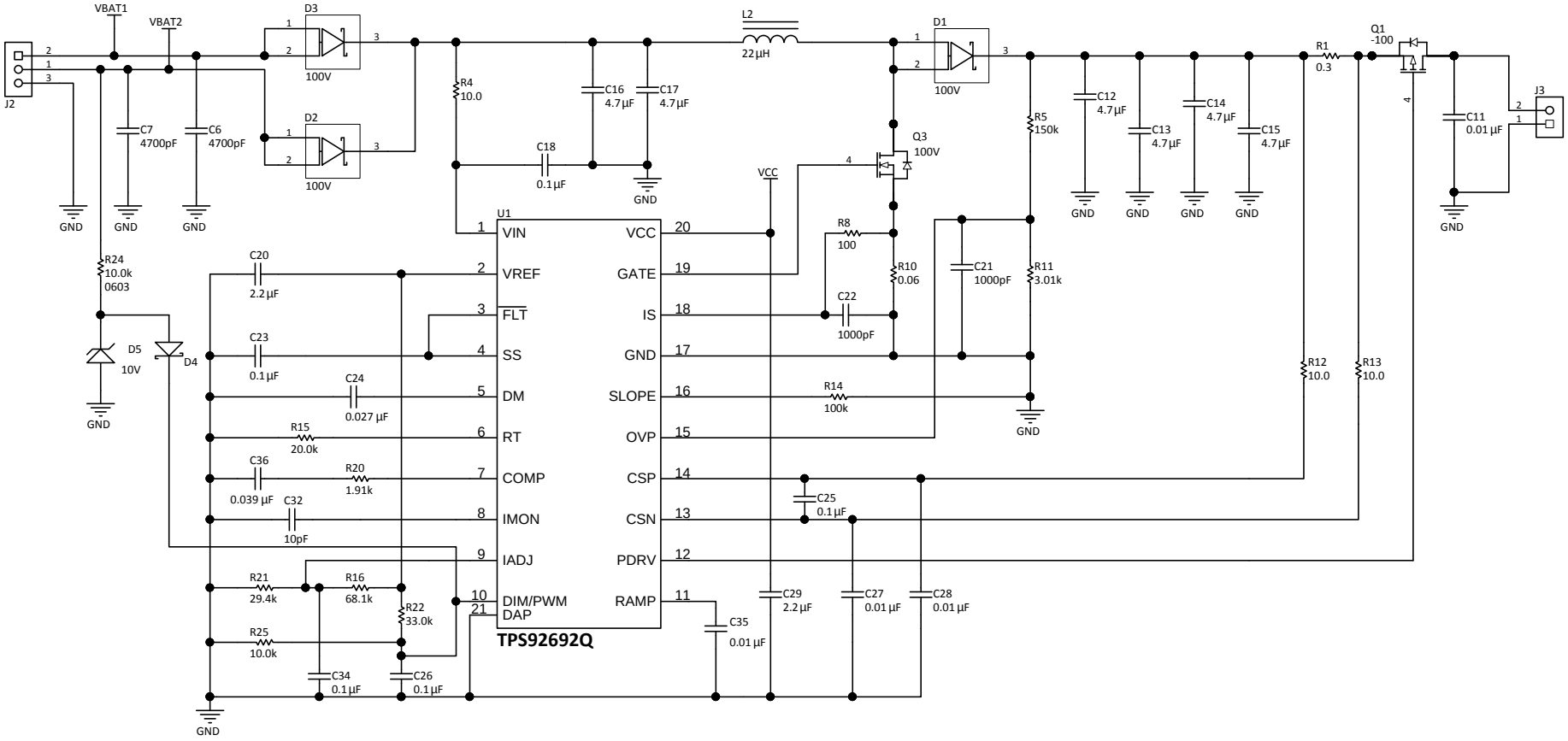


Figure 43. Boost LED Driver With High-Side Current Sense

9.2.1.1 Design Requirements

Table 3 shows the design parameters for the boost LED driver application.

Table 3. Design Parameters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
	Input voltage range		7	14	18	V
	Input UVLO setting			4.5		V
OUTPUT CHARACTERISTICS						
	LED forward voltage		2.8	3.2	3.6	V
	Number of LEDs in series			14		
V_O	Output voltage	LED+ to LED–	39.2	44.8	50.4	V
I_{LED}	Output current			350	500	mA
RR	LED current ripple ratio			4%		
r_D	LED string resistance			3		Ω
$P_{O(MAX)}$	Maximum output power				25	W
f_{PWM}	PWM dimming frequency			240		Hz
D_{PWM}	Analog to PWM duty cycle set point (low brightness mode)			8		%
SYSTEMS CHARACTERISTICS						
$P_{O(BDRY)}$	Output power at CCM-DCM boundary condition			6		W
$\Delta v_{IN(PP)}$	Input voltage ripple			20		mV
$V_{O(OV)}$	Output overvoltage protection threshold			62		V
$V_{OV(HYS)}$	Output overvoltage protection hysteresis			3		V
t_{ss}	Soft-start period			8		ms
f_{DM}	Dither Modulation Frequency			600		Hz
f_{SW}	Switching frequency			390		kHz

9.2.1.2 Detailed Design Procedure

This procedure is for the boost LED driver application.

9.2.1.2.1 Calculating Duty Cycle

Solve for D, D_{MAX}, and D_{MIN}:

$$D_{MAX} \quad \frac{V_{O(TYP)} - V_{IN(TYP)}}{V_{O(TYP)}} \quad \frac{44.8 - 14}{44.8} \quad 0.688 \tag{46}$$

$$D_{MAX} \quad \frac{V_{O(MAX)} - V_{IN(MIN)}}{V_{O(MAX)}} \quad \frac{50.4 - 7}{50.4} \quad 0.861 \tag{47}$$

$$D_{MIN} \quad \frac{V_{O(MIN)} - V_{IN(MAX)}}{V_{O(MIN)}} \quad \frac{39.2 - 18}{39.2} \quad 0.541 \tag{48}$$

9.2.1.2.2 Setting Switching Frequency

Solve for R_T:

$$R_T \quad \frac{1.432 \times 10^{10}}{\left(f_{SW}\right)^{1.047}} \quad \frac{1.432 \times 10^{10}}{\left(390 \times 10^3\right)^{1.047}} \quad 20.05 \times 10^3 \tag{49}$$

The closest standard resistor of 20 kΩ is selected.

9.2.1.2.3 Setting Dither Modulation Frequency

Solve for C_{DM}:

$$C_{DM} \quad \frac{10\times10^{-6}}{2\times f_{MOD}\times 0.3} \quad \frac{10\times10^{-6}}{2\times 600\times 0.3} \quad 27.7\times10^{-9} \tag{50}$$

The closest standard capacitor is 27 nF.

9.2.1.2.4 Inductor Selection

The inductor is selected to meet the CCM-DCM boundary power requirement, $P_{O(BDRY)}$. In most applications, $P_{O(BDRY)}$ is set to be 1/3 of the maximum output power, $P_{O(MAX)}$. The inductor value is calculated for typical input voltage, $V_{IN(TYP)}$, and output voltage, $V_{O(TYP)}$:

$$L \quad \frac{V_{IN(MAX)}^2}{2\times P_{O(BDRY)}\times f_{SW}}\times\left(1-\frac{V_{IN(TYP)}}{V_{O(TYP)}}\right) \quad \frac{(14)^2}{2\times 8\times 390\times10^3}\times\left(1-\frac{14}{44.8}\right) \quad 21.59\times10^{-6} \tag{51}$$

The closest standard inductor is 22 µH.

For best results, ensure that the inductor saturation current rating is greater than the peak inductor current, $I_{L(PK)}$.

$$i_{L(PK)} \quad \frac{P_{O(MAX)}}{V_{IN(MIN)}}+\frac{V_{IN(MIN)}}{2\times L\times f_{SW}\times V_{O(MAX)}}\times\left(1-\frac{V_{IN(MIN)}}{V_{O(MAX)}}\right) \quad \frac{25}{7}+\frac{7}{2\times22\times10^{-6}\times390\times10^3\times50.4}\times\left(1-\frac{7}{50.4}\right) \quad 3.58 \tag{52}$$

9.2.1.2.5 Output Capacitor Selection

The specified peak-to-peak LED current ripple, $\Delta i_{LED(PP)}$, is:

$$\Delta i_{LED(PP)} = RR\times I_{LED(MAX)} = 0.03\times500\times10^{-3} \quad 15\times10^{-3} \tag{53}$$

The output capacitance required to achieve the target LED current ripple is:

$$C_{OUT} \quad \frac{P_{O(MAX)}}{\Delta i_{LED(PP)}\times r_{D(MIN)}\times f_{SW}\times V_{O(MAX)}}\times\left(1-\frac{V_{IN(MIN)}}{V_{O(MAX)}}\right) \quad \frac{25}{15\times10^{-3}\times4.2\times390\times10^3\times50.4}\times\left(1-\frac{7}{50.4}\right)=17.38\times10^{-6} \tag{54}$$

Four 4.7-µF, 100-V rated X7R ceramic capacitors are used in parallel to achieve a combined output capacitance of 18.8 µF.

9.2.1.2.6 Input Capacitor Selection

The input capacitor is required to reduce switching noise conducted through the input wires and reduced the input impedance of the LED driver. The capacitor required to limit peak-to-peak input ripple voltage ripple, $\Delta v_{IN(PP)}$, to 20 mV is given by:

$$C_{IN} \quad \frac{V_{IN(MIN)}}{8\times L\times f_{SW}^2\times\Delta v_{IN(PP)}}\times\left(1-\frac{V_{IN(MIN)}}{V_{O(MAX)}}\right) \quad \frac{7}{8\times22\times10^{-6}\times390\times10^3\times20\times10^{-3}}\times\left(1-\frac{7}{50.4}\right)=11.26\times10^{-6} \tag{55}$$

Two 4.7-µF, 50-V X7R ceramic capacitors are used in parallel to achieve a combined input capacitance of 9.4-µF.

9.2.1.2.7 Main N-Channel MOSFET Selection

Ensure that the MOSFET ratings exceed the maximum output voltage and RMS switch current.

$$V_{DS} = V_{O(OV)}\times1.1 = 62\times1.1 = 68.2 \tag{56}$$

$$I_{Q(RMS)} \quad \frac{P_{O(MAX)}}{V_{IN(MIN)}}\times\sqrt{\left(1+\frac{V_{IN(MIN)}}{V_{O(MIN)}}\right)} \quad \frac{25}{7}\times\sqrt{\left(1+\frac{7}{39.2}\right)} \quad 3.88 \tag{57}$$

A N-channel MOSFET with a voltage rating of 100-V and a current rating of 4 A is required for this design.

9.2.1.2.8 Rectifying Diode Selection

Select a diode should be selected based on the following voltage and current ratings:

$$V_{D(BR)} \quad V_{O(OV)} \times 1.2 \quad 62 \times 1.1 \quad 68.2 \tag{58}$$

$$I_D = I_{LED(MAX)} = 0.5 \tag{59}$$

A 100-V Schottky diode with low reverse leakage current is suitable for this design. The package must be able to handle the power dissipation resulting from continuous forward current, I_D, of 0.5 A.

9.2.1.2.9 Programming LED Current

The LED current can be programmed to match the LED string configuration by using a resistor divider, R_{ADJ1} and R_{ADJ2}, from V_{REF} to GND for a given sense resistor, R_{CS}, as shown in Figure 43. To maximize the accuracy, the IADJ pin voltage is set to 2.1 V for the specified maximum LED current of 500-mA. The current sense resistor, R_{CS}, is then calculated as:

$$R_{CS} \quad \frac{V_{IADJ(MAX)}}{14 \times I_{LED(MAX)}} \quad \frac{2.1}{14 \times 0.5} \quad 0.3 \tag{60}$$

A standard resistor of 0.3 Ω is selected. Table 4 summarizes the IADJ pin voltage and the choice of the R_{ADJ1} and R_{ADJ2} resistors for different current settings.

Table 4. Design Requirements

LED CURRENT	IADJ VOLTAGE (V_{IADJ})	R_{ADJ1}	R_{ADJ2}
100 mA	420 mV	6.34 kΩ	68.1 kΩ
350 mA	1.47 V	29.4 kΩ	68.1 kΩ
500 mA	2.1 V	49.9 kΩ	68.1 kΩ

9.2.1.2.10 Setting Switch Current Limit

Solve for current sense resistor, R_{IS}:

$$R_{IS} \quad \frac{V_{IS(LIMIT)}}{I_{L(PK)}} \quad \frac{0.25}{3.58} \quad 0.07 \tag{61}$$

A standard value of 0.06 Ω is selected.

9.2.1.2.11 Programming Slope Compensation

The artificial slope is programmed by resistor, R_{SL}.

$$R_{SL} \quad 274.4 \times 10^6 \times \frac{L}{R_{IS}} \quad 274.4 \times 10^6 \times \frac{22 \times 10^{-6}}{0.06} \quad 100.6 \times 10^3 \tag{62}$$

A standard resistor of 100 kΩ is selected.

9.2.1.2.12 Deriving Compensator Parameters

The modulator transfer function for the Boost converter is derived for nominal V_{IN} voltage and corresponding duty cycle, D, and is given by the following equation. (See Feedback Compensation section for more information.)

$$\frac{\hat{i}_{LED}}{\hat{v}_{COMP}} \quad G_0 \times \frac{\left(1 - \frac{s}{\omega_Z}\right)}{\left(1 + \frac{s}{\omega_P}\right)} \quad 2.184 \times \frac{\left(1 - \frac{s}{311.8 \times 10^3}\right)}{\left(1 + \frac{s}{13.4 \times 10^3}\right)} \tag{63}$$

The proportional-integral compensator components C_{COMP} and R_{COMP} are obtained by solving the following expressions:

$$C_{COMP} \quad 8.75 \times 10^{-3} \times \left(\frac{R_{CS} \times G_0}{\omega_Z}\right) \quad 8.75 \times 10^{-3} \times \left(\frac{0.3 \times 2.184}{311.8 \times 10^3}\right) \quad 0.018 \times 10^{-6} \tag{64}$$

$$R_{COMP} \quad \frac{1}{\omega_P \times C_{COMP}} \quad \frac{1}{13.4\times10^{3}\times18\times10^{-9}} \quad 4.12\times10^{3} \tag{65}$$

The closet standard capacitor of 18-nF and resistor of 4.12-kΩ is selected. The high frequency pole location is set by a 1-nF C_{HF} capacitor.

9.2.1.2.13 Setting Start-up Duration

The soft-start capacitor required to achieve start-up in 8 ms is given by:

$$C_{SS} \quad 12.5\times10^{-6}\times t_{SS} \quad 12.5\times10^{-6}\times8\times10^{-3} \quad 100\times10^{-9} \tag{66}$$

The closet standard capacitor of 100 nF is selected.

9.2.1.2.14 Setting Overvoltage Protection Threshold

The overvoltage protection threshold of 62 V and hysteresis of 3 V is set by the R_{OV1} and R_{OV2} resistor divider.

$$R_{OV2} \quad \frac{V_{OV(HYS)}}{20\times10^{-6}} \quad \frac{3}{20\times10^{-6}} \quad 150\times10^{3} \tag{67}$$

$$R_{OV1} \quad \left(\frac{1.228}{V_{O(OV)}-1.228}\right)\times R_{OV2} \quad \left(\frac{1.228}{62-1.228}\right)\times150\times10^{3} \quad 3.03\times10^{3} \tag{68}$$

The standard resistor values of 150 kΩ and 3.01 kΩ are chosen.

9.2.1.2.15 Analog-to-PWM Dimming Considerations

The PWM dimming frequency is set by the C_{RAMP} capacitor.

$$C_{DIM} \quad \frac{10\times10^{-6}}{2\times2\times f_{DIM}} \quad \frac{10\times10^{-6}}{2\times2\times240} \quad 10.4\times10^{-9} \tag{69}$$

The closet standard capacitor of 10 nF is selected.

The PWM duty cycle of 8% programmed by setting the DIM/PWM voltage using resistor divider, R_{DIM1} and $_{RDIM2}$ connected from VREF pin to GND.

$$V_{DIM} = 2\times D_{PWM} + 1 = 2\times0.08 + 1 = 1.16 \tag{70}$$

The value of resistor, R_{DIM1} is set as of 10-kΩ. The resistor R_{DIM2} is calculated using the following equation:

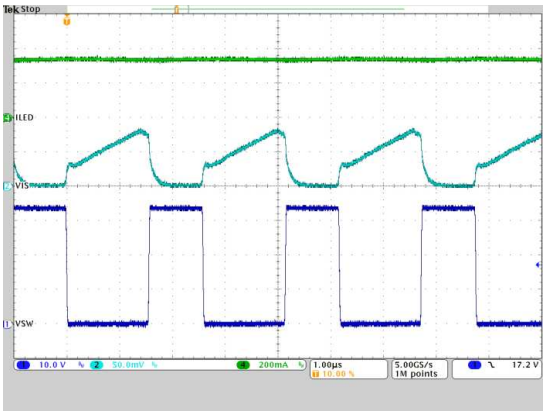
$$R_{DIM2} \quad \frac{V_{REF}-V_{DIM}}{V_{DIM}}\times R_{DIM1} \quad \frac{4.96-1.16}{4.96}\times10\times10^{3} \quad 32.76\times10^{3} \tag{71}$$

A standard resistor of 33 kΩ is selected.

A P-channel MOSFET with a voltage rating of 100-V and a current rating of 1 A is required to enable series FET dimming for this design.

9.2.1.3 Application Curves

These curves are for the boost LED driver.



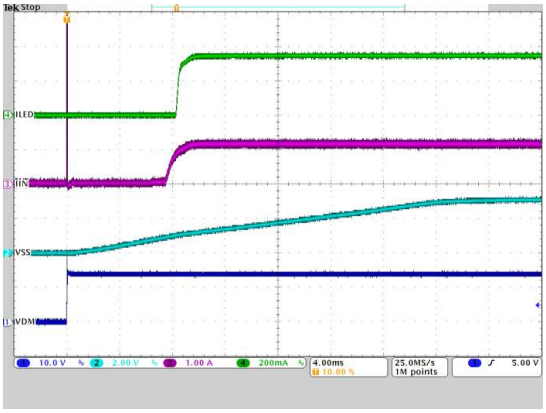
Ch1: Switch node voltage;
Ch2: Switch current sense voltage;
Ch4: LED current; Time: 1 µs/div

Figure 44. Normal Operation



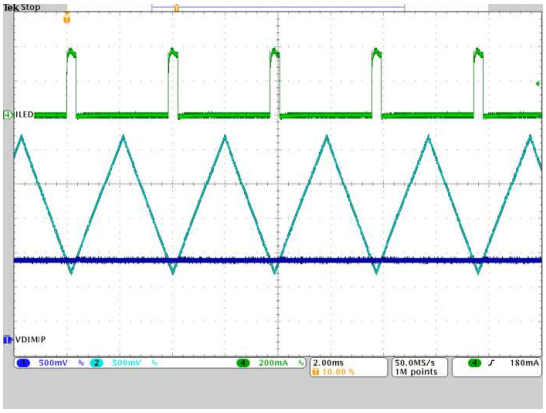
Ch1: Dither modulation voltage;
Ch4: LED current; Time: 400 µs/div

Figure 45. Spread Spectrum Frequency Modulation



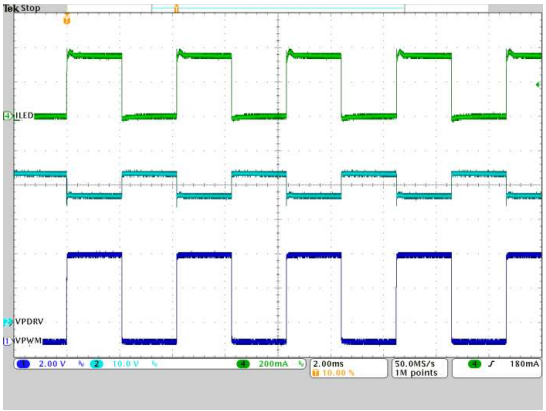
Ch1: Input voltage; Ch2: Soft-start (SS) voltage;
Ch3: Input current;
Ch4: LED current; Time: 4 ms/div

Figure 46. Startup Transient



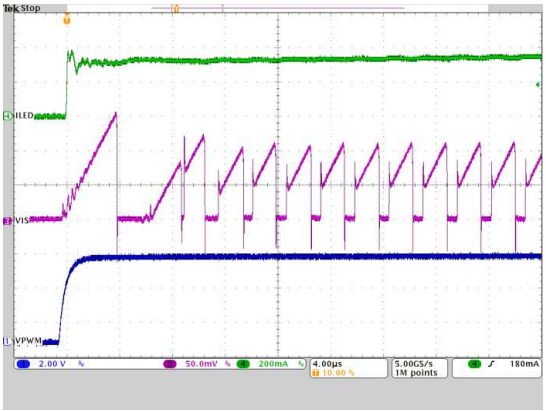
Ch1: Dim/PWM voltage;
Ch2: RAMP pin voltage;
Ch4: LED current; Time: 2 ms/div

Figure 47. Analog-to-PWM Dimming Transient



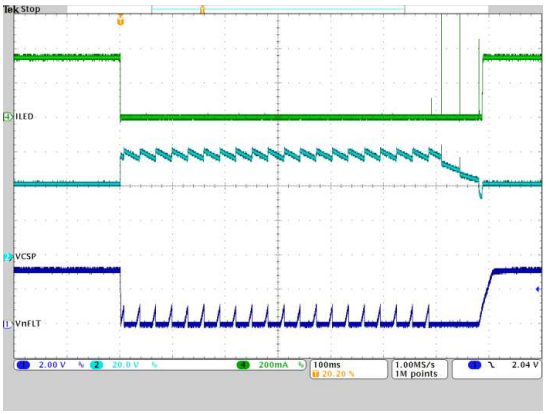
Ch1: External PWM input signal;
Ch2: PDRV voltage;
Ch4: LED current; Time: 2 ms/div

Figure 48. Direct PWM Dimming Transient



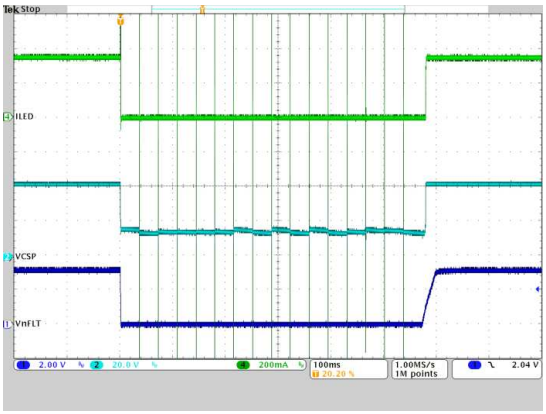
Ch1: External PWM input voltage;
Ch3: Switch sense current resistor voltage;
Ch4: LED current; Time: 4 µs/div

Figure 49. PWM Dimming Transient (Zoomed)



Ch1: $\overline{\text{FLT}}$ output;
Ch2: CSP pin voltage;
Ch4: LED current; Time: 100 ms/div

Figure 50. LED Open-Circuit Fault



Ch1: $\overline{\text{FLT}}$ output;
Ch2: CSP pin voltage;
Ch4: LED current; Time: 100 ms/div

Figure 51. LED Short-Circuit Fault

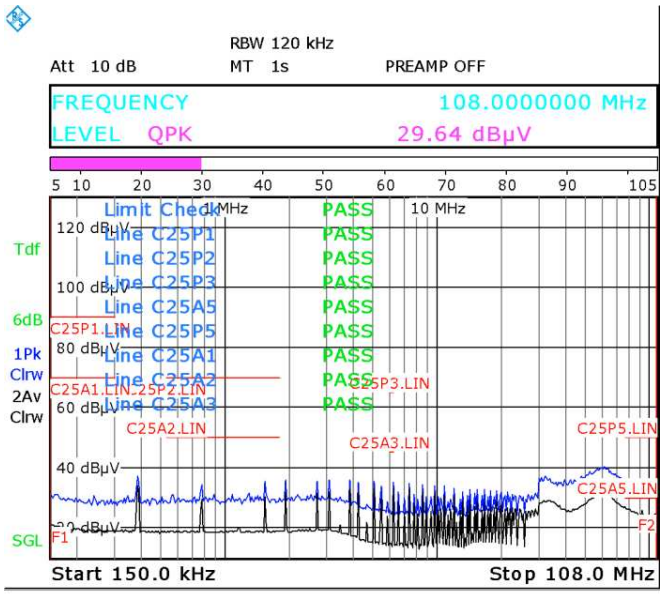


Figure 52. Conducted EMI Scan (SSFM Disabled)

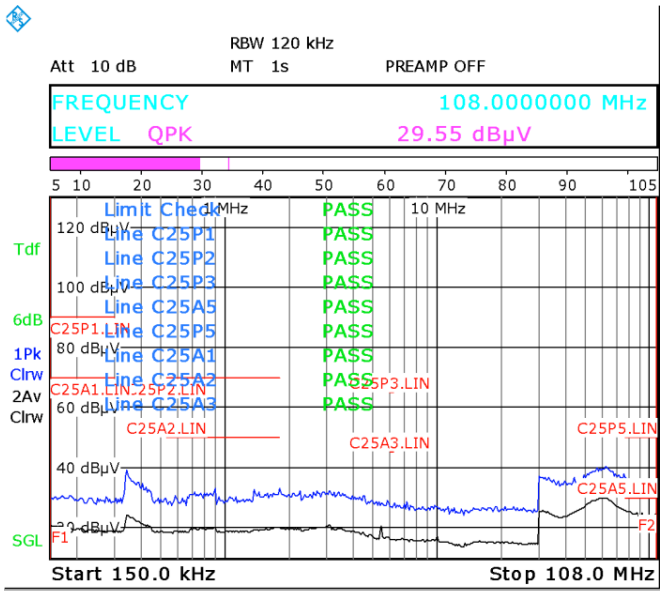


Figure 53. Conducted EMI Scan (SSFM Enabled)

9.2.2 Typical Buck-Boost LED Driver

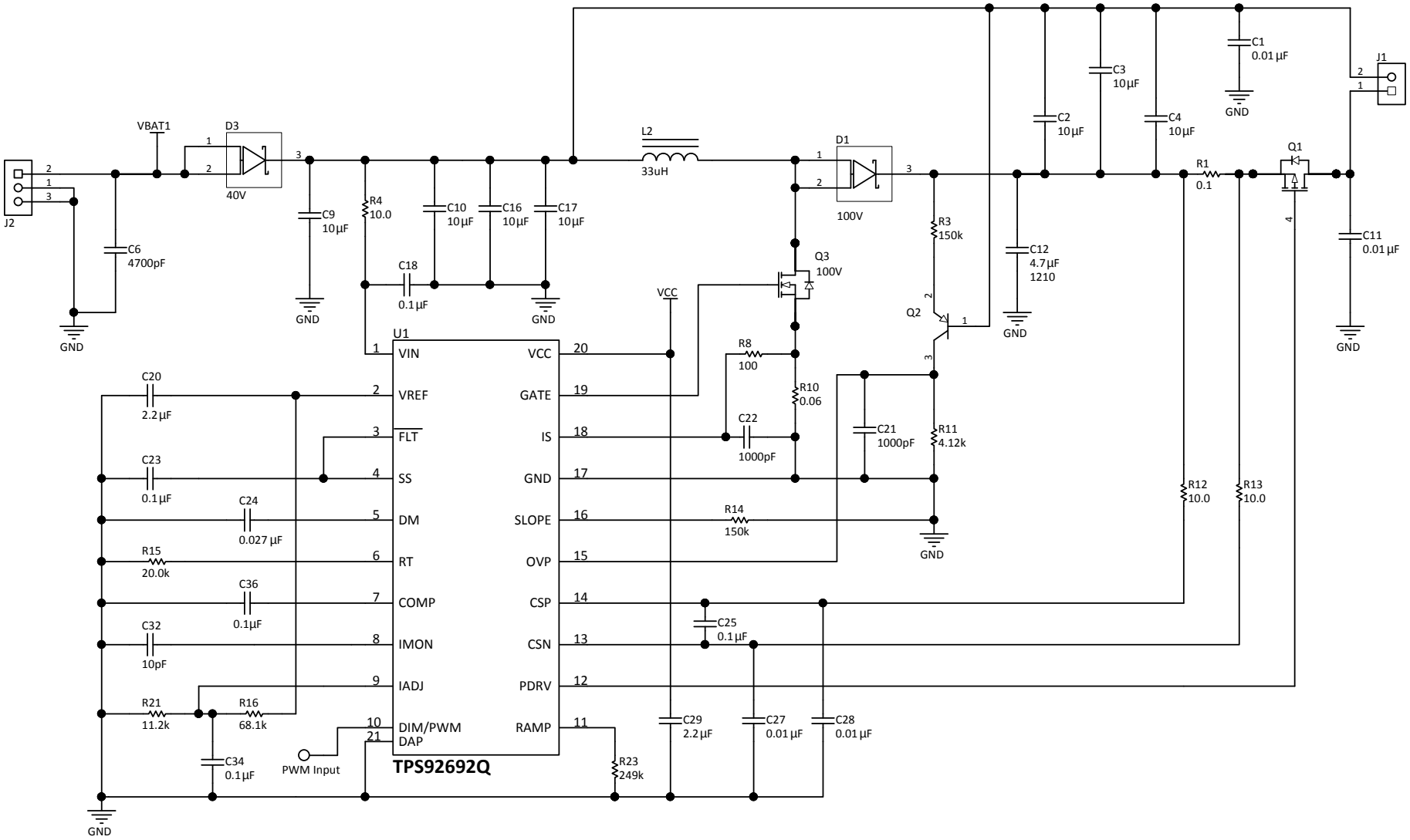


Figure 54. Buck-Boost LED Driver

9.2.2.1 Design Requirements

Buck-Boost LED drivers provide the flexibility needed in applications that support multiple LED load configurations. For such applications, it is necessary to modify the design procedure presented in to account for the wider range of output voltage and LED current specifications. This design is based on the maximum output power $P_{O(MAX)}$, set by the lumen output specified for the lighting application. The design procedure for a battery connected application with 3 to 9 LEDs in series and maximum 15 W output power is outlined in this section.

Table 5. Design Parameters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
	Input voltage range		7	14	18	V
	Input UVLO setting			4.5		V
OUTPUT CHARACTERISTICS						
	LED forward voltage		2.8	3.2	3.6	V
	Number of LEDs in series		3	7	11	
V_O	Output voltage	LED+ to LED–	8.4	22.4	39.6	V
I_{LED}	Output current		100	500	1500	mA
$\Delta i_{LED(PP)}$	LED current ripple			5%		
r_D	LED string resistance		0.9	2.1	3.3	Ω
$P_{O(MAX)}$	Maximum output power				12.6	W
D_{PWM}	Direct PWM dimming range	f_{PWM} = 240 Hz	4%		100%	
SYSTEMS CHARACTERISTICS						
$P_{O(BDRY)}$	Output power at CCM-DCM boundary condition			3		W
$\Delta v_{IN(PP)}$	Input voltage ripple			70		mV
$V_{O(OV)}$	Output overvoltage protection threshold			45		V
$V_{OV(HYS)}$	Output overvoltage protection hysteresis			3		V
t_{SS}	Soft-start period			8		ms
f_{SW}	Switching frequency			390		kHz

9.2.2.2 Detailed Design Procedure

9.2.2.2.1 Calculating Duty Cycle

Solving for D, D_{MAX}, and D_{MIN}:

$$D \quad \frac{V_{O(TYP)}}{V_{O(TYP)} + V_{IN(TYP)}} \quad \frac{22.4}{22.4 + 14} \quad 0.615 \tag{72}$$

$$D_{MAX} \quad \frac{V_{O(MAX)}}{V_{O(MAX)} + V_{IN(MIN)}} \quad \frac{39.6}{39.6 + 7} \quad 0.850 \tag{73}$$

$$D_{MIN} \quad \frac{V_{O(MIN)}}{V_{O(MIN)} + V_{IN(MAX)}} \quad \frac{8.4}{8.4 + 18} \quad 0.318 \tag{74}$$

9.2.2.2.2 Setting Switching Frequency

Solving for R_T resistor:

$$R_T \quad \frac{1.432 \times 10^{10}}{\left(f_{SW}\right)^{1.047}} \quad \frac{1.432 \times 10^{10}}{\left(390 \times 10^3\right)^{1.047}} \quad 20.05 \times 10^3 \tag{75}$$

9.2.2.2.3 Setting Dither Modulation Frequency

Solve for C_{DM}:

$$C_{DM} \quad \frac{10\times10^{-6}}{2\times f_{MOD}\times 0.3} \quad \frac{10\times10^{-6}}{2\times 600\times 0.3} \quad 27.7\times10^{-9} \tag{76}$$

The closest standard capacitor is 27 nF.

9.2.2.2.4 Inductor Selection

The inductor is selected to meet the CCM-DCM boundary power requirement, $P_{O(BDRY)}$. Typically, the boundary condition is set to enable CCM operation at the lowest possible operating power based on minimum LED forward voltage drop and LED current. In most applications, $P_{O(BDRY)}$ is set to be 1/3 of the maximum output power, $P_{O(MAX)}$. The inductor value is calculated for maximum input voltage, $V_{IN(MAX)}$, and output voltage, $V_{O(MAX)}$:

$$L \quad \frac{1}{2\times P_{O(BDRY)}\times f_{SW}\times\left(\frac{1}{V_{O(TYP)}}+\frac{1}{V_{IN(TYP)}}\right)^2} \quad \frac{1}{2\times 3\times 390\times10^{3}\times\left(\frac{1}{22.4}+\frac{1}{14}\right)^2} \quad 31.72\times10^{-6} \tag{77}$$

The closest standard value of 33 µH is selected. The inductor ripple current is given by:

$$\Delta i_{L(PP)} \quad \frac{V_{IN(MIN)}\times D_{MAX}}{L\times f_{SW}} \quad \frac{7\times 0.85}{33\times10^{-6}\times 390\times10^{3}} \quad 0.4623 \tag{78}$$

Ensure that the inductor saturation rating exceeds the calculated peak current which is based on the maximum output power using Equation 79.

$$I_{L(PK)} \quad P_{O(MAX)}\times\left(\frac{1}{V_{O(MIN)}}+\frac{1}{V_{IN(MIN)}}\right)+\frac{V_{O(MIN)}\times V_{IN(MIN)}}{2\times L\times f_{SW}\times\left(V_{O(MIN)}+V_{IN(MIN)}\right)} \tag{79}$$

$$I_{L(PK)}=12.6\times\left(\frac{1}{8.4}+\frac{1}{7}\right)+\frac{8.4\times 7}{2\times 33\times10^{-6}\times 390\times10^{3}\times\left(8.4+7\right)} \quad 3.45$$

9.2.2.2.5 Output Capacitor Selection

Select the output capacitance to achieve the 5% peak-to-peak LED current ripple specification. Based on the maximum power, the capacitor is calculated in Equation 80.

$$C_{OUT} \quad \frac{P_{O(MAX)}}{f_{SW}\times r_{D(MIN)}\times\Delta i_{LED(PP)}\times\left(V_{O(MIN)}+V_{IN(MIN)}\right)} \tag{80}$$

$$C_{OUT} \quad \frac{12.6}{390\times10^{3}\times 0.9\times 0.075\times\left(8.4+7\right)} \quad 31.08\times10^{-6}$$

This design requires a minimum of three, 10-µF, 50-V and one 4.7-µF, 100-V, X7R ceramic capacitors in parallel to meet the LED current ripple specification over the entire range of output power. Additional capacitance may be required based on the derating factor under DC bias operation.

9.2.2.2.6 Input Capacitor Selection

The input capacitor is calculated based on the peak-to-peak input ripple specifications, $\Delta v_{IN(PP)}$. The capacitor required to limit the ripple to 70 mV over range of operation is calculated using:

$$C_{IN} \quad \frac{P_{O(MAX)}}{f_{SW}\times\Delta v_{IN(PP)}\times\left(V_{O(MIN)}+V_{IN(MIN)}\right)} \quad \frac{12.6}{390\times10^{3}\times 0.07\times\left(8.4+7\right)} \quad 29.97\times10^{-6} \tag{81}$$

A parallel combination of four 10-µF, 50-V X7R ceramic capacitors are used for a combined capacitance of 40 µF. Additional capacitance may be required based on the derating factor under DC bias operation.

9.2.2.2.7 Main N-Channel MOSFET Selection

Calculating the minimum transistor voltage and current rating:

$$V_{DS}=1.1\times\left(V_{O(OV)}+V_{IN(MAX)}\right)=1.1\times(45+18)=69.3 \tag{82}$$

$$I_{Q(RMS)} \quad \frac{P_{O(MAX)}}{V_{IN(MIN)}} \times \sqrt{\left(1+\frac{V_{IN(MIN)}}{V_{O(MIN)}}\right)} \quad \frac{12.6}{7} \times \sqrt{\left(1+\frac{7}{8.4}\right)} \quad 2.44 \tag{83}$$

This application requires a 100-V N-channel MOSFET with a current rating exceeding 3 A.

9.2.2.2.8 Rectifier Diode Selection

Calculating the minimum Schottky diode voltage and current rating:

$$V_{D(BR)} \quad 1.1 \times \left(V_{O(OV)} + V_{IN(MAX)}\right) \quad 1.1 \times (45+18) \quad 69.3 \tag{84}$$

$$I_D = I_{LED(MAX)} = 1.5 \tag{85}$$

This application requires a 100-V Schottky diode with a current rating exceeding 1.5 A. TI recommends a single high-current diode instead of paralleling multiple lower-current-rated diodes to ensure reliable operation over temperature.

9.2.2.2.9 Programming LED Current

The LED current can be programmed to match the LED string configuration by using a resistor divider, R_{ADJ1} and R_{ADJ2}, from V_{REF} to GND for a given sense resistor, R_{CS}, as shown in Figure 54. To maximize the accuracy, the IADJ pin voltage is set to 2.1 V for the specified LED current of 1.5 A. The current sense resistor, R_{CS}, is then calculated as:

$$R_{CS} \quad \frac{V_{IADJ}}{14 \times I_{LED(MAX)}} \quad \frac{2.1}{14 \times 1.5} \quad 0.1 \tag{86}$$

A standard resistor of 0.1 Ω is selected. Table 5 summarizes the IADJ pin voltage and the choice of the R_{ADJ1} and R_{ADJ2} resistors for different current settings.

Table 6. Design Requirements

LED CURRENT	IADJ VOLTAGE (V_{IADJ})	R_{ADJ1}	R_{ADJ2}
100 mA	140 mV	2.0 kΩ	68.1 kΩ
500 mA	700 mV	11.2 kΩ	68.1 kΩ
1.5 A	2.1 V	50 kΩ	68.1 kΩ

9.2.2.2.10 Setting Switch Current Limit and Slope Compensation

Solving for R_{IS}:

$$R_{IS} \quad \frac{V_{IS(LIMIT)}}{I_{L(PK)}} \quad \frac{0.25}{3.45} \quad 0.072 \tag{87}$$

A standard resistor of 0.06 Ω is selected.

9.2.2.2.11 Programming Slope Compensation

The artificial slope is programmed by resistor, R_{SL}.

$$R_{SL} \quad 274.4 \times 10^6 \times \frac{L}{R_{IS}} \quad 274.4 \times 10^6 \times \frac{33 \times 10^{-6}}{0.06} \quad 150.7 \times 10^3 \tag{88}$$

A standard resistor of 150 kΩ is selected.

9.2.2.2.12 Deriving Compensator Parameters

A simple integral compensator provides a good starting point to achieve stable operation across the wide operating range. The modulator transfer function with the lowest frequency pole location is calculated based on maximum output voltage, $V_{O(MAX)}$, duty cycle, D_{MAX}, LED dynamic resistance, $r_{D(MAX)}$, and minimum LED string current, $I_{LED(MIN)}$. (See Table 2 for more information.)

$$\frac{\hat{i}_{LED}}{\hat{v}_{COMP}} \quad G_0 \times \frac{\left(1 - \frac{s}{\omega_Z}\right)}{\left(1 + \frac{s}{\omega_P}\right)} \quad 2.48 \times \frac{\left(1 - \frac{s}{145.7 \times 10^3}\right)}{\left(1 + \frac{s}{8.9 \times 10^3}\right)} \tag{89}$$

The compensation capacitor needed to achieve stable response is:

$$C_{COMP} \quad \frac{8.75 \times 10^{-3} \times R_{CS}}{\omega_P} \quad \frac{8.75 \times 10^{-3} \times 0.1}{8.9 \times 10^3} \quad 98.3 \times 10^{-9} \tag{90}$$

A 100 nF capacitor is selected.

A proportional integral compensator can be used to achieve higher bandwidth and improved transient performance. However, it is necessary to experimentally tune the compensator parameters over the entire operating range to ensure stable operation.

9.2.2.2.13 Setting Startup Duration

Solving for soft-start capacitor, C_{SS}, based on 8-ms startup duration:

$$C_{SS} \quad 12.5 \times 10^{-6} \times t_{SS} \quad 12.5 \times 10^{-6} \times 8 \times 10^{-3} \quad 100 \times 10^{-9} \tag{91}$$

A 100-nF soft-start capacitor is selected.

9.2.2.2.14 Setting Overvoltage Protection Threshold

Solving for resistors, R_{OV1} and R_{OV2}:

$$R_{OV2} \quad \frac{V_{OV(HYS)}}{20 \times 10^{-6}} \quad \frac{3}{20 \times 10^{-6}} \quad 150 \times 10^3 \tag{92}$$

$$R_{OV1} \quad \frac{1.228 \times R_{OV2}}{V_{O(OV)} - 0.7} \quad \frac{1.228 \times 150 \times 10^3}{45 - 0.7} \quad 4.16 \times 10^3 \tag{93}$$

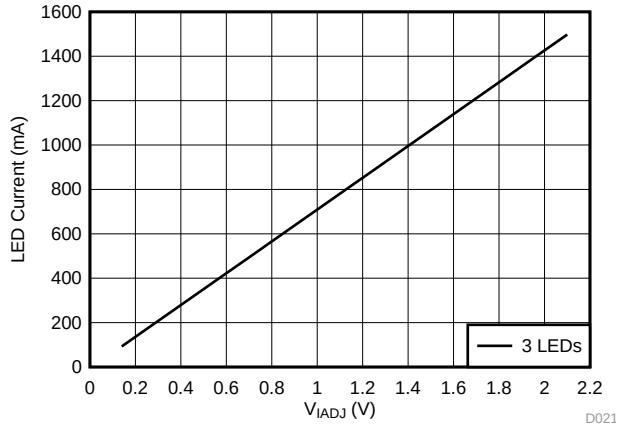
The closest standard values of 150 kΩ and 4.12 kΩ along with a 60-V PNP transistor are used to set the OVP threshold to 45 V with 3 V of hysteresis.

9.2.2.2.15 Direct PWM Dimming Consideration

A 60-V, 2-A P-channel FET is used to achieve series FET PWM dimming.

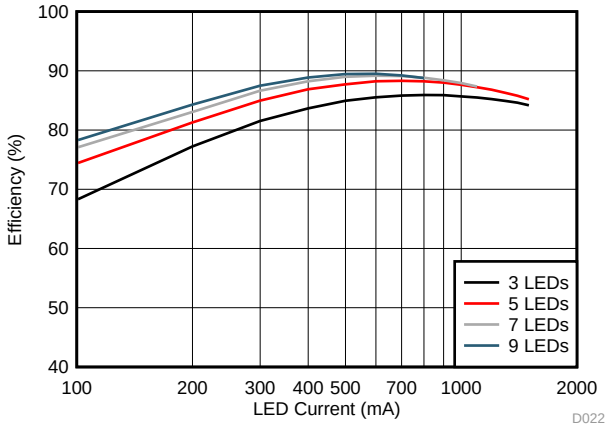
9.2.2.3 Application Curves

These curves are for the buck-boost LED driver.



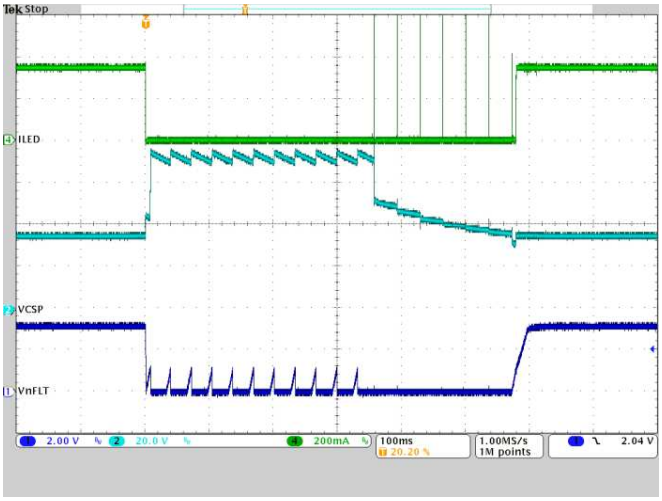
V_{IN} = 14 V

Figure 55. LED Current vs IADJ Voltage



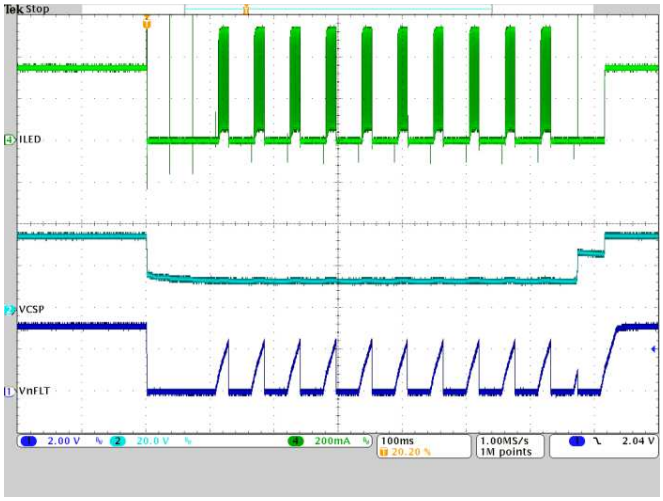
V_{IN} = 14 V

Figure 56. Efficiency



Ch1: $\overline{FLT}$ output;
Ch2: CSP pin voltage;
Ch4: LED current; Time: 100 ms/div

Figure 57. LED Open-Circuit Fault



Ch1: $\overline{FLT}$ output;
Ch2: CSP pin voltage;
Ch4: LED current; Time: 100 ms/div

Figure 58. LED Short-Circuit Fault

10 Power Supply Recommendations

This device is designed to operate from an input voltage supply range between 4.5 V and 65 V. The input could be a car battery or another preregulated power supply. If the input supply is located more than a few inches from the TPS92692 or TPS92692-Q1 device, additional bulk capacitance or an input filter may be required in addition to the ceramic bypass capacitors to address noise and EMI concerns.

11 Layout

11.1 Layout Guidelines

- The performance of the switching regulator depends as much on the layout of the PCB as the component selection. Following a few simple guidelines will maximize noise rejection and minimize the generation of EMI within the circuit.
- Discontinuous currents are the most likely to generate EMI. Therefore, take care when routing these paths. The main path for discontinuous current in the devices using a buck regulator topology contains the input capacitor, C_{IN}, the recirculating diode, D, the N-channel MOSFET, Q1, and the sense resistor, R_{IS}. In the TPS92692 and TPS92692-Q1 devices using a boost regulator topology, the discontinuous current flows through the output capacitor C_{OUT}, diode, D, N-channel MOSFET, Q1, and the current sense resistor, R_{IS}. In devices using a buck-boost regulator topolog. Be careful when laying out both discontinuous loops. Ensure that these loops are as small as possible. In order to minimize parasitic inductance, ensure that the connection between all the components are short and thick. In particular, make the switch node (where L, D, and Q1 connect) just large enough to connect the components. To minimize excessive heating, large copper pours can be placed adjacent to the short current path of the switch node.
- Route the CSP and CSN together with Kelvin connections to the current sense resistor with traces as short as possible. If needed, use common mode and differential mode noise filters to attenuate switching and diode reverse recovery noise from affecting the internal current sense amplifier.
- Because the COMP, IS, OV, DIM/PWM, and IADJ pins are all high-impedance inputs that couple external noise easily, ensure that the loops containing these nodes are minimized whenever possible.
- In some applications, the LED or LED array can be far away from the TPS92692 and TPS92692-Q1 devices, or on a separate PCB connected by a wiring harness. When an output capacitor is used and the LED array is large or separated from the rest of the regulator, place the output capacitor close to the LEDs to reduce the effects of parasitic inductance on the AC impedance of the capacitor.
- The TPS92692 and TPS92692-Q1 devices have an exposed thermal pad to aid power dissipation. Adding several vias under the exposed pad helps conduct heat away from the device. The junction-to-ambient thermal resistance varies with application. The most significant variables are the area of copper in the PCB and the number of vias under the exposed pad. The integrity of the solder connection from the device exposed pad to the PCB is critical. Excessive voids greatly decrease the thermal dissipation capacity.

11.2 Layout Example

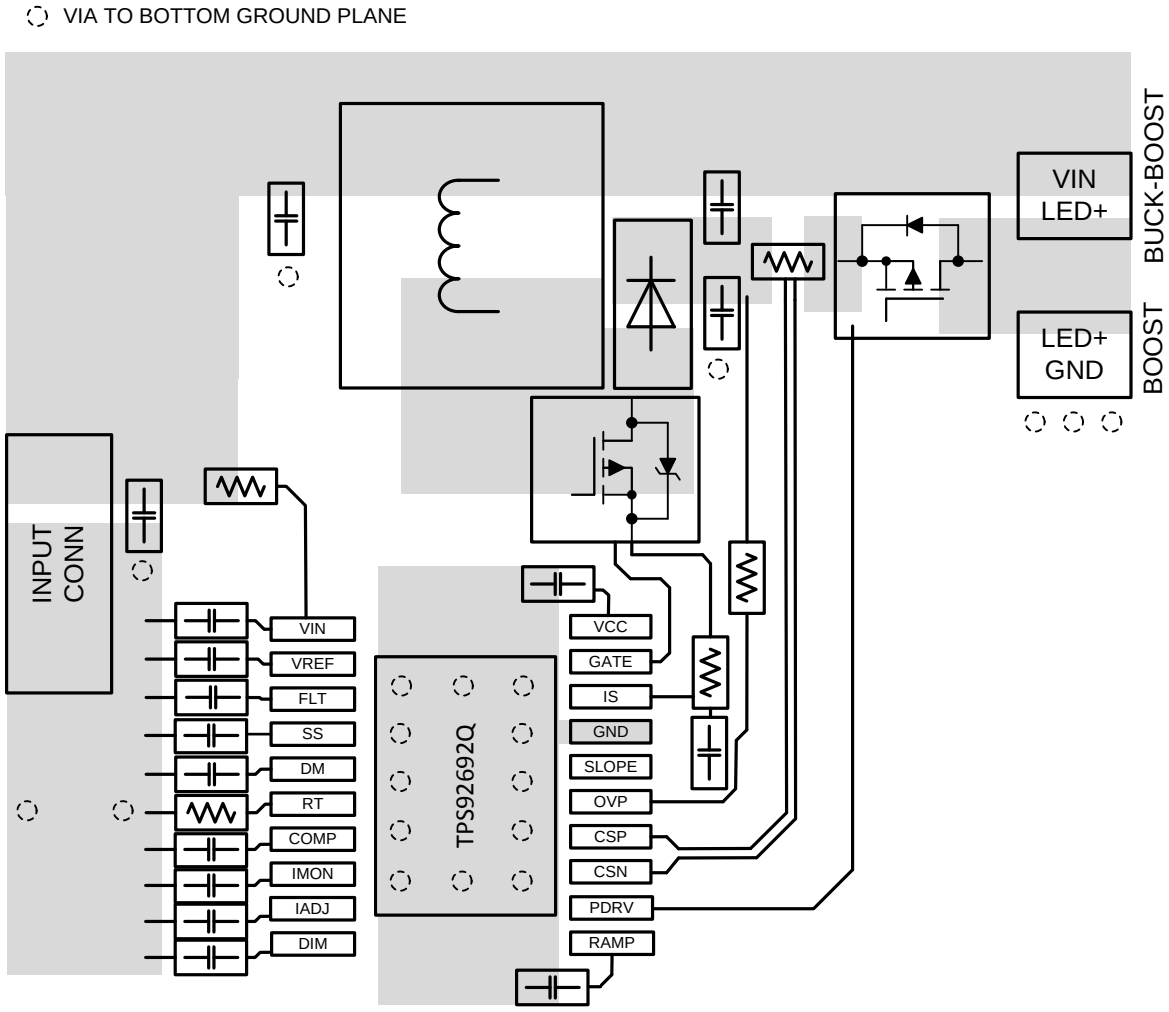


Figure 59. Layout Recommendation

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 7. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS92692	Click here	Click here	Click here	Click here	Click here
TPS92692-Q1	Click here	Click here	Click here	Click here	Click here

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92692PWPR	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	92692	Samples
TPS92692PWPT	ACTIVE	HTSSOP	PWP	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	92692	Samples
TPS92692QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	92692Q	Samples
TPS92692QPWPTQ1	ACTIVE	HTSSOP	PWP	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	92692Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS92692, TPS92692-Q1 :

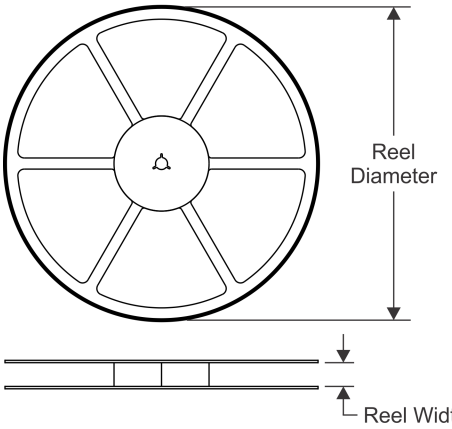
- Catalog: TPS92692
- Automotive: TPS92692-Q1

NOTE: Qualified Version Definitions:

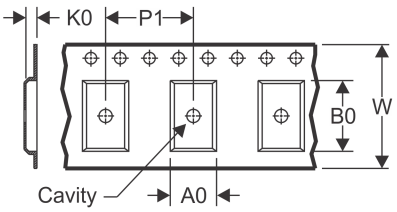
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

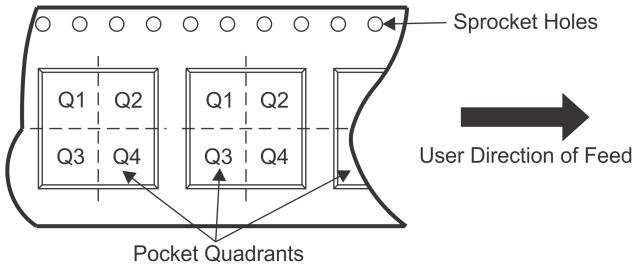


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



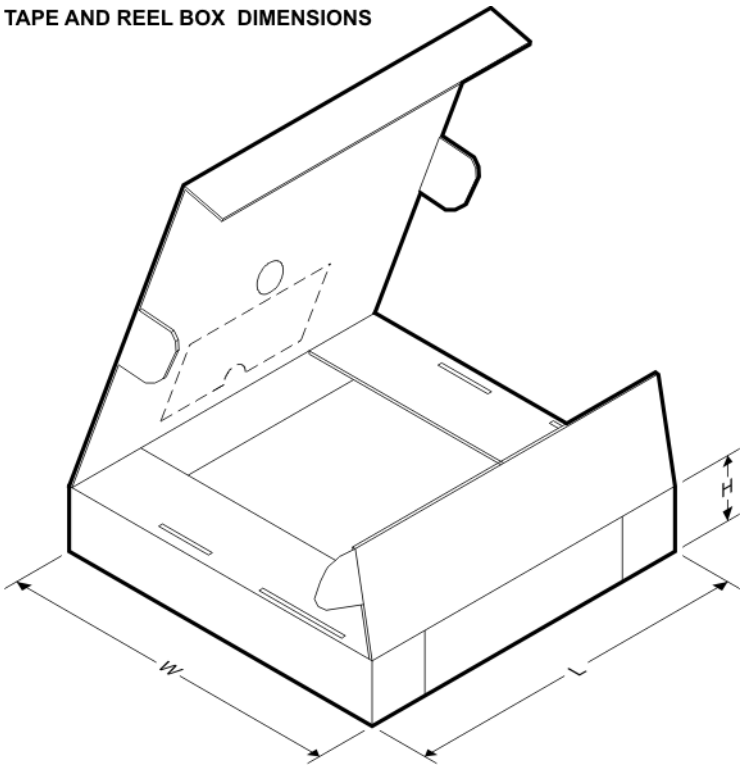
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92692PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS92692QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

1-Sep-2021

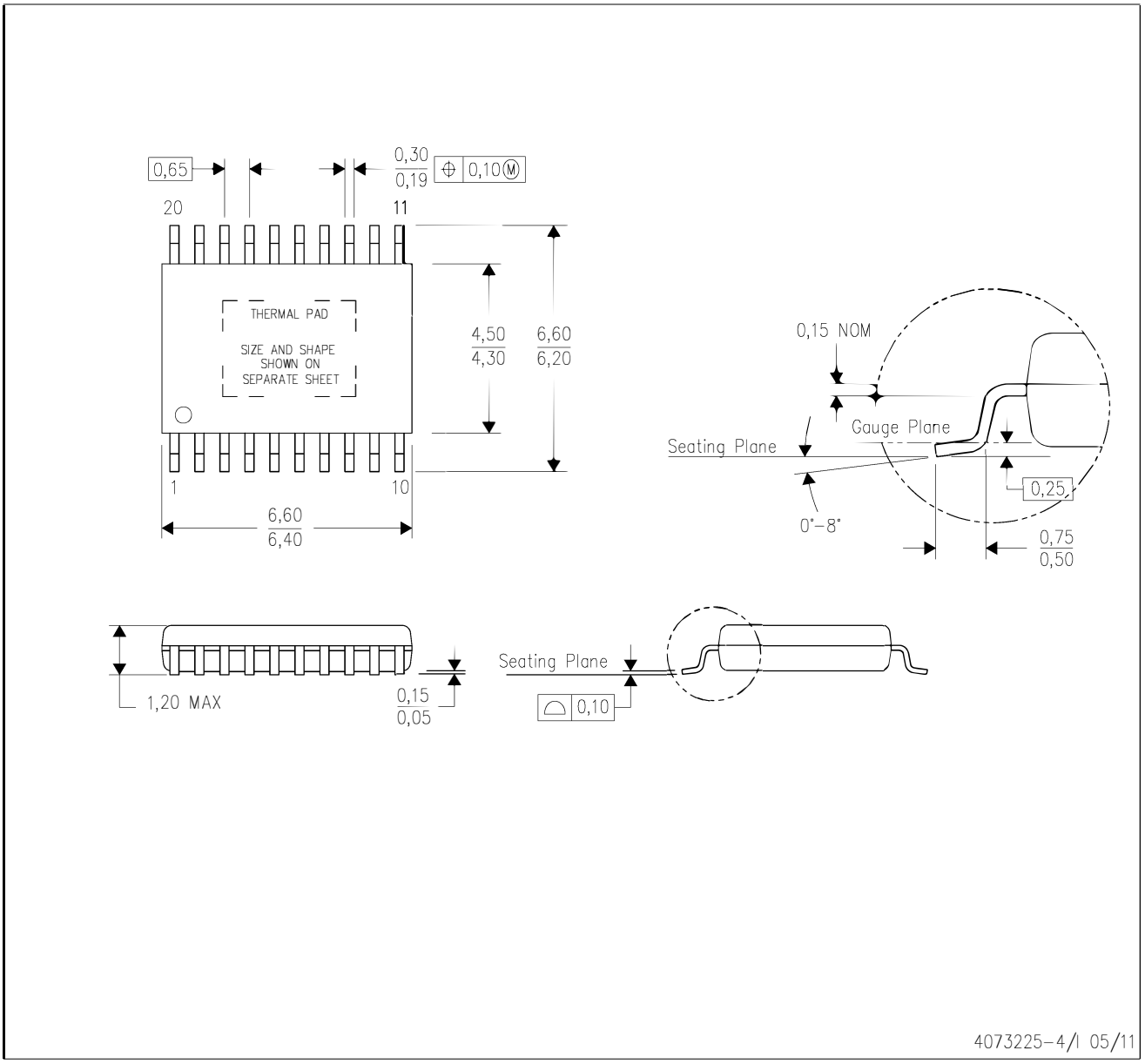
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92692PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS92692QPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

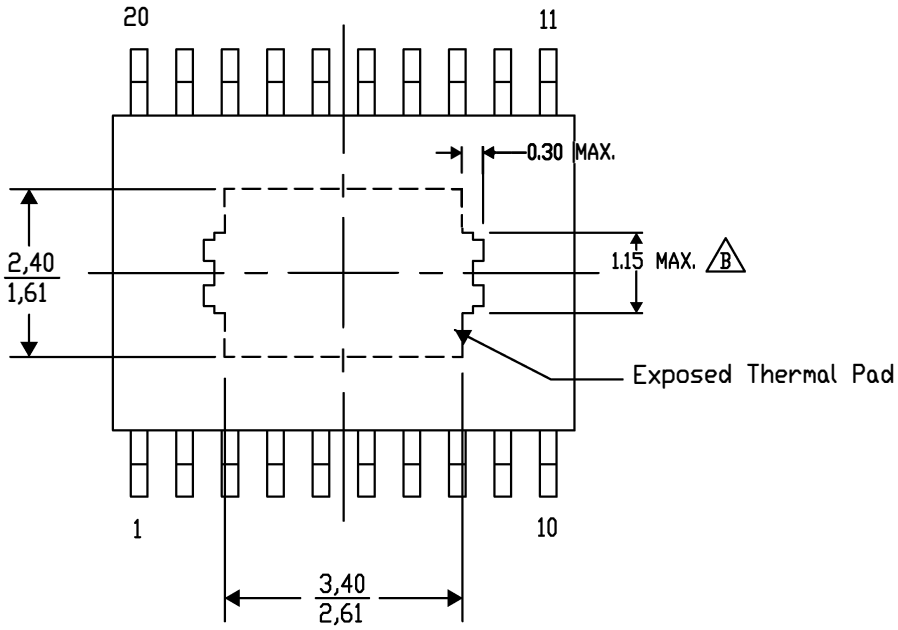
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

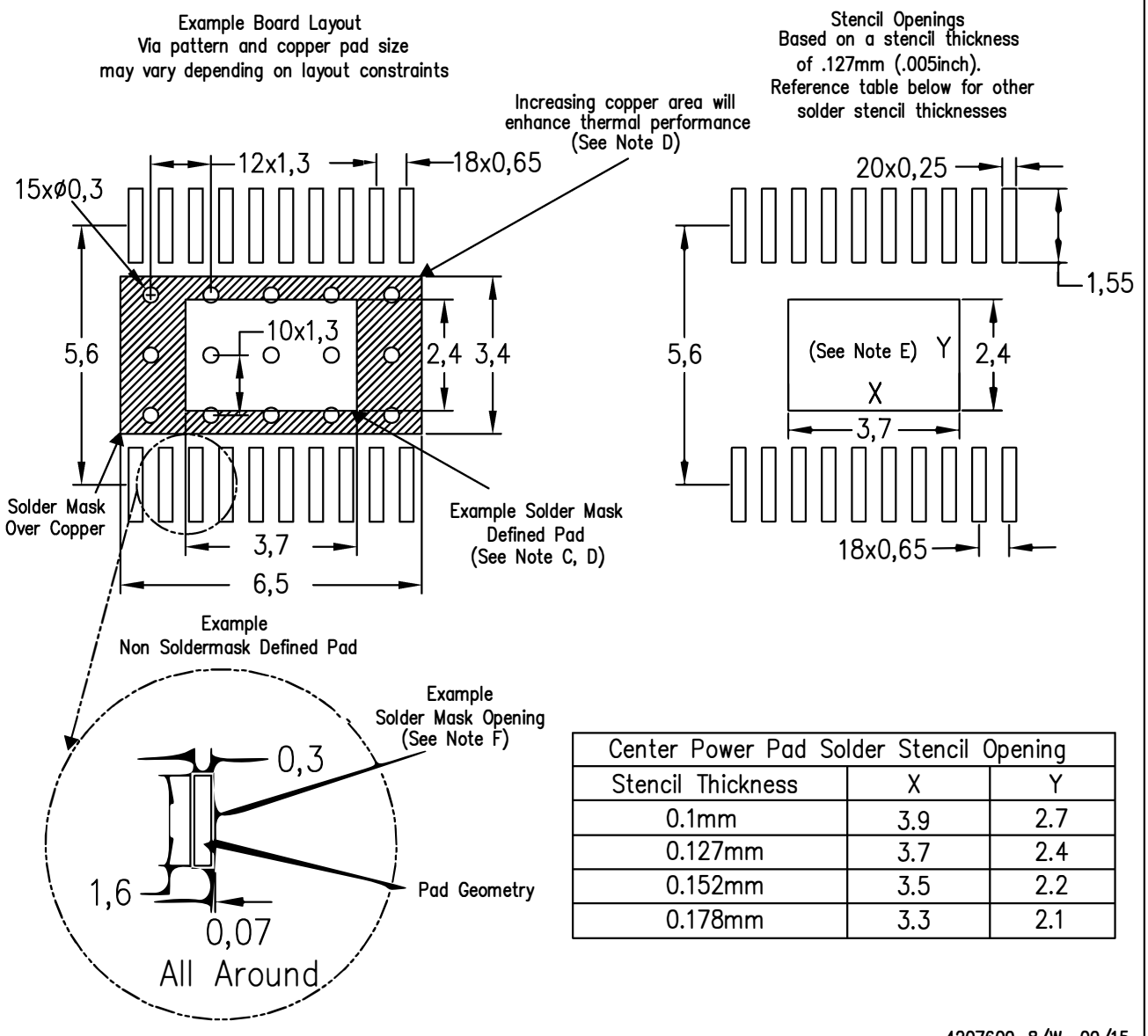
4206332–15/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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