SGM3775Q
Automotive High Accuracy LED Controller with Spread Spectrum Frequency Modulation

GENERAL DESCRIPTION

The SGM3775Q is a peak current mode, asynchronous controller for LED lights. The device supports Boost, Buck-Boost, SEPIC and Flyback configurations to meet multi-purpose applications. The SGM3775Q features a wide 4.5V to 65V input voltage range and supports up to 65V output voltage.

The switching frequency can be set by the RT pin, or it can be synchronized by an external clock signal. The configurable frequency spread spectrum function is available to improve EMI performance.

The SGM3775Q provides both analog dimming and PWM dimming methods to modulate LED current independently. Adjust the IADJ input to set the regulated LED current with over 15:1 contrast ratio, and adjust the DIM/PWM input to get a dimming range over 1000:1. The PDRV output is used to drive an external optional P-Channel MOSFET, which provides the fast response to the PWM signal.

The device provides full protections including LED over-current, output over-voltage, output under-voltage, switch current limit, and thermal shutdown protections. The nFLT open-drain output indicates the logic low when fault occurs. The IMON output provides extra continuous LED current monitor, connecting IMON to external microcontroller for fault detection if necessary.

The device is AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and it is suitable for automotive applications.

The device is available in a Green TSSOP-20A (Exposed Pad) package.

FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
  Device Temperature Grade 1
  T_A = -40℃ to +125℃
- **4.5V to 65V Wide Input Voltage Range**
- **Programmable Switching Frequency**
- **Support External Synchronized Frequency**
- **Frequency Spread Spectrum**
- **External Analog Dimming via IADJ Pin**
- **External PWM Dimming via DIM/PWM Pin**
- **Integrated P-Channel Dimming MOSFET Driver**
- **Flexible External Loop Compensation**
- **Flexible External Slope Compensation**
- **Support Boost, Buck-Boost, SEPIC and Flyback Topologies**
- **Short LED Protection**
- **Open LED Protection**
- **Thermal Shutdown**
- **Fault Indicator**
- **High LED Current Accuracy (< ±10%) over -40℃ to +150℃ Junction Temperature Range**
- **Available in a Green TSSOP-20A (Exposed Pad) Package**

APPLICATIONS

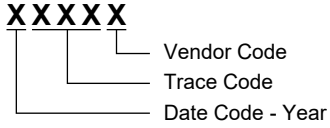
LED General Lighting Applications
Automotive Exterior Lighting Applications
Driver Monitoring Systems (DMS)
Exit Signs and Emergency Lighting

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM3775Q	TSSOP-20A (Exposed Pad)	-40℃ to +125℃	SGM3775QPTS20G/TR	SGM0I9PTS20 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS (1)

VIN, CSP, CSN Voltages ..... -0.3V to 65V
DIM/PWM Voltage ..... -0.3V to 14V
IS, RT Voltages ..... -0.3V to 8.8V
nFLT Voltage ..... -0.3V to 6.0V
OV, SS, RAMP, DM, SLOPE, VREF, IADJ ..... -0.3V to 5.5V
CSP to CSN Voltage (2) ..... -0.3V to 0.3V
VCC, GATE Voltages (3) ..... -0.3V to 8.8V
PDRV Voltage (3) ..... V_{CSP} - 8.8V to V_{CSP}
COMP Voltage (3) ..... -0.3V to 5.0V
Package Thermal Resistance
TSSOP-20A (Exposed Pad), θ_{JA} ..... 32.8℃/W
TSSOP-20A (Exposed Pad), θ_{JB} ..... 16.2℃/W
TSSOP-20A (Exposed Pad), $\theta_{JC\ (TOP)}$ ..... 27.9℃/W
TSSOP-20A (Exposed Pad), $\theta_{JC\ (BOT)}$ ..... 3.2℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (4) (5)
HBM ..... ±2000V
CDM ..... ±1000V

NOTES:

1. All voltages are with reference to GND unless otherwise noted.

2. Continuous sustaining voltage.

3. All output pins are not specified to have an external voltage applied.

4. For human body model (HBM), all pins comply with AEC-Q100-002 specification.

5. For charged device model (CDM), all pins comply with AEC-Q100-011 specification.

RECOMMENDED OPERATING CONDITIONS

Input Supply Voltage, V_{IN} ..... 6.5V to 65V
Input Supply Battery Crank Voltage, V_{IN_CRACK} ..... 4.5V (MIN)
Current-Sense Common Mode, V_{CSP}, V_{CSN} ..... 6.5V to 60V
Switching Frequency, f_{SW} ..... 80kHz to 700kHz
Spread Spectrum Modulation Frequency, f_M ..... 0.1kHz to 12kHz
Internal PWM Ramp Generator Frequency, f_{RAMP} ..... 100Hz to 2000Hz
Current Reference Voltage, V_{IADJ} ..... 0.14V to V_{IADJ_CLAMP}
Operating Junction Temperature Range ..... -40℃ to +150℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

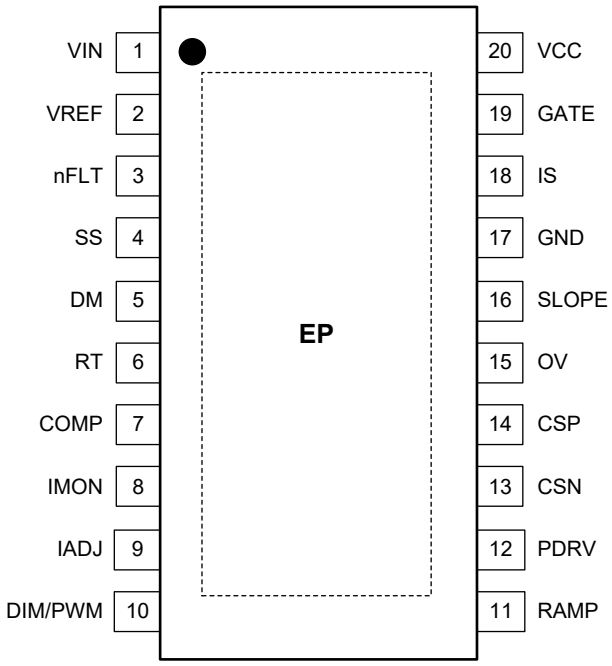
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TSSOP-20A (Exposed Pad)

PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
1	VIN	—	Power Supply Input. Connect a low pass filter with 10Ω resistor and 10nF capacitor from VIN pin to GND to reduce the noise.
2	VREF	—	4.96V Bias Supply Pin. VREF is used to power the internal logic circuit. Connect an external 2.2μF bypass ceramic capacitor from VREF pin to GND.
3	nFLT	O	Fault Flag Indicator Output. The nFLT is an active-low, open-drain output. Connect an external pull-up resistor to this pin.
4	SS	I/O	Soft-Start Configuration Pin. Connect a capacitor to GND to program the start-up time. Pulling SS pin to GND can disable the switching.
5	DM	I/O	Spread Spectrum Modulation Frequency Configuration Pin. Program the spread spectrum modulation frequency by the capacitor between DM pin to GND. Disable the spread spectrum modulation function if pull down this pin to GND.
6	RT	I/O	Oscillator Frequency Configuration Pin. Program the converter switching frequency by the resistor between RT pin to GND. The switching frequency also can be synchronized to external clock from RT pin.
7	COMP	I/O	Compensation Connection. The COMP pin is the internal error amplifier's output. Connect a compensation network to this pin for system stability.
8	IMON	O	LED Current Monitor Pin. The IMON pin voltage is V_{IMON} = 14.1 × I_{LED} × R_{CS}. Connect a 1nF bypass ceramic capacitor from this pin to GND.

PIN DESCRIPTION (continued)

PIN	NAME	I/O	FUNCTION
9	IADJ	I	LED Current Adjust Input. Set this pin from 140mV to 2.31V to adjust the LED current reference voltage for analog dimming. Pull up IADJ pin to VREF pin through a 100kΩ resistor to set the current-sense reference $V_{CSP-CSN}$ to the maximum value of 176mV.
10	DIM/PWM	I	External PWM Dimming Input. The external analog or PWM command is used to generate an internal PWM signal to control the LED on duty cycle. When the external analog voltage is applied, the voltage compares the internal 0.96V to 2.88V triangle signal and then generates the internal PWM duty cycle. When disable the internal triangle and apply the external PWM signal to DIM/PWM pin, the internal PWM duty cycle and frequency are the same as the external PWM signal. During the PWM off period, the GATE and PDRV pins are off. The COMP pin is disconnected for fast response when PWM is on. If PWM dimming is not required, connect the DIM/PWM pin to VREF pin for internal PWM signal 100% duty cycle.
11	RAMP	I/O	Internal PWM Generator Frequency Configuration Pin. When the external analog voltage is applied on DIM/PWM pin, program the internal PWM signal frequency by the capacitor between the RAMP pin and GND. When the external PWM signal is applied on DIM/PWM pin, connect a 249kΩ resistor between RAMP pin and GND to get the same internal PWM frequency and duty cycle as the external PWM signal. Do not leave this pin floating.
12	PDRV	O	Dimming P-Channel MOSFET Gate Driver Output. If the dimming P-channel MOSFET is connected, the PDRV pin drives the external P-channel MOSFET as a dimming switch. Float PDRV pin if the external P-channel MOSFET is not connected.
13	CSN	I	High-side LED Current-Sense Negative Input.
14	CSP	I	High-side LED Current-Sense Positive Input.
15	OV	I	Output Voltage Sense Input. When this pin voltage is above 1.176V (TYP) or below 95.4mV (TYP), the device takes over-voltage or under-voltage protection actions respectively. Connecting the required resistor divider from LED voltage to GND can program the protection threshold.
16	SLOPE	I/O	Slope Compensation Configuration Pin. Connect a resistor from SLOPE pin to GND based on R_{IS} and inductor value to set the proper slope compensation.
17	GND	—	Power and Analog GND Pin. Separate the power loop ground and analog signal ground, and then connect them together at GND pin.
18	IS	I	Switch Current-Sense Pin. Sense the switch current via R_{IS} to generate the internal PWM comparator and control GATE output off.
19	GATE	O	N-Channel MOSFET Gate Driver Output. Connect this pin to the gate of external N-channel MOSFET.
20	VCC	—	7.5V (TYP) Bias Supply Pin. VCC pin is used to driver the external MOSFET. Connect an external 2.2μF bypass ceramic capacitor from VCC pin to GND.
Exposed Pad	—	—	Connect the Exposed Pad to GND pin together, and place some vias under the exposed pad to help the thermal dissipation.

NOTE: I: input, O: output, I/O = input/output.

TYPICAL APPLICATION

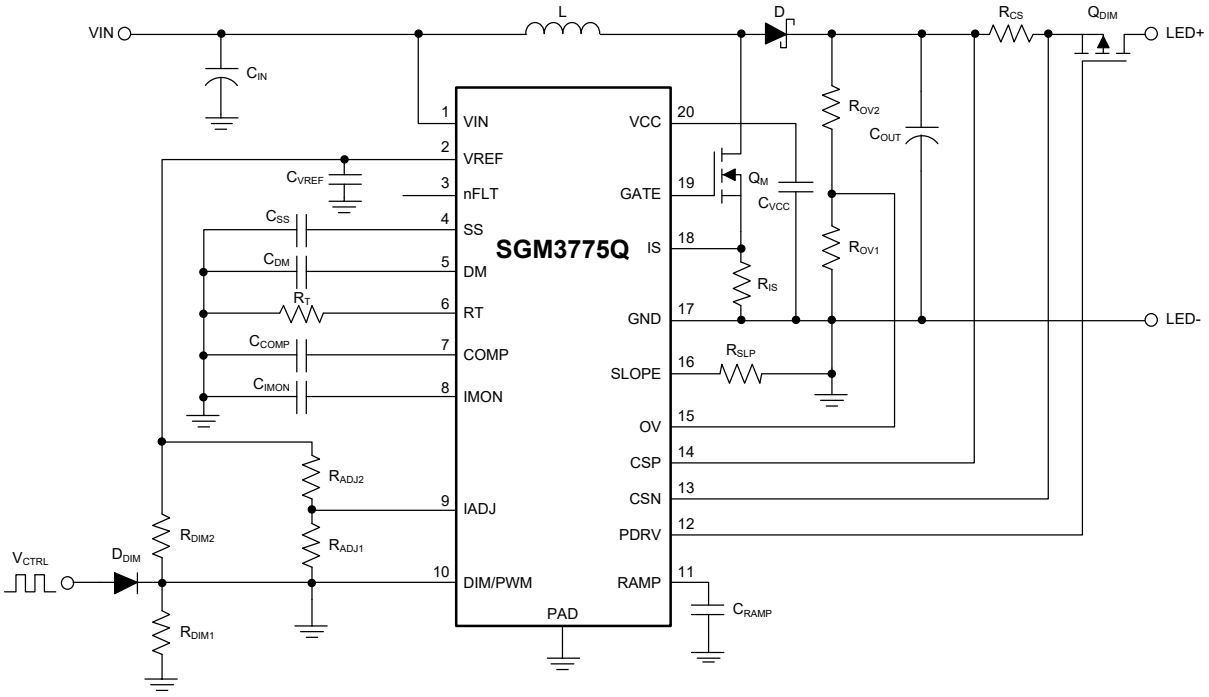


Figure 1. Typical Boost LED Driver

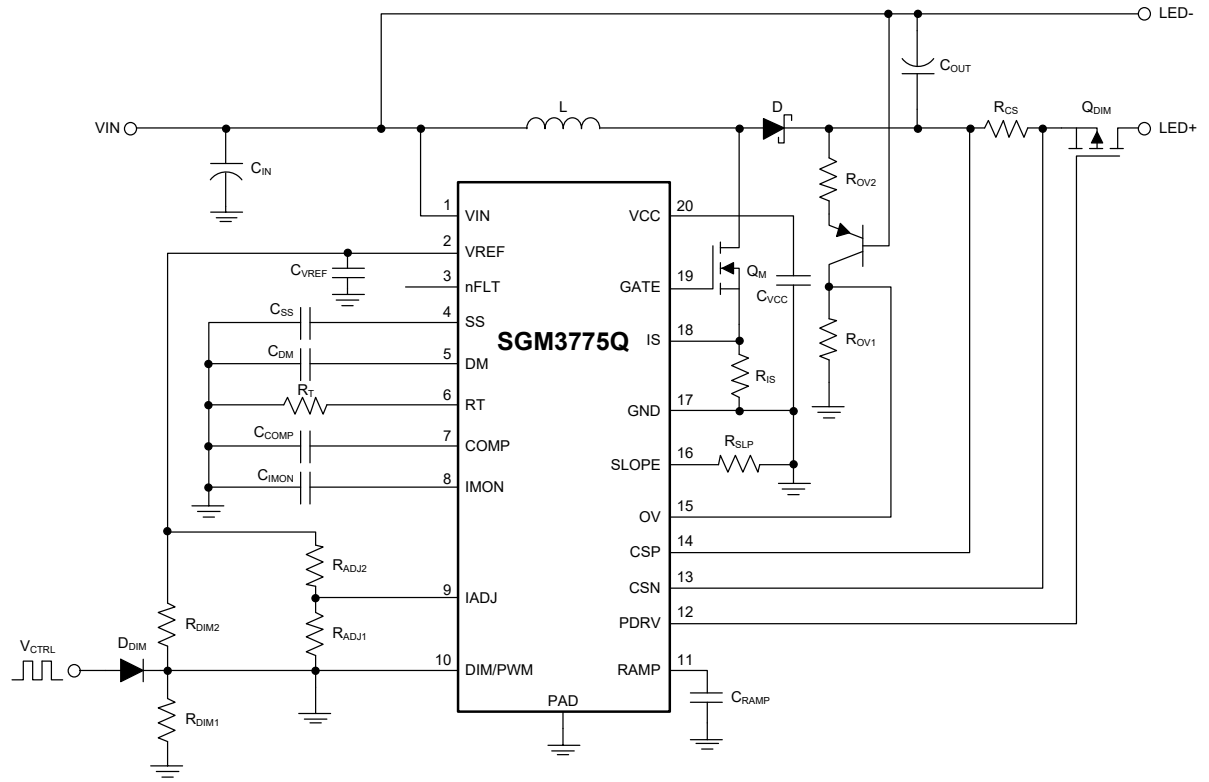


Figure 2. Buck-Boost LED Driver

TYPICAL APPLICATION (continued)

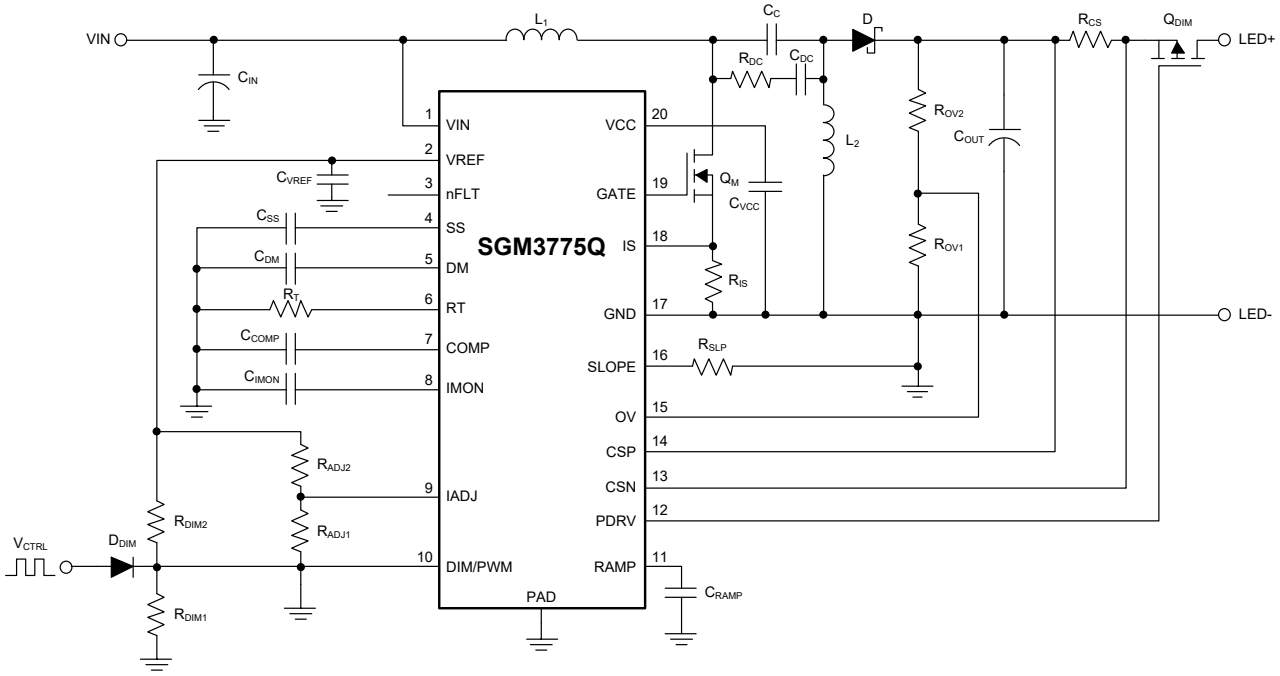


Figure 3. SEPIC LED Driver

ELECTRICAL CHARACTERISTICS

(V_{IN} = 14V, V_{IADJ} = 2.1V, V_{RAMP} = 500mV, $V_{DIM/PWM}$ = 3V, V_{OV} = 500mV, C_{VCC} = 1μF, C_{VREF} = 1μF, C_{COMP} = 2.2nF, R_{CS} = 100mΩ, R_T = 20kΩ, no load on GATE and PDRV, T_J = -40℃ to +150℃, all typical values are measured at T_A = +25℃, unless otherwise noted. (1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage (VIN)						
Input Standby Current	I_{IN_STBY}	V_{PWM} = 0V		1.1	1.7	mA
Input Switching Current	I_{IN_SW}	V_{CC} = 7.5V, C_{GATE} = 1nF		3.1	4.0	mA
Bias Supply (VCC)						
Regulation Voltage	V_{CC_REG}	No load	7.1	7.5	7.8	V
Supply Under-Voltage Protection	V_{CC_UVLO}	VCC rising threshold, V_{IN} = 8V		4.5	4.9	V
		VCC falling threshold, V_{IN} = 8V	3.7	4.1		V
	V_{CC_HYS}	Hysteresis		400		mV
Supply Current Limit	I_{CC_LIMIT}	V_{CC} = 0V	23	39	55	mA
LDO Dropout Voltage	V_{DO}	I_{CC} = 20mA, V_{IN} = 5V		320		mV
Reference Voltage (VREF)						
Reference Voltage	V_{REF}	No load	4.77	4.96	5.15	V
Current Limit	I_{REF_LIMIT}	V_{REF} = 0V	23	39	55	mA
Oscillator (RT)						
Switching Frequency	f_{SW}	R_T = 40kΩ	180	200	220	kHz
		R_T = 20kΩ	350	385	420	kHz
RT Output Voltage	V_{RT}		0.9	1.0	1.1	V
SYNC Rising Threshold	V_{SYNC}	V_{RT} rising		2.4	3.1	V
SYNC Falling Threshold		V_{RT} falling	1.80	1.92		V
Minimum SYNC Clock Pulse Width (2)	t_{SYNC_MIN}			100		ns
Spread Spectrum Frequency Modulation (DM)						
Triangle Wave Generator Sink Current	I_{DM}			10		μA
Triangle Wave Generator Source Current				10		μA
Triangle Wave Voltage Peak (High)	V_{DM_TR}		1.0	1.1	1.2	V
Triangle Wave Voltage Valley (Low)			0.77	0.82	0.86	V
Spread Spectrum Modulation Enable Threshold	V_{DM_EN}		0.60	0.67	0.75	V
Internal Clamp Voltage	V_{DM_CLAMP}	V_{PWM} = 0V, R_{RAMP} = 200kΩ	1.13	1.20	1.29	V
Gate Driver (GATE)						
Gate Driver High-side Resistance	R_{GH}	I_{GATE} = -10mA		6.8	13.0	Ω
Gate Driver Low-side Resistance	R_{GL}	I_{GATE} = 10mA		5.6	10.7	Ω
Current Sense (IS)						
Current Limit Threshold	V_{IS_LIMIT}	$V_{DIM/PWM}$ = 5V, R_{RAMP} = 249kΩ	220	240	270	mV
		$V_{DIM/PWM}$ = 0V, R_{RAMP} = 249kΩ	650	670	710	mV
Leading Edge Blanking Time (2)	t_{IS_BLANK}			118		ns
Current Limit Fault Time (2)	t_{IS_FAULT}			35		μs
IS to GATE Propagation Delay (2)	t_{ILMT_DLY}	V_{IS} pulsed from 0V to 1V		80		ns
PWM Comparator and Slope Compensation (SLOPE)						
Maximum Duty Cycle	D_{MAX}		88.0	90.6		%
Adaptive Slope Compensation	V_{SLOPE}	V_{CSP} = 24V		404		mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 14V, V_{IADJ} = 2.1V, V_{RAMP} = 500mV, $V_{DIM/PWM}$ = 3V, V_{OV} = 500mV, C_{VCC} = 1μF, C_{VREF} = 1μF, C_{COMP} = 2.2nF, R_{CS} = 100mΩ, R_T = 20kΩ, no load on GATE and PDRV, T_J = -40℃ to +150℃, all typical values are measured at T_A = +25℃, unless otherwise noted. (1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Slope Compensation Output Voltage	V_{SLOPE_MIN}	V_{CSP} = 0V		96		mV
IS to COMP Level Shift Voltage	V_{LV}	No slope compensation added	1.28	1.44	1.60	V
IS Level Shift Bias Current	I_{LV}	No slope compensation added		15		μA
Current-Sense Amplifier (CSP, CSN)						
Current-Sense Thresholds	$V_{CSP-CSN}$	V_{CSP} = 14V, V_{IADJ} = 3V	155	163.2	176	mV
		V_{CSP} = 14V, V_{IADJ} = 1.4V	93	99.13	110	mV
Current-Sense Unity Gain Bandwidth (2)	BW_{CS}			1.0		MHz
Current-Sense Amplifier Gain	G_{CS}	G = $V_{IADJ}/V_{CSP-CSN}$		14.1		
Ratio of Over-Current Detection Threshold to Analog Adjust Voltage	K_{OCP}	K_{OCP} = $V_{OCP-THR}/V_{IADJ}$	1.40	1.50	1.61	
CSP Bias Current	I_{CSP_BIAS}	V_{CSN} = 14.1V, V_{CSP} = 14V		106		μA
CSN Bias Current	I_{CSN_BIAS}	V_{CSN} = 14.1V, V_{CSP} = 14V		67		μA
Fault Indicator (nFLT)						
Open-Drain Pull-Down Resistance	R_{FLT}			208		Ω
Fault Timer (2)	t_{FAULT_TMR}		23	38	66	ms
Current Monitor (IMON)						
IMON Source Current	I_{IMON_SRC}	$V_{CSP-CSN}$ = 150mV, V_{IMON} = 0V		101	140	μA
IMON Output Voltage Clamp	V_{IMON_CLP}		3.30	3.54	3.78	V
IMON Buffer Offset Voltage	V_{IMON_OS}		-16	3.5	16	mV
Analog Adjust (IADJ)						
IADJ Internal Clamp Voltage	V_{IADJ_CLP}	I_{IADJ} = 1μA	2.19	2.31	2.45	V
IADJ Input Bias Current	I_{IADJ_BIAS}	V_{IADJ} < 2.2V		3		nA
IADJ Current Limiting Series Resistor	R_{IADJ_LMT}	V_{IADJ} > 2.6V		12		kΩ
Error Amplifier (COMP)						
Transconductance	g_M			117		μA/V
COMP Current Source Capacity	I_{COMP_SRC}	V_{IADJ} = 1.4V, $V_{CSP-CSN}$ = 0V		127		μA
COMP Current Sink Capacity	I_{COMP_SINK}	V_{IADJ} = 0V, $V_{CSP-CSN}$ = 0.1V		127		μA
Error Amplifier Bandwidth (2)	BW_{EA}	Gain = -3dB		5		MHz
COMP Pin Reset Voltage	V_{COMP_RST}			96		mV
COMP Discharge FET Resistance	R_{COMP_DCH}			240		Ω
Soft-Start (SS)						
Soft-Start Source Current	I_{SS}		7.5	10.1	12.5	μA
Soft-Start Voltage Threshold to Enable Output Under-Voltage Protection	$V_{SS_UVP_EN}$			2.3		V
Soft-Start Pin Reset Voltage	V_{SS_RST}			47		mV
SS Discharge FET Resistance	R_{SS_DCH}			210		Ω
Output Voltage Input (OV)						
Over-Voltage Protection Threshold	V_{OVP_THR}		1.130	1.176	1.228	V
Under-Voltage Protection Threshold	V_{UVP_THR}		73.0	95.4	118.0	mV
Under-Voltage Protection Blanking Period (2)	$t_{UVP-BLANK}$			4.0		μs
OVP Hysteresis Current	I_{OVP_HYS}		15.0	20.1	25.5	μA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 14V, V_{IADJ} = 2.1V, V_{RAMP} = 500mV, $V_{DIM/PWM}$ = 3V, V_{OV} = 500mV, C_{VCC} = 1μF, C_{VREF} = 1μF, C_{COMP} = 2.2nF, R_{CS} = 100mΩ, R_T = 20kΩ, no load on GATE and PDRV, T_J = -40℃ to +150℃, all typical values are measured at T_A = +25℃, unless otherwise noted. (1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Internal PWM Ramp Generator (RAMP)						
Ramp Generator Source Current	I_{RAMP}		7.8	10.2	12.8	μA
Ramp Generator Sink Current			7.5	10.1	12.5	μA
Ramp Signal Peak (High)	V_{RAMP}			2.88		V
Ramp Signal Valley (Low)				0.96		V
PWM Input (DIM/PWM)						
Schmitt Trigger Logic Level (High Threshold)	V_{PWM_HIGH}	V_{RAMP} = 2.0V		2.0	2.2	V
Schmitt Trigger Logic Level (Low Threshold)	V_{PWM_LOW}	V_{RAMP} = 2.0V	1.8	2.0		V
PWM Pull-Down Resistance	R_{PWM_PD}			9.6		MΩ
PWM Rising to PDRV Delay (2)	t_{DLY_RISE}	C_{PDRV} = 1nF		250		ns
PWM Falling to PDRV Delay (2)	t_{DLY_FALL}	C_{PDRV} = 1nF		160		ns
Series P-Channel PWM FET Gate Drive Output (PDRV)						
P-Channel Gate Driver Off-State Voltage	V_{PDRV_OFF}	V_{CSP} = 14V		14.0		V
P-Channel Gate Driver On-State Voltage	V_{PDRV_ON}	V_{CSP} = 14V		7.43		V
PDRV Sink Current (2)	I_{PDRV_SRC}	Pulsed 4μs		100		mA
PDRV Driver Pull-Up Resistance	R_{PDRV_L}			104		Ω
Thermal Shutdown						
Thermal Shutdown Temperature	T_{SD}			160		℃
Thermal Shutdown Hysteresis	T_{SD_HYS}			15		℃

NOTES:

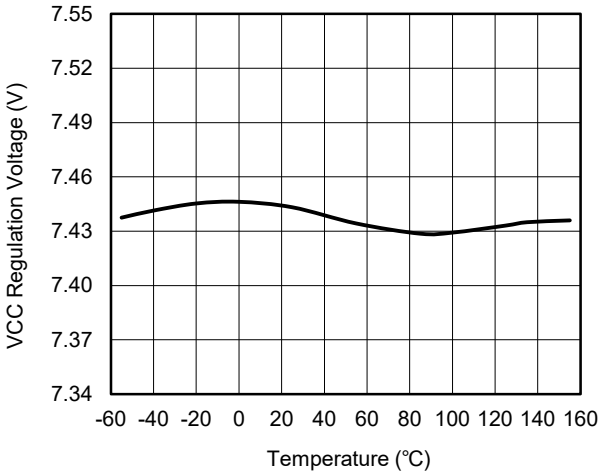
1. All voltages are related to GND unless otherwise noted.

2. Specified by design and characterization, not production tested.

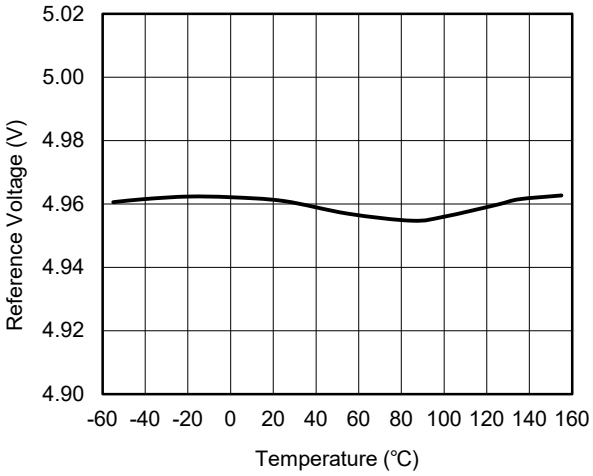
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{IN} = 14V, V_{IADJ} = 2.2V, C_{VCC} = 1μF, C_{COMP} = 2.2nF, R_{CS} = 100mΩ, R_T = 20kΩ, V_{PWM} = 5V, no load on GATE and PDRV, unless otherwise noted.

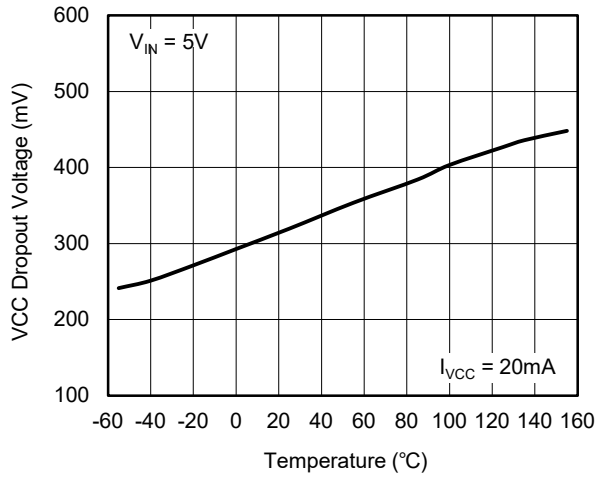
VCC Regulation Voltage vs. Temperature



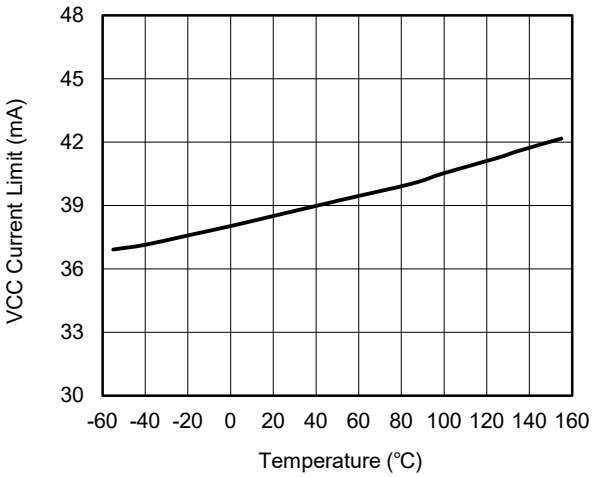
Reference Voltage vs. Temperature



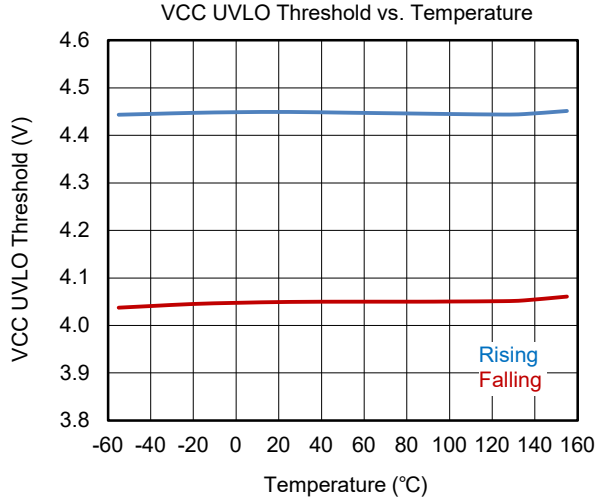
VCC Dropout Voltage vs. Temperature



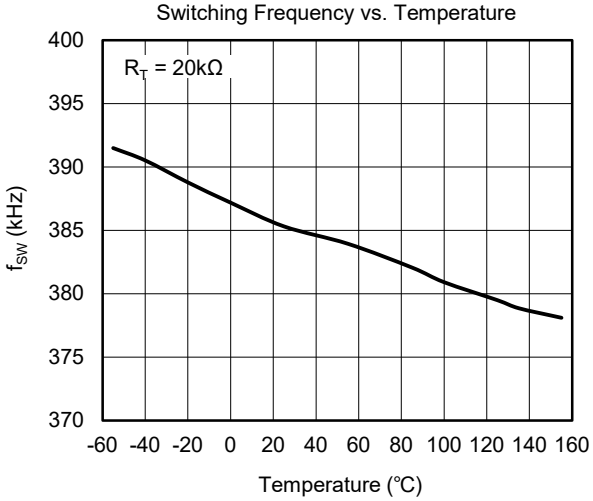
VCC Current Limit vs. Temperature



VCC UVLO Threshold vs. Temperature



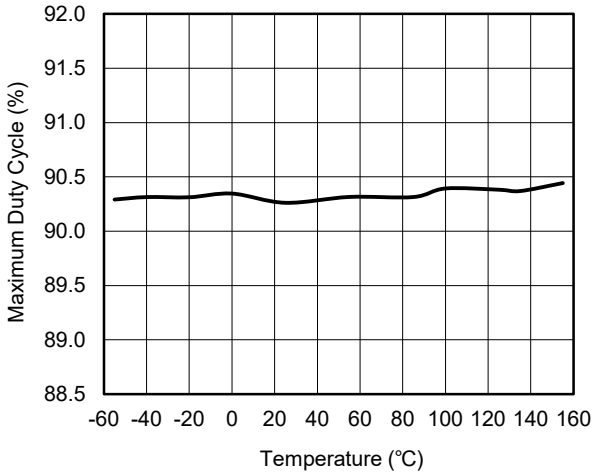
Switching Frequency vs. Temperature



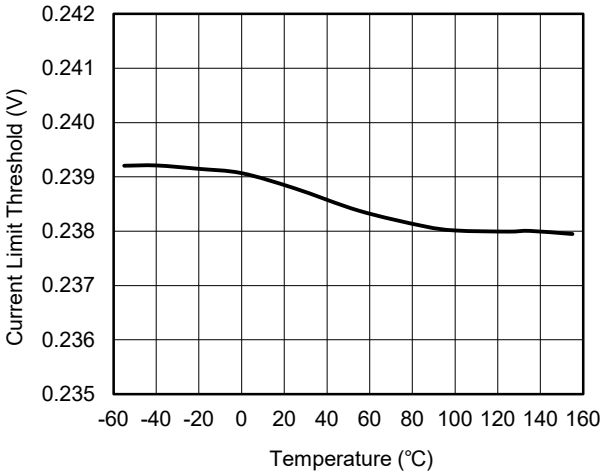
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 14V, V_{IADJ} = 2.2V, C_{VCC} = 1μF, C_{COMP} = 2.2nF, R_{CS} = 100mΩ, R_T = 20kΩ, V_{PWM} = 5V, no load on GATE and PDRV, unless otherwise noted.

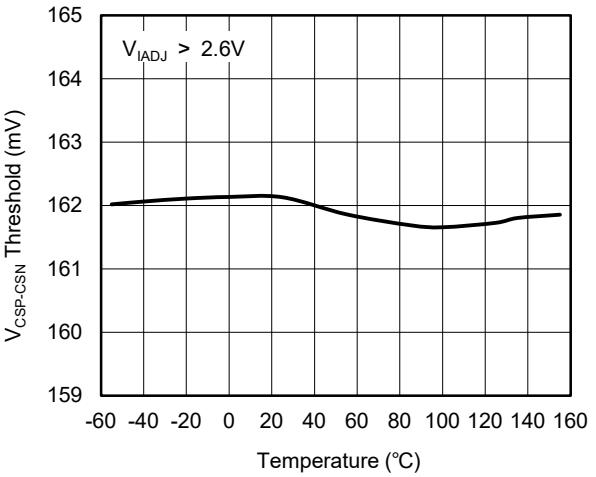
Maximum Duty Cycle vs. Temperature



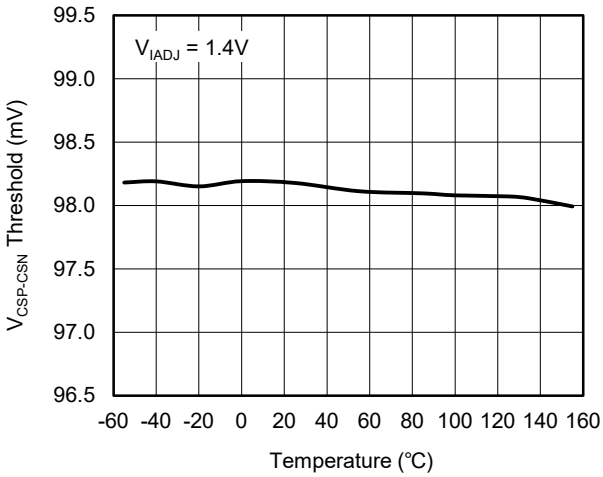
Current Limit Threshold vs. Temperature



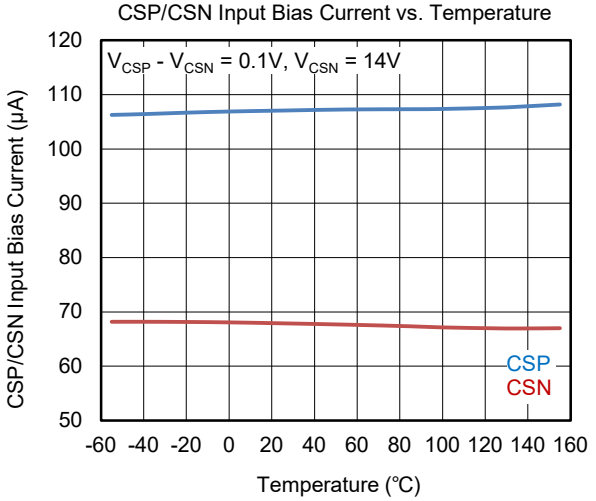
$V_{CSP-CSN}$ Threshold vs. Temperature



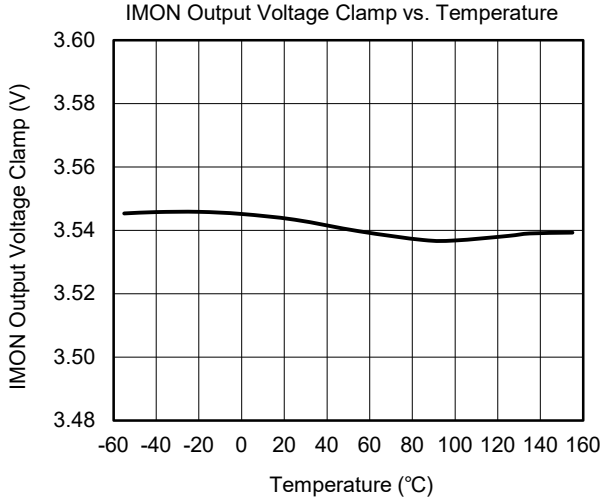
$V_{CSP-CSN}$ Threshold vs. Temperature



CSP/CSN Input Bias Current vs. Temperature



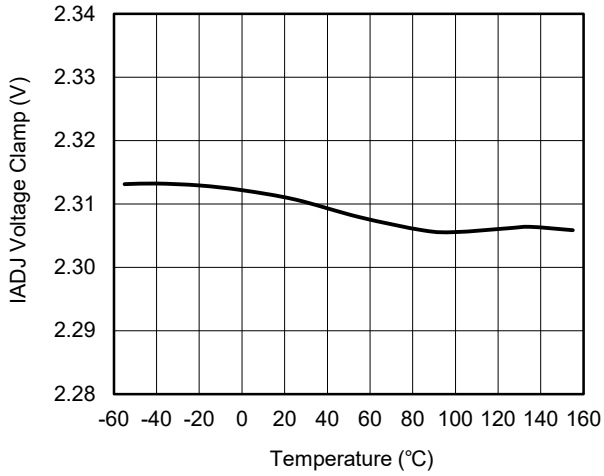
IMON Output Voltage Clamp vs. Temperature



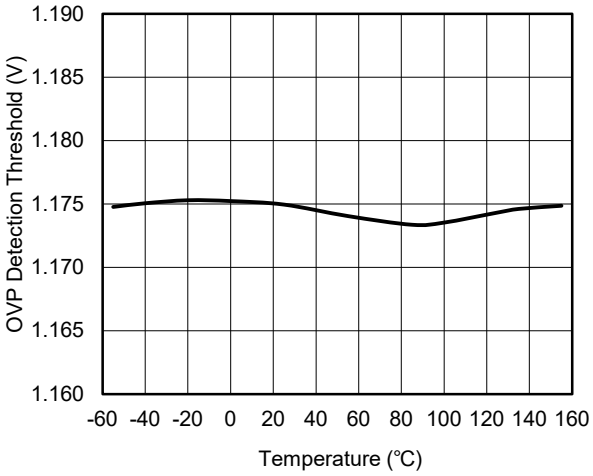
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 14V, V_{IADJ} = 2.2V, C_{VCC} = 1μF, C_{COMP} = 2.2nF, R_{CS} = 100mΩ, R_T = 20kΩ, V_{PWM} = 5V, no load on GATE and PDRV, unless otherwise noted.

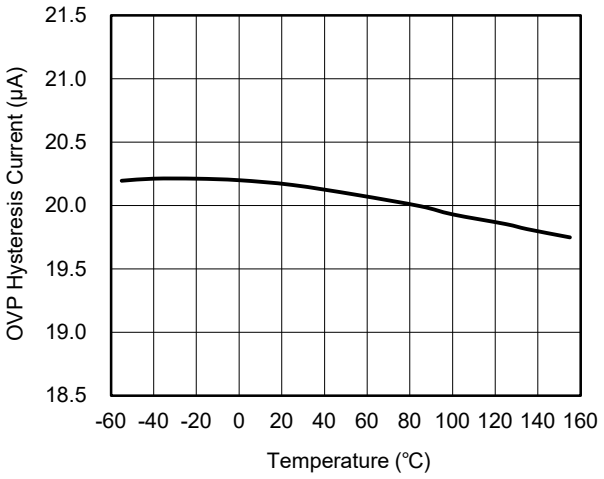
VIADJ Voltage Clamp vs. Temperature



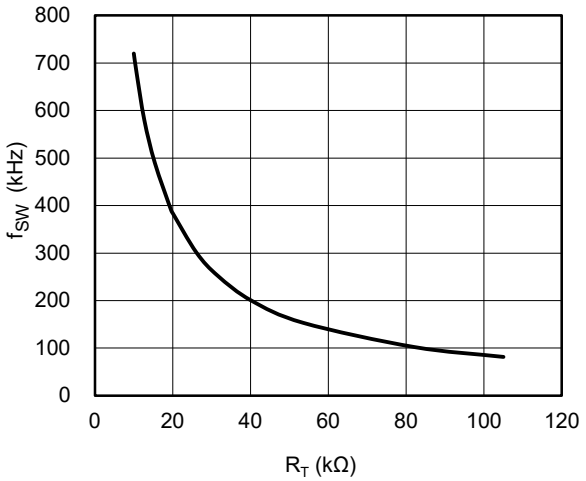
OVP Detection Threshold vs. Temperature



OVP Hysteresis Current vs. Temperature

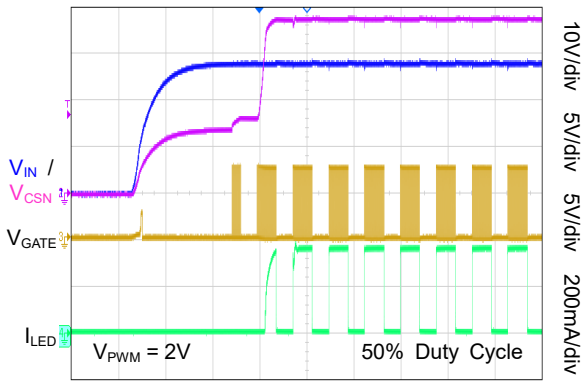


Switching Frequency vs. Timing Resistance (R_T)



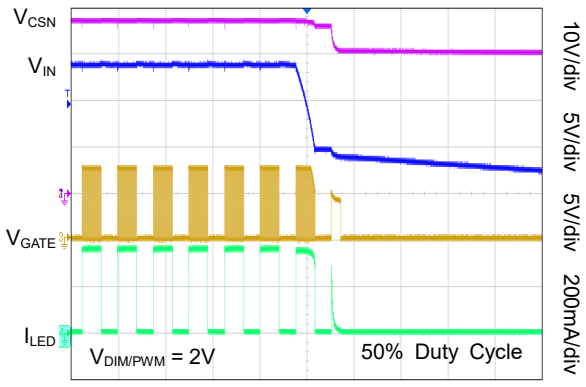
V_{IN} = 14V, V_{OUT} = 38V (12 LED), f_{SW} = 390kHz (R_T = 20kΩ), L = 22μH, V_{IADJ} = 1.51V, R_{CS} = 300mΩ, unless otherwise noted.

V_{IN} Power-on



Time (5ms/div)

V_{IN} Power-off

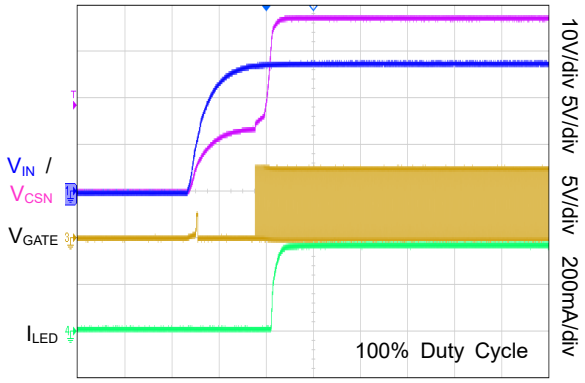


Time (5ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

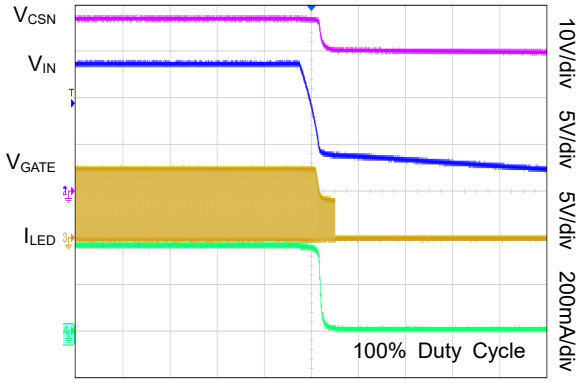
V_{IN} = 14V, V_{OUT} = 38V (12 LED), f_{SW} = 390kHz (R_T = 20kΩ), L = 22μH, V_{IADJ} = 1.51V, R_{CS} = 300mΩ, unless otherwise noted.

V_{IN} Power-on



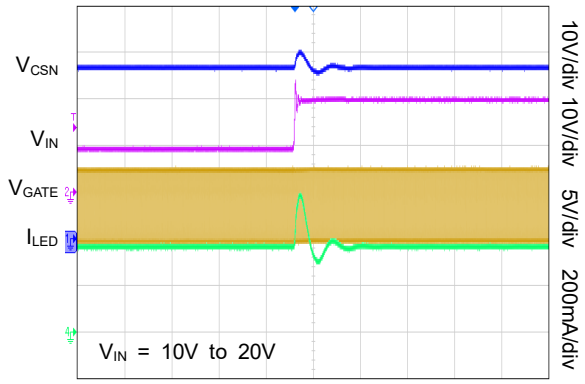
Time (5ms/div)

V_{IN} Power-off



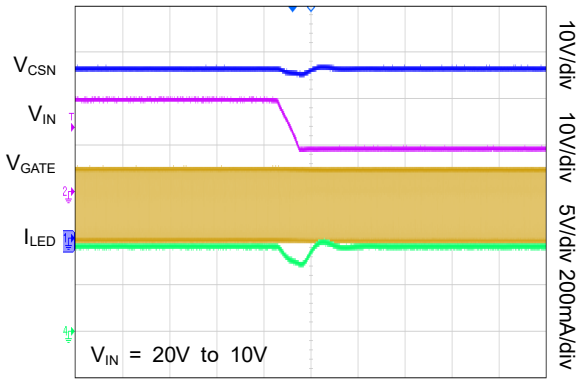
Time (5ms/div)

Line Transient



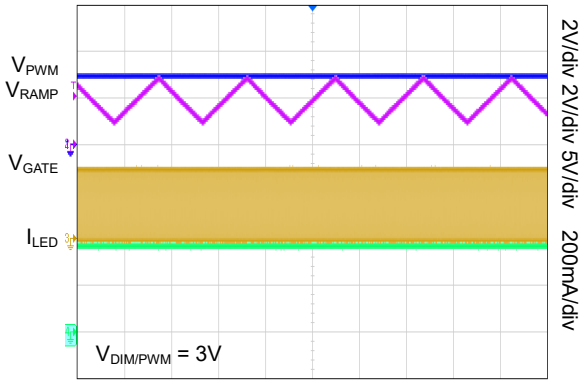
Time (500μs/div)

Line Transient



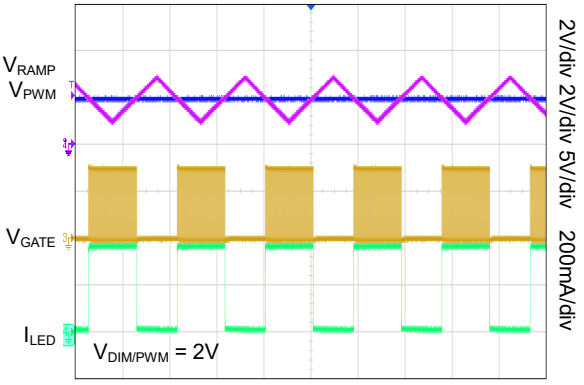
Time (500μs/div)

Steady State



Time (2ms/div)

Steady State

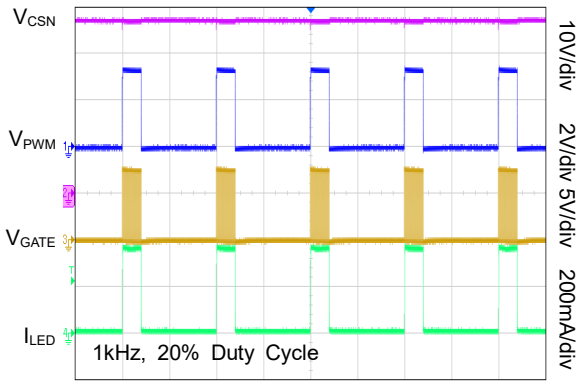


Time (2ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

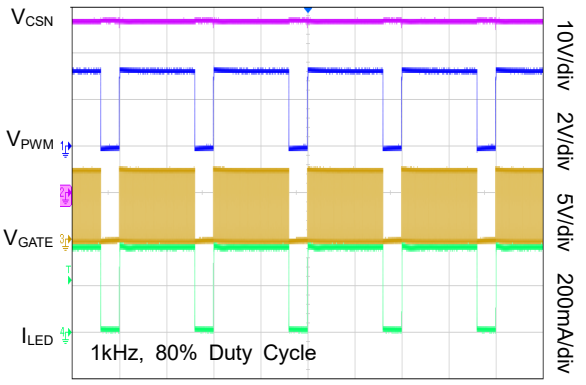
V_{IN} = 14V, V_{OUT} = 38V (12 LED), f_{SW} = 390kHz (R_T = 20kΩ), L = 22μH, V_{IADJ} = 1.51V, R_{CS} = 300mΩ, unless otherwise noted.

Steady State Direct PWM Dimming



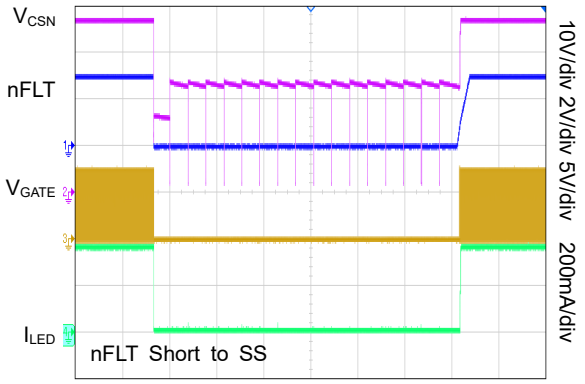
Time (500μs/div)

Steady State Direct PWM Dimming



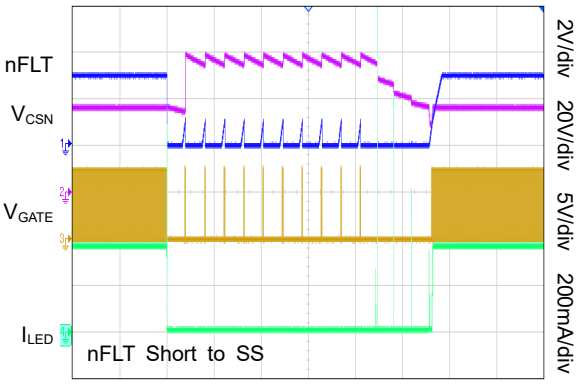
Time (500μs/div)

LED Short



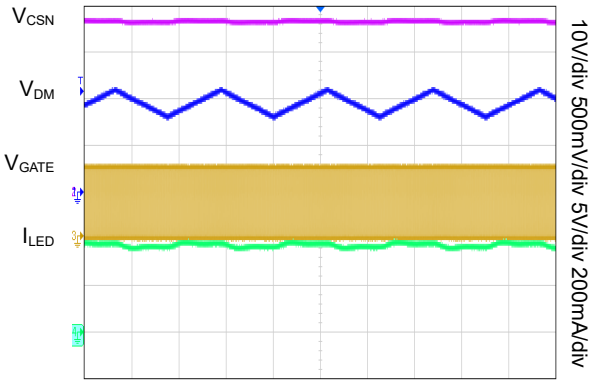
Time (100ms/div)

LED Open



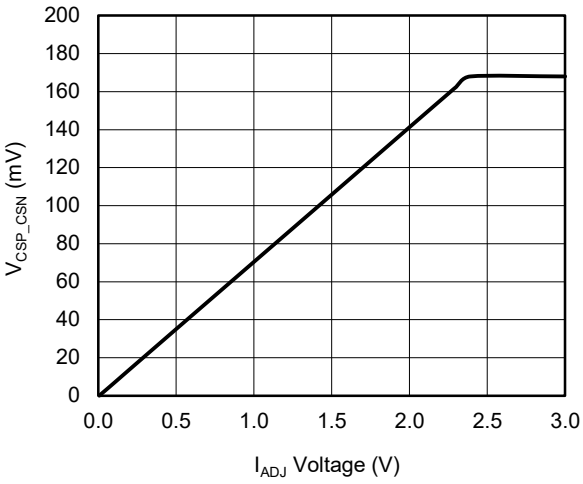
Time (100ms/div)

Frequency Spread Spectrum Mode



Time (500μs/div)

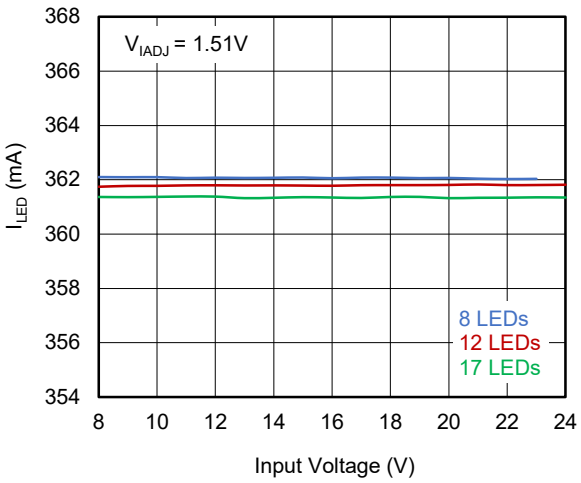
$V_{CSP-CSN}$ vs. I_{ADJ} Voltage



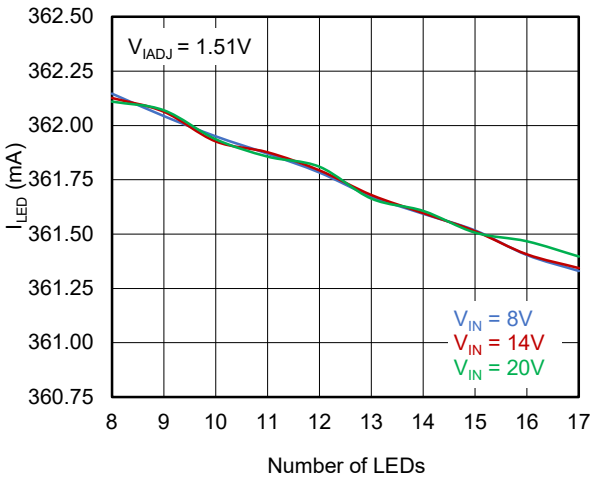
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 14V, V_{OUT} = 38V (12 LED), f_{SW} = 390kHz (R_T = 20kΩ), L = 22μH, V_{IADJ} = 1.51V, R_{CS} = 300mΩ, unless otherwise noted.

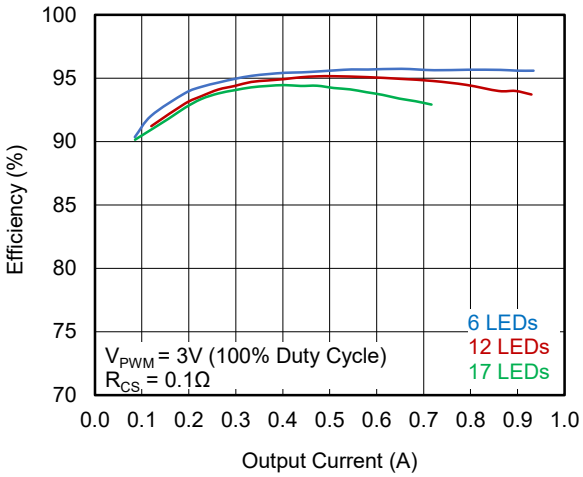
Line Regulation



Load Regulation



Efficiency vs. Output Current



FUNCTIONAL BLOCK DIAGRAM

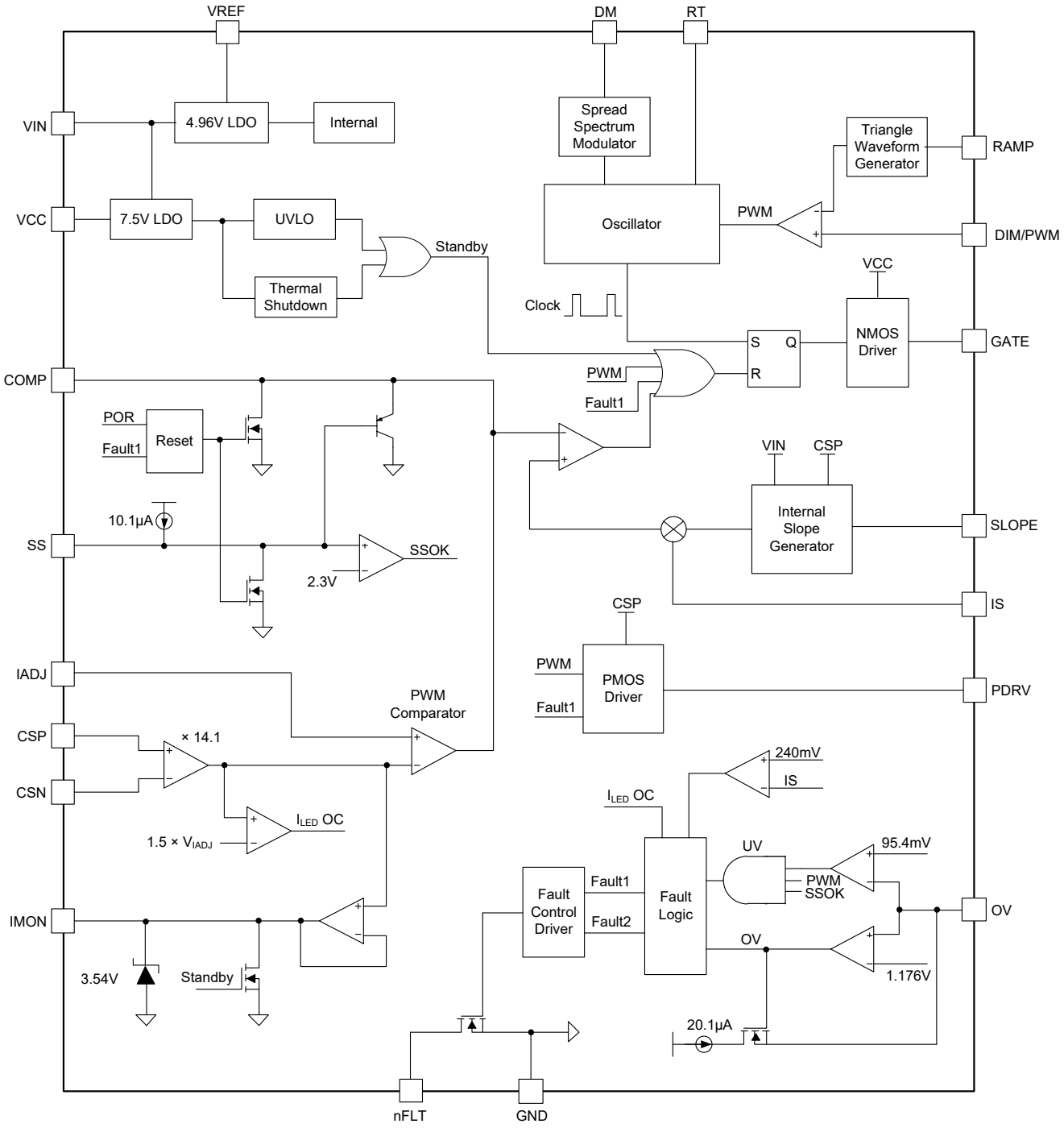


Figure 4. Block Diagram

DETAILED DESCRIPTION

SGM3775Q utilizes peak current mode control and it can achieve constant output current to drive LED lights when combined with external Boost, Buck-Boost power converter topologies. The operating frequency can be set through an external resistor (R_T) on the RT pin or by an external synchronization signal. It equips an optional spread spectrum frequency modulation circuit externally configured by DM pin in order to reduce peak and average conducted and radiated EMI. The integrated current-sense amplifier allows flexible application of a single string of 1 to 20 LEDs, maintaining an accuracy of over ±10% for the current. The LED current regulation threshold can be flexibly set using the analog adjusted input IADJ pin.

While IADJ provides analog adjustment for LED current, the SGM3775Q also integrates an internal PWM generator for PWM dimming of the current. By applying different DC voltages or PWM signals with varying frequencies to the external DIM/PWM pin, various PWM dimming effects can be achieved. When a DC voltage is directly applied to the DIM/PWM pin, the PWM dimming frequency is determined by the capacitor connected to the RAMP pin, C_{RAMP}.

The SGM3775Q also provides voltage on the IMON pin to indicate the instantaneous LED current. Additionally, the nFLT pin is available to report various fault conditions in the system, such as LED over-current, cycle-by-cycle current limit, VOUT over-voltage, and VOUT under-voltage conditions. By connecting the SS pin and nFLT pin together, the SGM3775Q can enter hiccup mode after a fault occurs. Pulling down the SS pin can also shut down the device. Furthermore, the SGM3775Q offers VCC under-voltage protection and thermal shutdown features.

Internal Regulator and Under-Voltage Lockout (UVLO)

SGM3775Q generates a 7.5V (TYP) VCC power supply and a 4.96V (TYP) VREF power supply from the input voltage VIN to provide power for the internal circuitry. The device is enabled when V_{CC} is higher than 4.5V with 400mV hysteresis. The VCC regulator features a 39mA (TYP) current limit to prevent short-circuits on the VCC rail. The VCC is used to power GATE (the N-channel gate driver output). When V_{IN} is lower than 7.5V (TYP), the V_{CC} is V_{IN} - 320mV, choose an N-channel MOSFET with a lower V_{GS_TH} for low V_{IN} application. A 2.2μF to 4.7μF decouple capacitor (C_{VCC}) is recommended to place near the VCC pin and GND. It is not recommended to power the VCC by an external supply or short VCC pin to GND during operation.

VREF is used to power the internal circuit. It also can be used to provide the pull-up supply to resistor divider (e.g. IADJ, DIM/PWM or other external circuit) or the pull-up supply for open-drain circuit (e.g. nFLT). And a 2.2μF to 4.7μF decouple capacitor (C_{VREF}) is recommended to place near the VREF pin and GND. It is not recommended to short VREF pin to GND during operation.

Soft-Start

Once V_{CC} exceeds its V_{CC_UVLO}, the internal soft-start circuit works, and a 10.1μA current source starts charging the external soft-start capacitor (C_{SS}) connected to the SS pin. The voltage on the COMP pin gradually increases with the voltage on the SS pin through an internal diode. When V_{COMP} exceeds 1.4V, the converter starts switching. Note that the 10.1μA (TYP) SS current is enabled only during internal PWM signal on period. The soft-start of COMP voltage helps implement the LED current soft-start. At the beginning of the soft-start sequence, the SS discharge circuit is not released until the V_{SS} is above 47mV (TYP).

The SGM3775Q also can be enabled or disabled by controlling the SS pin. When the SS pin is pulled low, the switching is disabled. And when the external SS signal turn-on slew rate is fast, the COMP voltage cannot follow the SS voltage with the diode, the LED start-up time and inrush current is controlled by the compensation network.

Power Converter

Typically, the SGM3775Q works in a fixed-frequency, peak current control mode. At the beginning of each switching cycle, the N-channel MOSFET turns on at the rising edge of the clock. A resistor (R_{IS}) connected from the IS pin to GND senses the current information of the N-channel MOSFET.

To prevent sub-harmonic oscillations when the duty cycle is larger than 50%, an internal artificial ramp is added to the N-channel MOSFET current-sense signal to generate the inductor peak current information. When the inductor peak current reaches the COMP voltage level, the N-channel MOSFET turns off until the next switching clock comes.

When the V_{IS} reaches 240mV (TYP) threshold, the GATE and PDRV are disabled, the SS and COMP capacitors are discharged. A new soft-start sequence is initiated after the expiration of the 35μs timer period.

DETAILED DESCRIPTION (continued)

Current-Sense

The LED current is sensed by the high-side sensing resistor (R_{CS}) connected between CSP and CSN pins, the CSP pin is connected to the output of the converter, and the CSN pin is connected to the source of the P-channel MOSFET. The SGM3775Q regulates the sensed differential voltage ($V_{CSP-CSN}$) to the analog adjust input voltage (V_{IADJ}) scaled by the current-sense amplifier voltage gain of 14.1.

The SGM3775Q features a configurable LED current reference by varying the V_{IADJ} from 140mV to 2.31V. It proves flexible methods to set the V_{IADJ}. Connect IADJ pin to VREF or external power supply through the resistor divider. Use NTC resistor as a down-divider to implement thermal foldback protection, or a PWM signal will be processed by low-pass filter.

An optional common mode or differential mode low-pass filter implementation can be used to mitigate the impact of large output current ripple and switching current noise. It recommends a filter resistance within the range of 10Ω to 100Ω.

Error Amplifier

The internal amplifier outputs an amplified signal (V_{COMP}) to the external compensation network to achieve closed-loop LED current regulation. The V_{COMP} is proportional to the difference between the LED current-sense feedback voltage ($V_{CSP-CSN}$) and the external IADJ pin voltage (V_{IADJ}). The COMP is connected to the PWM comparator to control the N-channel MOSFET peak current, which is sensed by a sensing resistor (R_{IS}) connected between the source of N-channel MOSFET and GND.

Oscillator

The SGM3775Q frequency can be programmed from 80kHz to 700kHz with a resistor (R_T) from RT pin to GND. The value of R_T for a given operation frequency can be calculated by:

$$R_T(k\Omega) = \frac{11950}{f_{SW}(kHz)^{1.076}} \quad (1)$$

Higher operation frequency takes more switching loss, which is not recommended; otherwise the N-channel MOSFET Q_G is small.

A switching frequency between 80kHz and 700kHz is recommended in order to get an optimal performance over input and output voltage operating range and get the best efficiency. When the device works at higher switching frequencies, it is necessary to select the N-channel MOSFET characteristics carefully and analyze switching losses in detail.

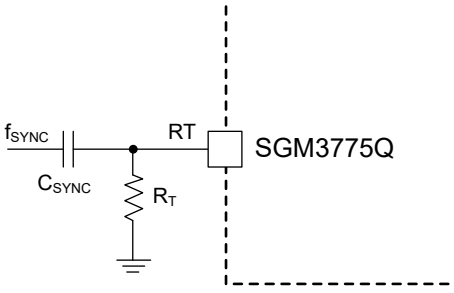


Figure 5. Oscillator Synchronization through AC Coupling

As shown in Figure 5, providing an external clock by a couple capacitors (C_{SYNC} to RT pin) can achieve the synchronization function. To trigger the internal synchronization pulse detector, the external clock at RT pin should meet the rising threshold and falling threshold requirements. A 100nF minimum AC coupled capacitor and a 100ns minimum pulse width clock are recommended during synchronization. Ensure that the external clock signal frequency is within ±20% of the oscillator frequency set by RT resistor. If the external clock signal is lost, the internal oscillator controls the switching clock to keep the LED current in regulation. The RT resistor is required even in synchronization condition.

Frequency Spread Spectrum

To optimize EMI performance, the SGM3775Q provides a frequency spread spectrum option. It can be enabled by connecting a capacitor (C_{DM}) from the DM pin to GND. The internal source and sink currents (both 10μA) charge or discharge the capacitor repeatedly to generate a stable triangular ramp waveform between 0.82V and 1.1V on DM pin. This triangle DM voltage modulates the internal clock frequency within ±15% of the frequency set by RT resistor.

The spread spectrum frequency can be estimated by Equation 2:

$$C_{DM} = \frac{10\mu A}{2 \times f_{MOD}(Hz) \times 0.28V}(\mu F) \quad (2)$$

DETAILED DESCRIPTION (continued)

The modulation frequency should be lower than the oscillator frequency set by RT resistor by a minimum factor of 10.

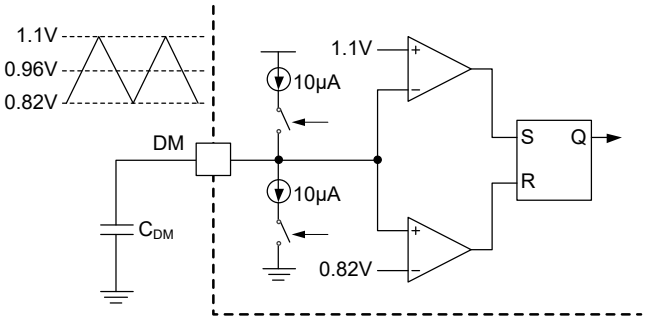


Figure 6. Frequency Spread Spectrum Operation

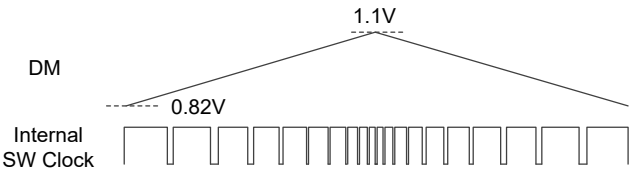


Figure 7. Frequency Spread Spectrum Waveforms

To deactivate the frequency spread spectrum function, connect the DM pin to GND. The internal frequency spread spectrum is not functional when the device operates in synchronization with an external clock signal.

DIM/PWM Input

The SGM3775Q features a PWM generator circuit that simplifies the translation of analog voltage into PWM duty cycle. Adjusting the dimming frequency involves connecting a capacitor (C_{RAMP}) from the RAMP pin to GND. The dimming frequency (f_{DIM}) can be calculated using the following formula:

$$f_{DIM} = \frac{10\mu A}{2 \times 1.92V \times C_{DIM}(\mu F)}(Hz) \quad (3)$$

The internal PWM signal can be adjusted within a range of 0% to 100% by configuring the voltage on the DIM/PWM pin between 0.96V and 2.88V. The relationship between the DIM/PWM pin voltage ($V_{DIM/PWM}$) and the internal PWM duty cycle (D_{PWM_INT}) is described by Equation 4.

$$D_{PWM_INT} = \frac{V_{DIM/PWM} - 0.96V}{1.92V} \quad (4)$$

To enhance dimming precision, it is recommended to utilize the VREF pin along with a resistor divider setup for configuring the $V_{DIM/PWM}$ and its corresponding duty cycle. Additionally, employ a diode to link an external control signal (V_{CTRL}) to the DIM/PWM pin, as depicted in Figure 8, allowing the device to step the duty cycle between 100% and the designated value. This external control signal, typically generated by the command module with amplitude of 2.88V, is determined based on the desired output LED current for the specific application.

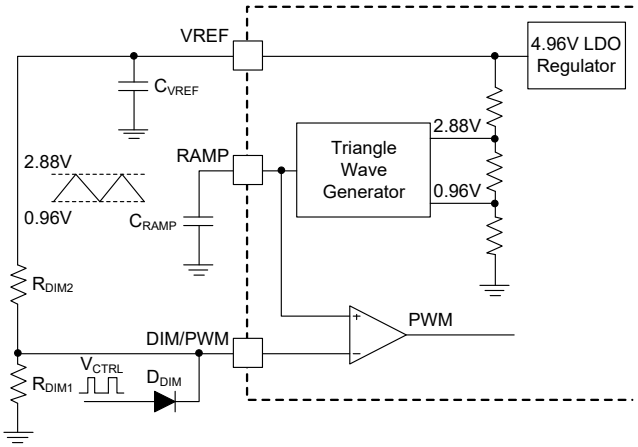


Figure 8. PWM Dimming Using Internal PWM Generator

The device can be set up to work harmoniously with an external PWM signal (V_{PWM_EXT}) which modulates the LED current according to the duty cycle (D_{PWM_EXT}). To enable direct PWM operation, a 249kΩ resistor from the RAMP pin to GND is suggested. In this case, the internal triangle waveform generator is disabled and the internal comparator threshold is adjusted to 2.49V, and the internal PWM duty cycle (D_{PWM_INT}) is managed by the external PWM signal. It's essential to note that the RAMP pin should not be left disconnected.

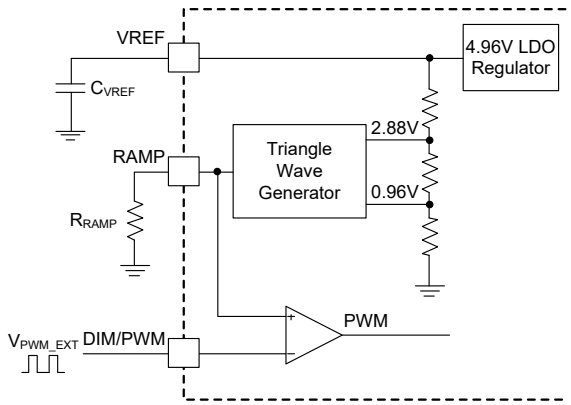


Figure 9. Direct PWM Dimming

DETAILED DESCRIPTION (continued)

The GATE and PDRV outputs are under the control of the internal PWM signal (V_{PWM}). Pushing V_{PWM} into a logic-low state deactivates the switching mechanism, suspends oscillator activity, breaks the COMP pin connection, and directs the PDRV output to VCSP. This configuration is aimed at preserving the charge within the compensation network and output capacitors. Upon the V_{PWM} signal rising edge, the GATE and PDRV outputs are active first, the inductor current is quickly back to its previous steady-state value. When the V_{IS} exceeds the V_{COMP} after the PWM signal changes to high, the internal EA and oscillator are enabled and the COMP recovers the connection.

As a result, the converter rapidly transits into a steady operational mode with minimal LED current over-shoot. If dimming is not necessary, simply connect the DIM/PWM pin to the VCC pin. An internal pull-down resistor configures the input as logic-low, when the DIM/PWM pin is floating, the SGM3775Q is disabled.

Series P-Channel FET Dimming Gate Driver Output

The behavior of the PDRV output hinges on the internal PWM signal and can both sink and source up to 50mA peak current. This capacity serves to regulate a high-side P-channel dimming FET connected in series. The PDRV output is enabled when V_{SS_RST} > 47mV (TYP). Depending on the PWM signal's state, the PDRV toggles between V_{CSP} and (V_{CSP} - 7.43V). This mechanism achieves a full control of the conducting state of the external P-channel dimming FET. To attain a substantial contrast ratio, a series dimming FET is indispensable, enabling swift LED current rise and fall times in response to the PWM input. Do not connect the PDRV pin if the P-channel dimming FET is not required. In this case, the LED current rise and fall times are subject to the inductor slew rate and the system's closed-loop bandwidth.

Current Monitoring Output

The voltage at the IMON pin corresponds to the LED current, which is measured by the current-sense amplifier across the high-side sensing resistor (R_{CS}). This IMON voltage and LED current relationship is linear and accounts for the amplifier's gain factor of 14.1. Connect the IMON output to an external microcontroller or comparator for tasks like detecting and addressing LED open, short, or cable harness faults. To prevent excessive values, the IMON voltage is internally clamped at 3.54V (TYP).

Output Over-Voltage Protection

The SGM3775Q incorporates a dedicated OV pin that can be employed for LED over-voltage protection. When the OV pin voltage is above the threshold (1.176V, TYP), the SGM3775Q immediately pulls the GATE pin low, deactivates the PDRV output, and discharges the SS and COMP capacitors. Configure proper resistor divider between the LED voltage and the OV pin to get the required LED voltage OV threshold. The internal 20.1μA source current is enabled when the OV pin voltage exceeds the 1.176V (TYP), and it can set the over-voltage protection hysteresis voltage combined with the external divider resistor.

Switch Current Limit Protection

The SGM3775Q monitors the IS pin voltage, which senses the N-channel MOSFET current by the IS resistor. When V_{IS_LIMIT} > 240mV (TYP) for 4 cycles or 20μs (the shorter timer works), the nFLT pin is pulled down to GND, the GATE and PDRV output are disabled, the SS and COMP voltage are internally discharged. After SS pin is pulled to low and delays for 35μs, SGM3775Q starts a new soft-start sequence.

LED Over-Current Protection

The SGM3775Q monitors the LED current through the sense voltage on CSP and CSN pins. When the $V_{CSP-CSN}$ exceeds 1.5 times of regulated LED current, the nFLT pin is pulled low for 38ms. Under the LED over-current condition, the power stage keeps normal operation.

DETAILED DESCRIPTION (continued)

Output Under-Voltage Protection

The SGM3775Q also monitors the OV pin voltage to indicate the output UV status. When the OV pin voltage is lower than 95.4mV (TYP), the nFLT pin is pulled low for 38ms. Under the output under-voltage condition, the power stage keeps normal operation. The under-voltage circuit is enabled when internal PWM signal is high and $V_{SS_UVP_EN}$ > 2.3V.

Output Short-Circuit Protection

In the case of SS pin unconnected to nFLT pin (nFLT is pulled up to VREF or other power rail), when the LED over-current or output under-voltage is triggered, the SGM3775Q doesn't discharge the SS and COMP voltages and disable the GATE and PDRV, the device keeps normal operation and just pulls down the nFLT pin for 38ms.

The SGM3775Q provides a flexible application when the LED over-current or output under-voltage is triggered, connecting the SS pin to nFLT together to enable the hiccup mode in this condition. When the nFLT is pulled low for 38ms due to the fault, the SS pin is forced to low, and then the GATE and PDRV output is disabled. After the 38ms timer expired, the nFLT pin changes to high-impedance and a new soft-start sequence is started. If the fault persists after the SS voltage rises to its detection circuit active threshold, the nFLT and SS are pulled down again. This action provides the hiccup mode during LED over-current or output under-voltage and automatically recovers from the fault condition.

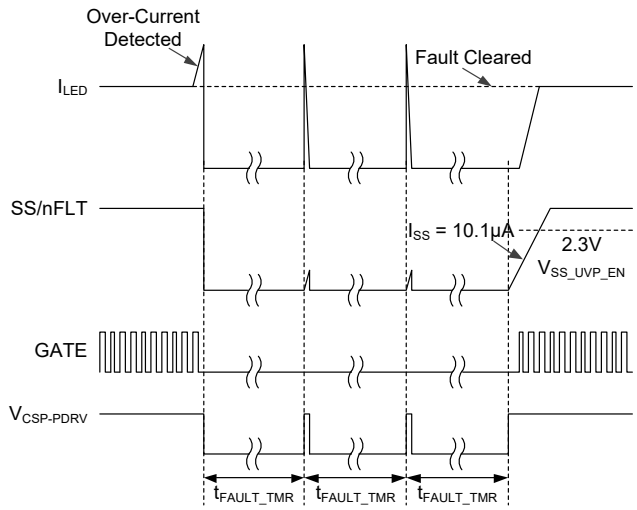


Figure 10. Output Over-Current Fault Protection

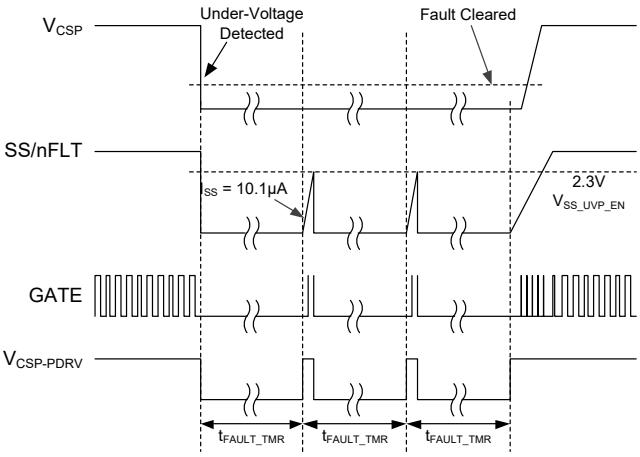


Figure 11. Output Under-Voltage Fault Protection

Over-Temperature Protection

The over-temperature protection (OTP) is implemented to prevent the SGM3775Q from operating at exceedingly high temperatures and possibly being damaged. If the junction temperature exceeds +160℃, the OTP shuts down the device and the nFLT pin keeps the high-impedance state. When the temperature recovers to +145℃, the device resumes the normal operation.

Fault Indicator (nFLT)

The nFLT is an active-low, open-drain output that should be connected to a voltage source via an external pull-up resistor for fault indication.

The nFLT pin is pulled low under the following conditions:

- LED over-voltage (V_{OVP_THR} > 1.176V)
- LED under-voltage (V_{UVP_THR} < 95.4mV)
- LED over-current ($V_{CSP-CSN}$ > 1.5 × V_{IADJ} /(14.1 × R_{CS}))
- Switch current limit condition (V_{IS_LIMIT} > 240mV)

The nFLT pin goes high when the fault conditions remove or when the internal 38ms timer expires. If nFLT is pulled up to VREF, the nFLT is low when the device enters standby state, which happens at UVLO, VREF short or thermal shutdown case.

DETAILED DESCRIPTION (continued)

Device Functional Modes

The following table summarizes the behavior of SGM3775Q in the fault states.

Table 1. Fault Descriptions

Fault	Detection	nFLT Indication	Operation
Input Under-Voltage (UVLO)	V_{CC_FALL} < 4.1V with 400mV hysteresis	High-impedance	The GATE and PDRV output are disabled, the SS and COMP are pulled to GND.
Output Over-Voltage Protection	V_{OVP_THR} > 1.176V	Pulled low, change to high-impedance when V_{OV} < V_{OV_F}	When the OV pin voltage exceeds 1.176V (TYP), the GATE and PDRV output are disabled, the SS and COMP voltage are internally discharged. The internal 20.1μA source current is enabled to set the over-voltage protection hysteresis voltage combined with the external divider resistor. After the output voltage drops below the hysteresis threshold, a new soft-start sequence is initiated.
Switch Current Limit	V_{IS_LIMIT} > 240mV	Pulled low for 38ms	When the IS pin voltage exceeds 240mV (TYP), the GATE and PDRV output are disabled, the SS and COMP voltage are internally discharged. After SS pin is pulled to low and delays for 35μs, SGM3775Q starts a new soft-start sequence.
Output Under-Voltage Protection	V_{UVP_THR} < 95.4mV	Pulled low for 38ms	Under the output under-voltage condition, the power stage keeps normal operation.
Fixed LED Over-Current Protection	$V_{CSP-CSN}$ > 1.5 × V_{IADJ} /(14.1 × R_{CS})	Pulled low for 38ms	Under the LED over-current condition, the power stage keeps normal operation.
Programmable LED Over-Current Protection	V_{IMON} > V_{IADJ}	High-impedance	The current monitor output (I_{MON}) can be utilized to set an external current limit. This output can be linked to an external microcontroller or comparator to offer help in the detection of LED open, short, or cable harness faults.
COMP Pin Short-to-Ground	V_{COMP} < 1.4V	High-impedance	When V_{COMP} < 1.4V, the GATE output is disabled.
VREF Pin Short-to-Ground	V_{REF} < 2.0V	High-impedance	The GATE and PDRV output are disabled, the SS and COMP are pulled to GND.
Thermal Protection	T_{SD} > +160℃	High-impedance	When the junction temperature exceeds +160℃, the OTP shuts down the device. The device resumes normal operation when the temperature falls below +145℃.

APPLICATION INFORMATION

The SGM3775Q is a peak current mode, asynchronous controller for LED lights. The device supports Boost, Buck-Boost, SEPIC and Flyback configurations to meet multi-purpose applications.

The following sections can be used to select component values for the SGM3775Q. The expressions derived for the Buck-Boost topology can be altered to select components for a 1:1 coupled-inductor SEPIC converter. The design process is suited for Flyback and similar converter topologies.

Setting the LED Current

The LED current is sensed by the high-side sensing resistor (R_{CS}) connected between CSP and CSN pins. The SGM3775Q regulates the sensed differential voltage, $V_{CSP-CSN}$, to the analog adjust input voltage, V_{IADJ}, scaled by the current-sense amplifier voltage gain of 14.1. When V_{IADJ} < 2.31V, the LED current is programmed by:

$$I_{LED} = \frac{V_{IADJ}}{14.1 \times R_{CS}} \quad (5)$$

When V_{IADJ} > 2.31V, the internal 2.31V reference sets the $V_{CSP-CSN}$ threshold to 163.2mV and the LED current is programmed by:

$$I_{LED} = \frac{163.2mV}{R_{CS}} \quad (6)$$

An optional common-mode or differential mode low-pass filter implementation can be used to mitigate the impact of large output current ripple and switching current noise. It recommends a filter resistance within the range of 10Ω to 100Ω.

Duty Cycle Limitation and Inductor Average Current

The switch duty cycle (D), as a function of the input and output voltages, defines the device operation. In a steady state, D is calculated by the following equations:

Boost:

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (7)$$

Buck-Boost:

$$D = \frac{V_{OUT}}{V_{IN} + V_{OUT}} \quad (8)$$

The D_{MIN} is determined by the minimum on-time and switching frequency. The D_{MAX} is designed to the fixed 90.6% (TYP) for all applications. If the duty cycle goes beyond the D_{MIN} and D_{MAX} limitation, the LED current cannot keep the regulation.

The Inductor average current can be calculated by the following formula:

Boost:

$$I_{L_AVG} = I_{LED} \times \frac{V_{OUT}}{V_{IN}} \quad (9)$$

Buck-Boost:

$$I_{L_AVG} = I_{LED} \times (1 + \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

Soft-Start

The soft-start time (t_{SS}) is defined as the rise time of LED current from 0 to target current. It is related to the SS capacitor (C_{SS}), output voltage (V_{OUT}), output capacitor (C_{OUT}), and the LED voltage (V_{LED}) as shown in the Figure 12.

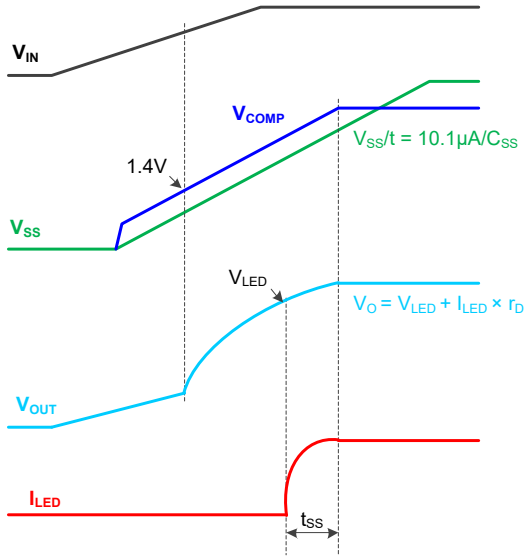


Figure 12. T_{SS} and the Factors

Slope Compensation

To provide the flexible artificial ramp over the wide input and output voltage range, the SGM3775Q senses the input and output voltage information to regulate the SLOPE pin voltage. The internal slope compensation voltage is determined by the regulated V_{SLOPE} and the external R_{SLOPE} setting. Setting the R_{SLOPE} according to inductor and R_{IS} value as the following equation can get the proper compensation and provide a stable operation for Boost and Buck-Boost topologies.

$$R_{SLOPE} = 275 \times 10^6 \times \frac{L}{R_{IS}} (\Omega) \quad (11)$$

APPLICATION INFORMATION (continued)

Inductor Selection

The selection of inductor affects the inductor current ripple and the boundary of DCM and CCM operation. In battery-powered LED driver applications, SGMICRO recommends that all LED current applications are in CCM. It means that setting the CCM boundary P_{O_BDRY} to the actual minimum output power P_{O_MIN}. If the P_{O_MIN} is too small, it is recommended to choose the P_{O_BDRY} between the 25% and 50% of P_{O_MAX}.

$$P_{O_BDRY} \le I_{LED_MIN} \times V_{OUT_MIN} \quad (12)$$

$$\frac{P_{O_MAX}}{4} \le P_{O_BDRY} \le \frac{P_{O_MAX}}{2} \quad (13)$$

Boost:

$$L \ge \frac{V_{IN}^2}{2 \times P_{O_BDRY} \times f_{SW}} \times (1 - \frac{V_{IN}}{V_{OUT}}) \quad (14)$$

The worst case occurs at V_{OUT_MAX} and $3V_{IN} = 2V_{OUT}$ condition.

Buck-Boost:

$$L \ge \frac{(V_{IN} \times V_{OUT})^2}{2 \times P_{O_BDRY} \times f_{SW} \times (V_{IN} + V_{OUT})^2} \quad (15)$$

The worst case occurs at V_{IN_MAX} and V_{OUT_MAX} condition.

Besides the inductance, the inductor saturation current rating also should be considered in the converter. The saturation current rating should be higher than the maximum peak inductor current during operation. Following gives the inductor peak current calculation formula and it is easy to analyze the maximum inductor peak current condition.

Boost:

$$I_{L_PK} = \frac{V_{OUT} \times I_{LED}}{V_{IN}} + \frac{V_{IN}}{2 \times L \times f_{SW}} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \quad (16)$$

In Equation 16, the first portion is the inductor average current, which plays a dominant role in whole peak current. So the worst case occurs at P_{O_MAX} and V_{IN_MIN} condition.

Buck-Boost:

$$I_{L_PK} = I_{LED} \times \left(1 + \frac{V_{OUT}}{V_{IN}}\right) + \frac{V_{IN} \times V_{OUT}}{2 \times L \times f_{SW} \times (V_{IN} + V_{OUT})} \quad (17)$$

Similar as the Boost converter, the inductor average current gives a larger portion in peak current, the worst case also occurs at P_{O_MAX} and V_{IN_MIN} condition.

Input Capacitor Selection

The input capacitors provide the energy story during the switching on/off and control the input voltage ripple within target design range. In Boost and SEPIC topologies, the input capacitor current is continuous, while in Buck-Boost and Flyback topologies, the input capacitor current is discontinuous. The input voltage ripple ΔV_{IN} is calculated by following formulas:

Boost:

$$\Delta V_{IN} = \frac{V_{IN}}{8 \times f_{SW}^2 \times L \times C_{IN}} \times (1 - \frac{V_{IN}}{V_{OUT}}) \quad (18)$$

The worst case occurs at V_{OUT_MAX} and $V_{IN} = 0.5 \times V_{OUT}$ condition.

Buck-Boost:

$$\Delta V_{IN} = \frac{I_{LED}}{f_{SW} \times C_{IN} \times (1 + \frac{V_{IN}}{V_{OUT}})} \quad (19)$$

The worst case occurs at V_{IN_MAX} and V_{OUT_MAX} condition.

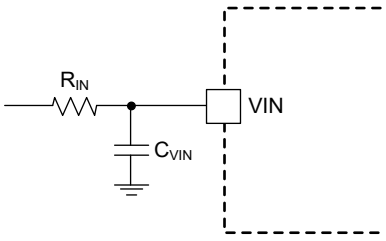


Figure 13. VIN Filter

The VIN pin is decoupled with a 0.1μF ceramic capacitor which is placed as close as possible to the device. A series 10Ω resistor is also put to create a 150kHz low-pass filter.

Output Capacitor Selection

The output current is discontinuous for both Boost and Buck-Boost topologies. The output capacitors provide the energy story during switching and control the LED current ripple within target design range.

Boost:

$$\Delta I_{LED} = \frac{I_{LED}}{f_{SW} \times r_D \times C_{OUT}} \times (1 - \frac{V_{IN}}{V_{OUT}}) \quad (20)$$

where, r_D is the total series resistance of the LED string. The LED current ripple worst case occurs at r_{D_MIN}, P_{O_MAX} and V_{IN_MIN} condition.

Buck-Boost:

$$\Delta I_{LED} = \frac{V_{OUT} \times I_{LED}}{(V_{IN} + V_{OUT}) \times f_{SW} \times C_{OUT} \times r_D} \quad (21)$$

APPLICATION INFORMATION (continued)

The worst case occurs at r_{D_MIN}, P_{O_MAX} and V_{IN_MIN} condition.

SGMICRO recommends ceramic capacitors for the output capacitor due to the low ESR and long lifetime. If aluminum electrolytic capacitor is chosen, the ESR influence should be considered in LED current ripple and the ripple current rating should be higher than the RMS current to avoid the overheating. The formula below gives the RMS output capacitor current calculation.

Boost and Buck-Boost:

$$I_{COUT_RMS} = I_{LED} \times \sqrt{\frac{D}{1-D}} \quad (22)$$

Give the further formula:

Boost:

$$I_{COUT_RMS} = I_{LED} \times \sqrt{\frac{V_{OUT}}{V_{IN}} - 1} \quad (23)$$

Buck-Boost:

$$I_{COUT_RMS} = I_{LED} \times \sqrt{\frac{V_{OUT}}{V_{IN}}} \quad (24)$$

For both Boost and Buck-Boost topologies, the worst case of RMS output capacitor current occurs at P_{O_MAX} and V_{IN_MIN} condition.

Main Power MOSFET Selection

The MOSFET's V_{DS}, I_{DS}, Q_G, R_{DSON} are the critical parameters during choosing the main power MOSFET. The V_{DS} should larger than the maximum SW node voltage, and the I_{DS} should larger than the MOSFET RMS current during switching. The formulas below give the VDS selection and the MOSFET RMS current calculation.

Boost:

$$V_{DS} = 1.1 \times V_{OUT_OV} \quad (25)$$

Buck-Boost:

$$V_{DS} = 1.1 \times \left(V_{OUT_OV} + V_{IN_MAX}\right) \quad (26)$$

where, V_{OUT_OV} is the over-voltage protection threshold and the worst-case output voltage under fault conditions.

Boost and Buck-Boost:

$$I_{Q_RMS} = I_{L_AVG} \times \sqrt{D} \quad (27)$$

Boost:

$$I_{Q_RMS} = \frac{V_{OUT} \times I_{LED}}{V_{IN}} \times \sqrt{1 - \frac{V_{IN}}{V_{OUT}}} \quad (28)$$

Buck-Boost:

$$I_{Q_RMS} = \frac{V_{OUT} \times I_{LED}}{V_{IN}} \times \sqrt{1 + \frac{V_{IN}}{V_{OUT}}} \quad (29)$$

Select a MOSFET with low total gate charge Q_G and low R_{DSON} to minimize switching loss and conduction loss. Generally, when the MOSFET has larger V_{DS}, the Q_G × R_{DSON} is larger. The switching and conduction losses are estimated as follows:

$$P_{COND_LOSS} = R_{DS(ON)} \times I^2_{Q_RMS} \quad (30)$$

$$P_{SW_LOSS} \approx V_{SW} \times I_L \times f_{SW} \times \left(\frac{0.5 \times Q_{GS} \times (R_{DRIVER} + R_G)}{V_{CC} - V_{th} - 0.5 \times I_L / g_{fs}} + \frac{Q_{GD} \times (R_{DRIVER} + R_G)}{V_{CC} - V_{th} - I_L / g_{fs}}\right) \quad (31)$$

Where, R_{DRIVER} is the gate driver resistance, R_G is the MOSFET intrinsic gate resistance. I_L is the average inductor current. g_{fs} is the MOSFET forward transconductance. Choose proper MOSFET and switching frequency to get an optimal efficiency for system.

If the Q_G is too large and the switching speed is too slow, the MOSFET may not turn on successfully finally.

When V_{IN} is lower than 7.5V, the V_{CC} is V_{IN} - 320mV, choose an N-channel MOSFET with a lower V_{GS_TH} for low V_{IN} application.

Rectifier Diode Selection

SGMICRO recommends to use a Schottky diode for D1 due to its low forward voltage drop and small reverse recovery charge. A low reverse leakage current is critical when selecting the Schottky diode, because it impacts the overall converter operation efficiency. The diode must be rated to handle the maximum output voltage and the maximum output current.

Switch Current-Sense Resistor

A resistor connected from the IS pin to GND (R_{IS}) senses the current information of the N-channel MOSFET. When the V_{IS} reaches 240mV (TYP) threshold, SGM3775Q turns off the N-channel MOSFET. The R_{IS} is used to set the switch peak current limit. The R_{IS} is calculated by the formula below:

$$R_{IS} = \frac{V_{IS_LIMIT}}{I_{L_PK}} \quad (32)$$

APPLICATION INFORMATION (continued)

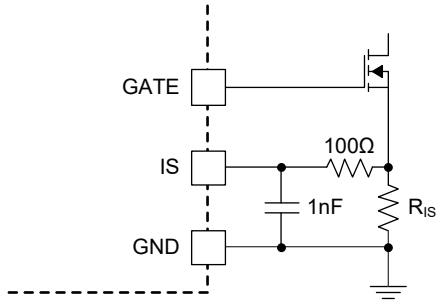


Figure 14. IS Input Filter

The low-pass filter is optional for the switch current sense. A 1nF and less than 100Ω RC network is recommended.

Feedback Compensation

The open-loop transfer function is constituted by power stage, feedback stage and compensation stage. The power stage transfer function (V_{COMP} to I_{LED}) is shown as follows in first-order approximation.

$$\frac{I_{LED}}{V_{COMP}} = G_0 \times \frac{1-\frac{s}{\omega_Z}}{1+\frac{s}{\omega_P}} \quad (33)$$

For both Boost and Buck-Boost topologies, there are a single pole ω_P and a right half-plane zero (R_{HPZ}) ω_Z in the power stage. The ω_P is related to the output voltage, output capacitor, LED current, and LED string dynamic resistance. The ω_Z is related to output voltage, duty cycle, inductance, and the LED current. The DC gain G0 is related to the output voltage, duty cycle, LED current, LED string dynamic resistance, and the switch current-sense resistor. Table 2 shows the G0, ω_P and ω_Z formulas in the power stage transfer function.

The feedback and compensation stages include the current sense and transconductance amplifier with external compensation network. To improve the DC gain and the gain margin of the open-loop transfer function, add a Type 1 compensation circuit as shown in Figure 15. A compensation capacitor, C_{COMP}, takes a pole at the origin, can provide the large DC gain and more gain margin. Large DC gain minimizes the output steady state error. The feedback and compensation stage transfer function with Type 1 compensation is shown as below:

$$-\frac{V_{COMP}}{I_{LED}} = \frac{1}{\frac{s}{\omega_{P0}}} \quad (34)$$

where,

$$\omega_{P0} = \frac{14 \times g_M \times R_{CS}}{C_{COMP}} \quad (35)$$

g_M is the amplifier transconductance (117μA/V, TYP).

To get above 45° phase margin for open-loop transfer function, SGMICRO recommends setting the ω_{P0} to about one fifth of ω_P:

$$C_{COMP} = \frac{70 \times g_M \times R_{CS}}{\omega_P}$$

Type 1 compensation provides high DC gain, efficient phase margin and gain margin, but the crossover frequency is extremely low. To improve the dynamic performance, Type 2 compensation network as shown in Figure 16 is recommended.

Type 2 compensation network provides a pole at the origin ω_{P0}, a zero ω_{Z1} consists of R_{COMP} and C_{COMP}, a high frequency pole ω_{P1} consists of R_{COMP}, C_{COMP}, and C_{HF}. The feedback and compensation stage transfer function with Type 2 compensation is shown as below:

$$-\frac{V_{COMP}}{I_{LED}} = \frac{14.1 \times g_M \times R_{CS}}{s \times (C_{COMP}+C_{HF})} \times \frac{1+s \times R_{COMP} \times C_{COMP}}{1+s \times R_{COMP} \times \frac{C_{COMP} \times C_{HF}}{C_{COMP}+C_{HF}}} \quad (36)$$

Generally, the $C_{HF} << C_{COMP}$, then:

$$-\frac{V_{COMP}}{I_{LED}} = \frac{1}{\frac{s}{\omega_{P0}}} \times \frac{1+\frac{s}{\omega_{Z1}}}{1+\frac{s}{\omega_{P1}}} \quad (37)$$

where,

$$\omega_{P0} = \frac{14.1 \times g_M \times R_{CS}}{C_{COMP}} \quad (38)$$

$$\omega_{Z1} = \frac{1}{R_{COMP} \times C_{COMP}} \quad (39)$$

$$\omega_{P1} = \frac{1}{R_{COMP} \times C_{HF}} \quad (40)$$

APPLICATION INFORMATION (continued)

To get above 45° phase margin for open-loop transfer function, SGMICRO recommends putting the ω_{Z1} at around ω_P and setting the crossover frequency ω_C to about one fifth of ω_Z, and then the C_{COMP} and R_{COMP} can be calculated by:

$$\omega_C = G_0 \times \omega_{P0} \quad (41)$$

$$C_{COMP} = \frac{70 \times g_M \times R_{CS} \times G_0}{\omega_Z} \quad (42)$$

$$R_{COMP} = \frac{1}{\omega_P \times C_{COMP}} \quad (43)$$

Over-Voltage and Under-Voltage Protection

The over-voltage and under-voltage protection are both aimed at LED string voltage (V_{OUT}). For Boost and SEPIC topologies, the LED voltage reference is GND, so the OV or UV threshold is set by resistor divider R_{OV2} and R_{OV1} directly. For Buck-Boost topology, the LED voltage reference is V_{IN}, so the LED voltage is sensed by a PNP transistor and is translated to GND reference. The OV and UV threshold setting can follow the formulas below:

Boost:

$$V_{OUT_OV} = V_{OVP_THR} \times \frac{R_{OV1} + R_{OV2}}{R_{OV1}} \quad (44)$$

Buck and Buck-Boost:

$$V_{OUT_OV} = V_{OVP_THR} \times \frac{R_{OV2}}{R_{OV1}} + 0.7 \quad (45)$$

The over-voltage hysteresis, V_{OV_HYS} is:

$$V_{OV_HYS} = I_{OVP_HYS} \times R_{OV2} \quad (46)$$

The corresponding under-voltage fault threshold, V_{OUT_UV} is:

$$V_{OV_UV} = 0.1 \times \frac{R_{OV1} + R_{OV2}}{R_{OV1}} \quad (47)$$

Series P-Channel MOSFET Selection

The P-channel MOSFET is used for dimming to improve dimming performance. When dimming is off, the voltage on the P-channel is equal to the LED voltage. Select the P-channel MOSFET V_{DS} to exceed the LED voltage, and ensure that the continuous drain current exceeds the 110% of LED current with a lower R_{DSON}. Besides, the C_{SS} and Q_G of the MOSFET impact on the on or off speed. Select MOSFET with lower C_{SS} and Q_G to improve the PWM dimming accuracy at small dimming duty cycle.

Table 2. Small-Signal Model Parameters

	DC Gain (G0)	Pole Frequency (ω_P)	Zero Frequency (ω_Z)
Boost	$\frac{(1-D) \times V_{OUT}}{R_{IS} \times (V_{OUT} + r_D \times I_{LED})}$	$\frac{V_{OUT} + r_D \times I_{LED}}{V_{OUT} \times r_D \times C_{OUT}}$	$\frac{V_{OUT} \times (1-D)^2}{L \times I_{LED}}$
Buck-Boost	$\frac{(1-D) \times V_{OUT}}{R_{IS} \times (V_{OUT} + D \times r_D \times I_{LED})}$	$\frac{V_{OUT} + D \times r_D \times I_{LED}}{V_{OUT} \times r_D \times C_{OUT}}$	$\frac{V_{OUT} \times (1-D)^2}{D \times L \times I_{LED}}$

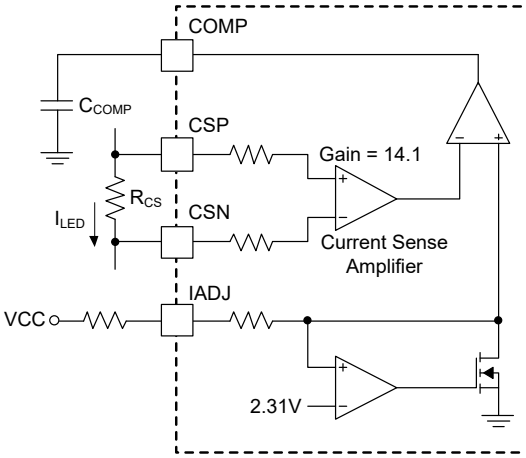


Figure 15. Integral Compensator

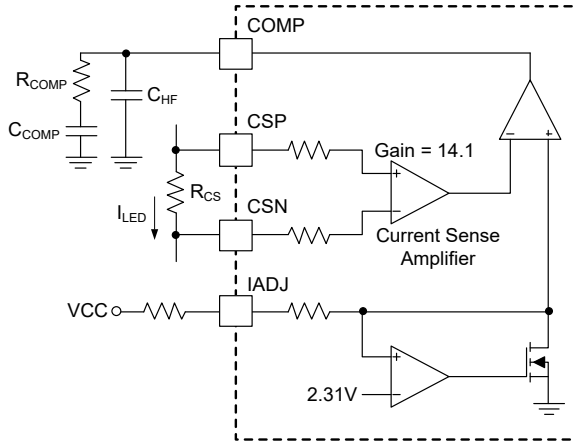


Figure 16. Proportional Integral Compensation

APPLICATION INFORMATION (continued)

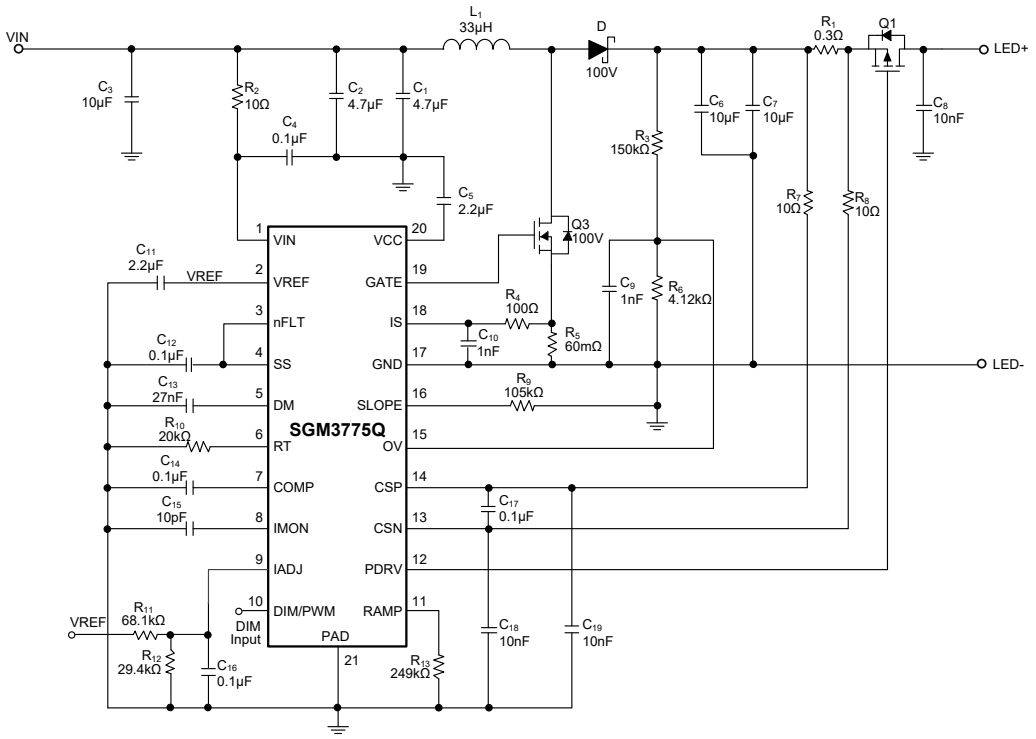


Figure 17. Typical Application Circuit for Boost Topology

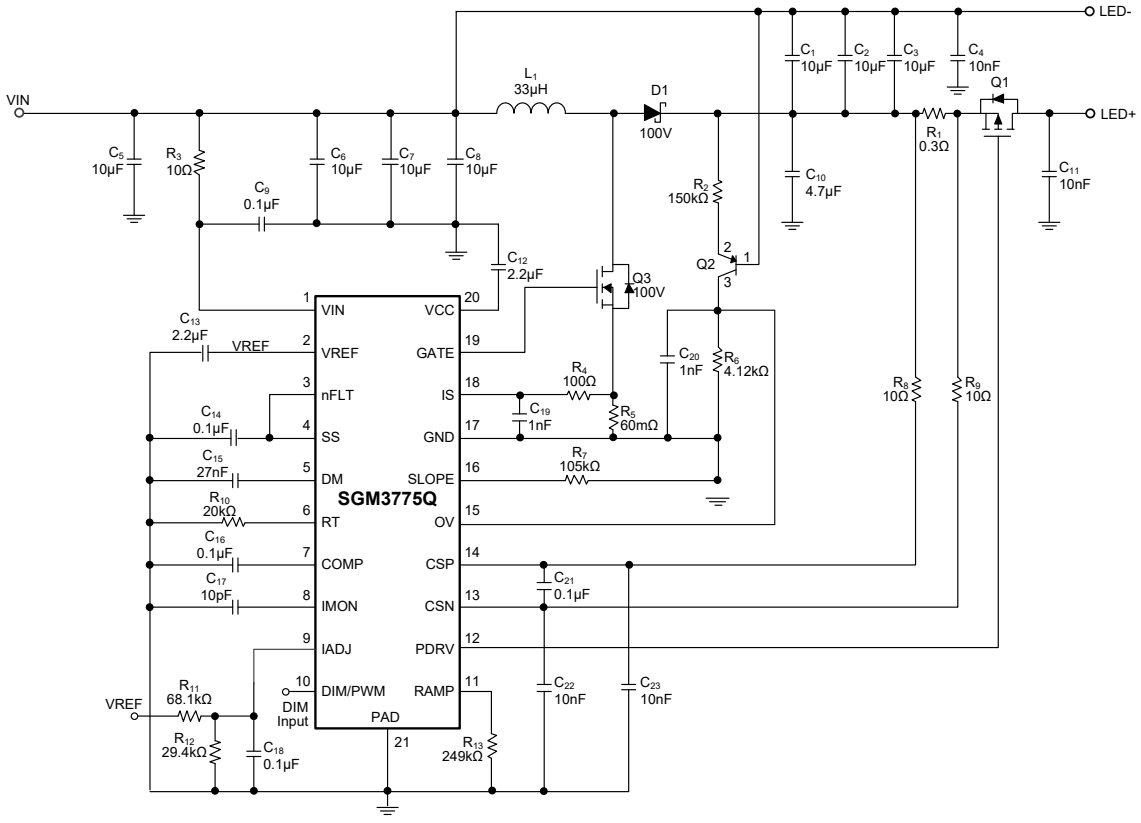


Figure 18. Typical Application Circuit for Buck-Boost Topology

APPLICATION INFORMATION (continued)

Power Supply Recommendations

The SGM3775Q is intended to function within a supply voltage range of 4.5V to 65V. The source could be a car battery or another pre-regulated power supply. If the input supply is situated at a distance from the device, bulk capacitance or an input filter, alongside ceramic bypass capacitors are recommended to mitigate noise and electromagnetic interference (EMI) issues.

Layout Guidelines

Efficient PCB layout is critical for stable operation and device performance. For the best results, please refer to the following guidelines:

1. For all converter topology, please pay attention to the layout of discontinuous current paths. Make sure these paths short and wide enough to get the discontinuous loop as small as possible.

2. There are some sensitive signals, such as IADJ, IS, COMP and DIM/PWM, make sure these signal routes short and far away from the high-speed switching nodes and routes.

3. Kelvin connects the current-sense resistor (R_{CS}) to CSP and CSN pins. Reserve the optional location for the common mode and differential mode noise filter for these two pins.

4. Separate the power loop GND and analog signal GND, and connect them together at IC GND pin.

5. Use at least one internal PCB layer for the GND plane to shield the EMI and keep radiated noise away from the device.

6. Place some vias under the exposed pad to help the thermal dissipation. Use large copper areas to minimize the conduction and thermal stress.

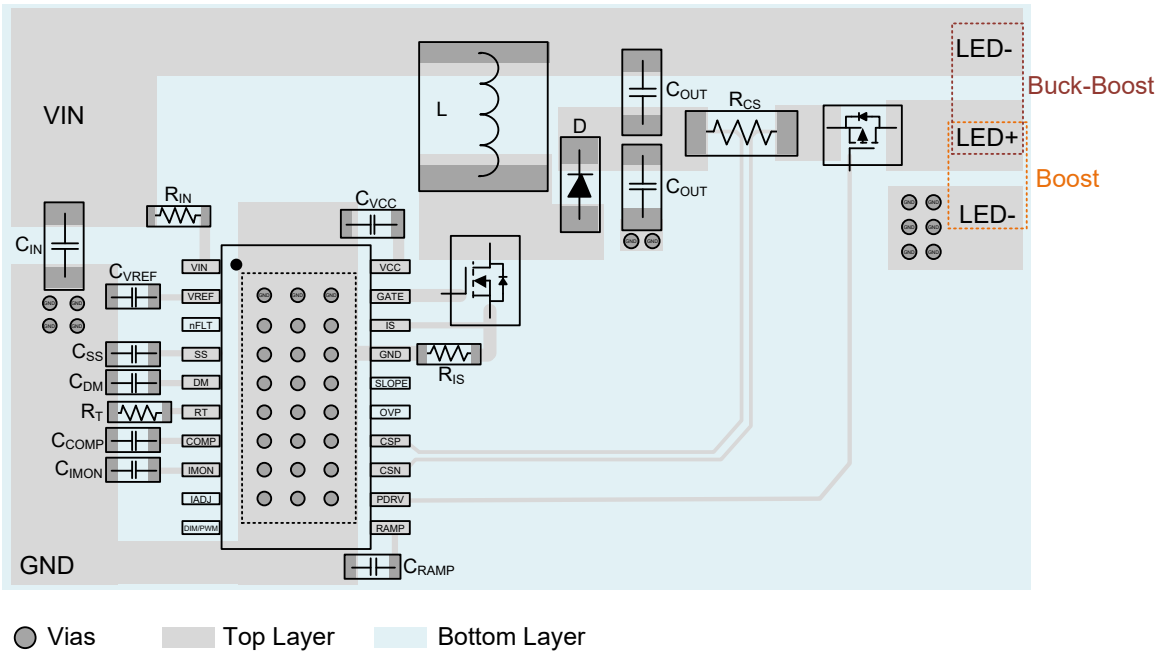


Figure 19. PCB Layout Example

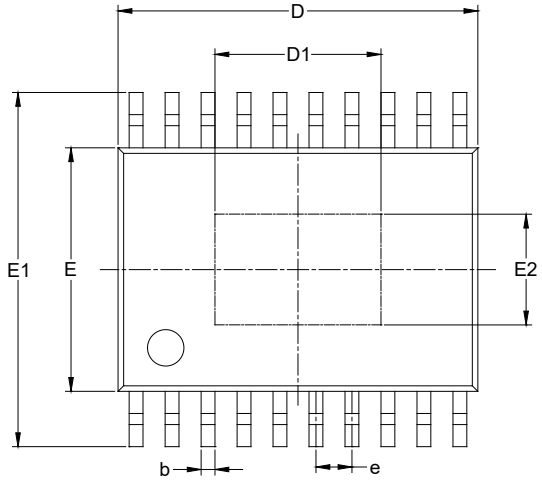
REVISION HISTORY

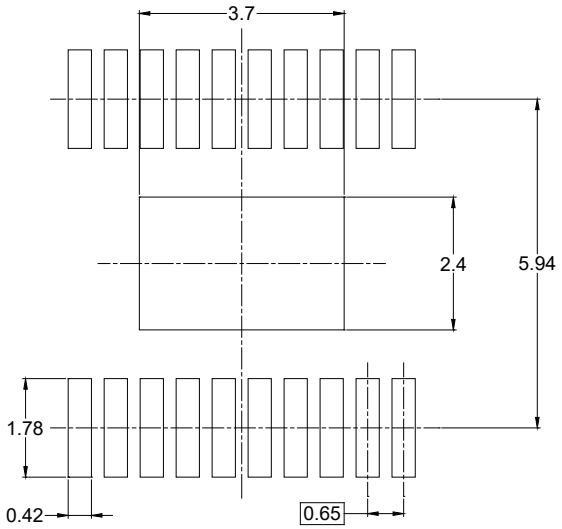
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (SEPTEMBER 2024) to REV.A	Page
Changed from product preview to production data	All

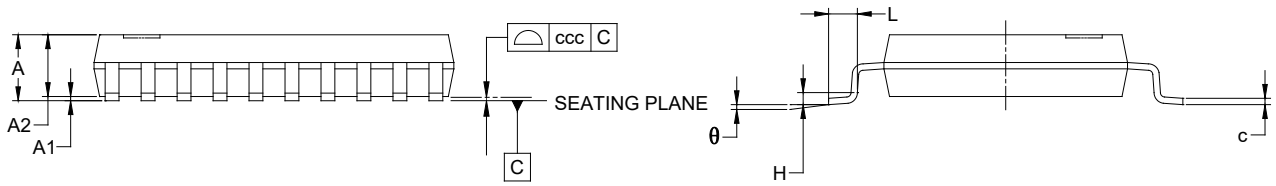
PACKAGE OUTLINE DIMENSIONS

TSSOP-20A (Exposed Pad)





RECOMMENDED LAND PATTERN (Unit: mm)

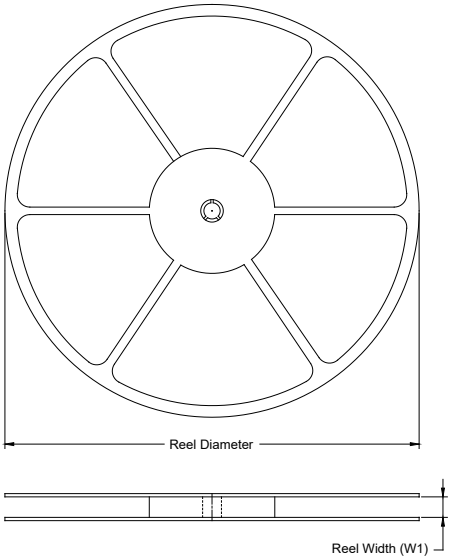


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	6.400	-	6.600
D1	2.610	-	3.400
E	4.300		4.500
E1	6.200	-	6.600
E2	1.610	-	2.400
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

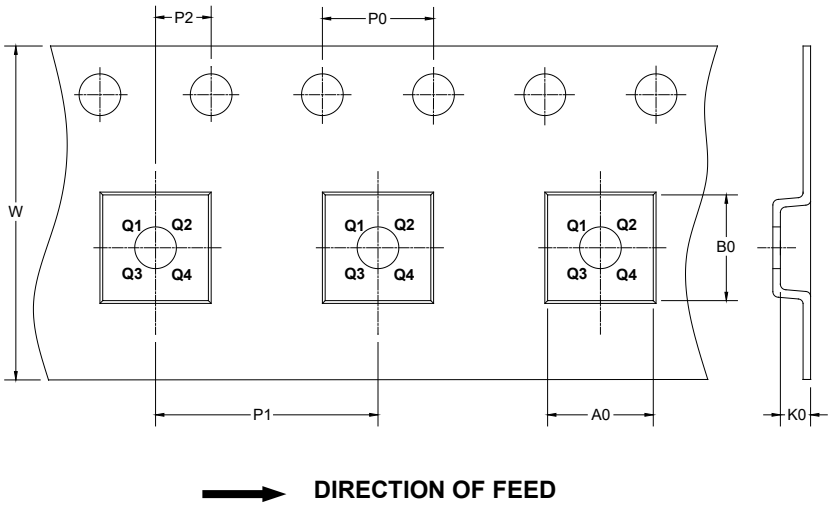
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



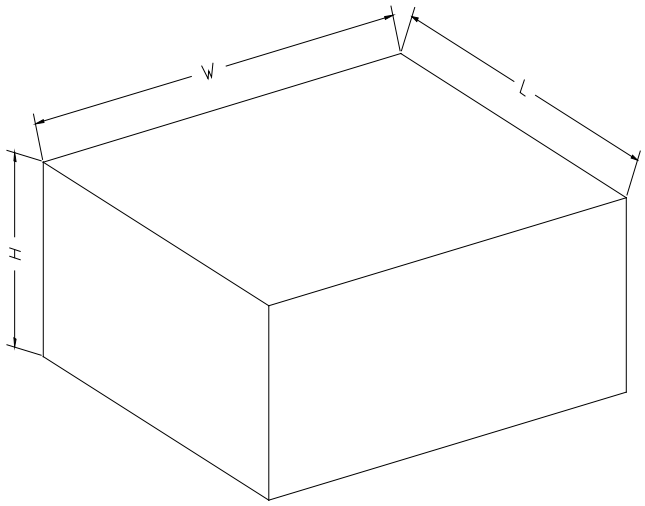
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-20A (Exposed Pad)	13"	16.4	6.95	7.10	1.60	4.0	8.0	2.0	16.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002