SGM42203Q
2-Channel High-side Driver with Analog Current Sense for 24V Automotive Applications

GENERAL DESCRIPTION

The SGM42203Q is a high-side driver intended for a wide range of automotive applications. It is usually used to drive resistive or inductive load with the other terminal connected to GND. If low energy spike occurs on VCC, the internal VCC voltage clamp protects the device.

The device integrates current sense function for sensing load current through the current sense pin current out. If any of following occurs, overload current, over-temperature or short-to-VCC, the current sense pin will function to report these faults.

The current limit protects the device in case of overload conditions. Built-in output current limit mask-time allows the current limit to foldback to a preset (selectable) lower level after a preset (adjustable) time delay to protect the load more robustly per application demands.

The device will be reset by pulling low the fault reset standby pin (nFR_STBY). Pulling all the inputs and nFR_STBY pins low will disable the device and leave it in standby state.

The device is AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and it is suitable for automotive applications.

The SGM42203Q is available in a Green TSSOP-16A (Exposed Pad) package.

APPLICATIONS

Resistive Loads
Inductive Loads
Capacitive Loads

FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
  Device Temperature Grade 1
  T_A = -40℃ to +125℃
- **Wide Supply Voltage Range: 5V to 36V**
- **Low R_{DSON}: 86mΩ/Channel (TYP)**
- **Low Off-State Supply Current: 3.5μA (TYP)**
- **Current Sense Gain: 1655**
- **Built-in Variable Over-Current Mask-Time Setting Function**
- **Programmable Over-Current Limit: 2.5A, 5A, 10A, 15A**
- **3V and 5V Compatible Logic Inputs**
- **High Accurate Proportional Load Current Sense for Both Channels**
- **Continues Load Current:**
  - **3.5A, 1-Channel On**
  - **2.5A/CH, 2-Channel On**
- **Open-Load Detection in Off-State**
- **Short-to-GND Protection by Current Limit**
- **Thermal Shutdown with Latch or Restart Option**
- **Inductive Load Negative Voltage Clamp**
- **Loss of GND and Loss of Battery Protection**
- **Under-Voltage Shutdown**
- **Over-Voltage Clamp**

TYPICAL APPLICATION

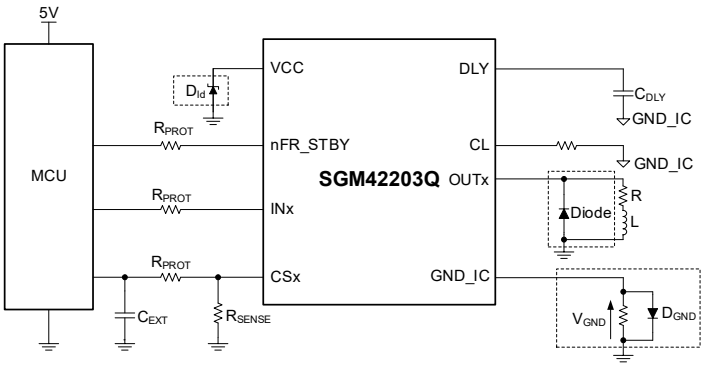


Figure 1. Application Schematic

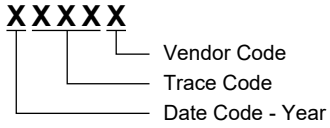
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PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM42203Q	TSSOP-16A (Exposed Pad)	-40℃ to +125℃	SGM42203QPTS16G/TR	MEJPTS16 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage, V_{CC} 60V
Reverse DC Supply Voltage, $-V_{CC}$ 0.3V
DC Reverse Ground Pin Current, $-I_{GND}$ 200mA (1)
DC Output Current, I_{OUT} ..... Internally limited
DC Input Current, I_{IN} ..... -1mA to 10mA (1)
Fault Reset Standby DC Input Current, I_{nFR_STBY} .....
.....-1mA to 1.5mA (1)
DC Reverse CS Pin Current, $-I_{CS}$ 200mA (1)
Current Sense Maximum Voltage, V_{CS} ..... V_{CC} - 58V to V_{CC}
Inductive Load Switch-Off Energy Dissipation, Single Pulse, Single Channel (2) 280mJ
Package Thermal Resistance
TSSOP-16A (Exposed Pad), θ_{JA} ..... 29.7℃/W
TSSOP-16A (Exposed Pad), θ_{JB} ..... 9℃/W
TSSOP-16A (Exposed Pad), $\theta_{JC\ (TOP)}$ ..... 22.7℃/W
TSSOP-16A (Exposed Pad), $\theta_{JC\ (BOT)}$ ..... 1.8℃/W
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility (3) (4)
HBM (VCC, OUTx Pins).....±6000V
HBM (All Other Pins) .....±4000V
CDM .....±1000V

NOTES:

1. Guaranteed by design, and not included in the production testing.
2. Test condition: V_{CC} = 24V, L = 300mH, R = 6.3Ω, I_L = 1.13A, T_A = +125℃. FR4 2s2p board, 2 × 70μm Cu, 2 × 35μm Cu. 600mm^2 thermal pad copper area.
3. For human body model (HBM), all pins comply with AEC-Q100-002 specification.
4. For charged device model (CDM), all pins comply with AEC-Q100-011 specification.

RECOMMENDED OPERATING CONDITIONS

Operating Ambient Temperature Range..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

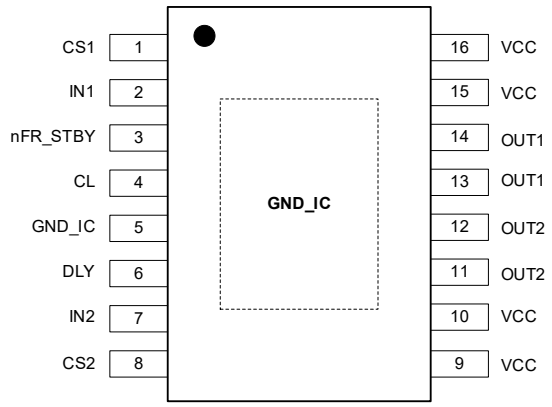
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TSSOP-16A (Exposed Pad)

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	CS1	Current Sense Output Pin. The out-going current is proportional to the load current. Connect it to the ground through a 10kΩ resistor if not used. It is not allowed to be floating.
8	CS2	
2	IN1	Voltage Controlled Input Pin. Control the output switch state. Connect it to the ground through a 10kΩ resistor if not used.
7	IN2	
3	nFR_STBY	Active-Low Reset Output/Standby Mode Pin. When over-temperature or over-current occurs and latches, pull nFR_STBY pin down to reset the device. If all the inputs and nFR_STBY pins are low, the device will enter into standby state. Connect it to the ground through a 10kΩ resistor if not used.
4	CL	Adjustable Current Limit. Connect respective resistor to GND_IC to set the current limit foldback level. If the current limit foldback function is not used, short this pin and the DLY pin to GND_IC.
5	GND_IC	Device Ground.
6	DLY	Over-Current Mask-Time Setting Pin. Connect respective capacitor to set the over-current mask-time. If the current limit foldback function is not used, short this pin and the CL pin to GND_IC.
9, 10, 15, 16	VCC	Power Supply. Short all the VCC pins together and connect to the supply. Do not let any of VCC pin floating.
13, 14	OUT1	Power Output. Do not connect to ground if the channel is not used, should leave it floating, there is an internal high-valued resistor as bleeding path.
11, 12	OUT2	
Exposed Pad	GND_IC	Device Ground.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V to 36V, T_A = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supplies							
Operating Supply Voltage	V_{CC}			5	24	36	V
Under-Voltage Lockout	V_{UVLO}				3.7	4	V
Under-Voltage Lockout Hysteresis	V_{UVLO_HYS}				0.5		V
On-Resistance/Channel	R_{ON}	I_{OUT} = 1.5A	T_A = +25℃		86		mΩ
			T_A = +125℃			150	
VCC Clamp Voltage	V_{CLAMP}	I_S = 20mA		60	73	85	V
Supply Current	I_Q	Off-state: V_{CC} = 24V, V_{IN} = V_{OUT} = V_{SENSE} = 0V, T_A = +25℃			3.5 (1)	8	μA
		On-state: V_{CC} = 24V, V_{IN} = 5V, I_{OUT} = 0A			5.5	6.5	mA
Off-State Output Current	I_{L_OFF}	V_{IN} = V_{OUT} = 0V, V_{CC} = 24V	T_A = +25℃	0	0.5	1	μA
			T_A = +125℃	0		2	
Output - VCC Diode Voltage	V_F	I_{OUT} = 1.5A, T_A = +125℃				0.96	V
Logic Inputs							
Low Level Input Voltage	V_{IL}					0.9	V
High Level Input Voltage	V_{IH}			2.3			V
Input Hysteresis Voltage	V_{I_HYS}			0.25			V
Low Level Input Current	I_{IL}	V_{IN} = 0.9V		0.5			μA
High Level Input Current	I_{IH}	V_{IN} = 2.3V				12	μA
Input Clamp Voltage	V_{ICL}	I_{IN} = 1mA		5.5		6.5	V
		I_{IN} = -1mA			-0.6		V
Low Level nFR_STBY Voltage	$V_{nFR_STBY_L}$					0.9	V
High Level nFR_STBY Voltage	$V_{nFR_STBY_H}$			2.3			V
nFR_STBY Hysteresis Voltage	$V_{nFR_STBY_HYS}$			0.25			V
Low Level nFR_STBY Current	$I_{nFR_STBY_L}$	V_{nFR_STBY} = 0.9V		0.5			μA
High Level nFR_STBY Current	$I_{nFR_STBY_H}$	V_{nFR_STBY} = 2.3V				12	μA
nFR_STBY Clamp Voltage	$V_{nFR_STBY_CL}$	I_{nFR_STBY} = 15mA (t < 10ms)		13.5		16	V
		I_{nFR_STBY} = -1mA			-0.7		
Standby Delay	t_{STBY}	See Figure 2		17		55	ms
Overload Latch-Off Reset Time	t_{RESET}	See Figure 3		2		24	μs
Open-Load Detection							
Open-Load Off-State Voltage Detection Threshold	V_{OL}	V_{IN} = 0V, V_{CC} = 5V to 36V, V_{nFR_STBY} = 5V		2		4	V
Output Short-Circuit to V_{CC} Detection Delay at Turn-Off	t_{DSTKON}	See Figure 4, V_{nFR_STBY} = 5V		200		1800	μs
Output Short-Circuit to V_{CC} Detection Delay at nFR_STBY Activation	$t_{DnFRSTK_ON}$	See Figure 5, INx = low				50	μs
Off-State Output Current at V_{OUT} = 4V	I_{L_OFF2}	V_{IN} = 0V, V_{SENSE} = 0V, V_{nFR_STBY} = 5V, V_{OUT} rising from 0V to 4V		-80		0	μA
Delay Response from Output Rising Edge to V_{SENSE} Rising Edge in Open-Load	t_{D_VOL}	V_{OUT} = 4V, V_{IN} = 0V, V_{SENSE} = 90% of V_{SENSEH}, R_{SENSE} = 3.9kΩ, V_{nFR_STBY} = 5V				20	μs
Switching (V_{CC} = 24V, T_A = +25℃) (see Figure 6)							
Turn-On Delay Time	t_{D_ON}	R_L = 16Ω			12		μs
Turn-Off Delay Time	t_{D_OFF}	R_L = 16Ω			45		μs
Turn-On Voltage Slope	dV_{OUT}/dt_{ON}	R_L = 16Ω			0.7		V/μs
Turn-Off Voltage Slope	dV_{OUT}/dt_{OFF}	R_L = 16Ω			0.65		V/μs
Switching Energy Losses during t_{WON}	W_{ON}	R_L = 16Ω			0.16		mJ
Switching Energy Losses during t_{WOFF}	W_{OFF}	R_L = 16Ω			0.17		mJ

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V to 36V, T_A = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Protections and Diagnostics						
CL Pin Current	I_{CL}	CL = 0V		10		μA
DLY Pin Current	I_{DLY}	DLY = 0V		10		μA
DC Short-Circuit Current	I_{LIMH}	V_{CC} = 24V	13	22	32	A
Short-Circuit Current during Thermal Cycling, I_{LIML_CX}	I_{LIML_C1}	V_{CC} = 24V, $T_R < T_A < T_{SD}$, DLY = open, CL = float		6.5		A
	I_{LIML_C2}	V_{CC} = 24V, $T_R < T_A < T_{SD}$, DLY = open, CL = 0.7V		6.5		
	I_{LIML_C3}	V_{CC} = 24V, $T_R < T_A < T_{SD}$, DLY = open, CL = 0.3V		5		
	I_{LIML_C4}	V_{CC} = 24V, $T_R < T_A < T_{SD}$, DLY = open, CL = 0V		2.5		
Custom Short-Circuit Current, I_{LIM_CX}	I_{LIM_C1}	V_{CC} = 24V, DLY = open, CL = float		15		A
	I_{LIM_C2}	V_{CC} = 24V, DLY = open, CL = 0.7V		10		
	I_{LIM_C3}	V_{CC} = 24V, DLY = open, CL = 0.3V		5		
	I_{LIM_C4}	V_{CC} = 24V, DLY = open, CL = 0V		2.5		
Thermal Shutdown Temperature	T_{SD}			145		℃
Thermal Hysteresis	T_{HYS}			10		℃
Reset Temperature (3)	T_R			110		℃
Turn-Off Output Voltage Clamp	V_{DEMAG}	V_{IN} = 0V, I_{OUT} = 10mA	V_{CC} - 49	V_{CC} - 60	V_{CC} - 71	V
Output Voltage Drop Limitation	V_{ON}	I_{OUT} = 50mA		4		mV
Current Sense						
I_{OUT}/I_{SENSE}	K_0 (2)	I_{OUT} = 0.1A, V_{SENSE} = 0.5V, T_A = -40℃ to +125℃	1200	1645	2150	
Current Sense Ratio Drift	dK_0/K_0	I_{OUT} = 0.1A, V_{SENSE} = 0.5V, T_A = +25℃	-5		5	%
I_{OUT}/I_{SENSE}	K_1 (2)	I_{OUT} = 0.4A, V_{SENSE} = 1V, T_A = -40℃ to +125℃	1500	1655	1850	
Current Sense Ratio Drift	dK_1/K_1	I_{OUT} = 0.4A, V_{SENSE} = 1V, T_A = +25℃	-5		5	%
I_{OUT}/I_{SENSE}	K_2 (2)	I_{OUT} = 0.8A, V_{SENSE} = 2V, T_A = -40℃ to +125℃	1550	1655	1800	
Current Sense Ratio Drift	dK_2/K_2	I_{OUT} = 0.8A, V_{SENSE} = 2V, T_A = +25℃	-5		5	%
I_{OUT}/I_{SENSE}	K_3 (2)	I_{OUT} = 1.5A, V_{SENSE} = 2V, T_A = -40℃ to +125℃	1550	1655	1800	
Current Sense Ratio Drift	dK_3/K_3	I_{OUT} = 1.5A, V_{SENSE} = 2V, T_A = +25℃	-5.5		5.5	%
I_{OUT}/I_{SENSE}	K_4 (2)	I_{OUT} = 6A, V_{SENSE} = 2V, T_A = -40℃ to +125℃	1550	1655	1800	
Current Sense Ratio Drift	dK_4/K_4	I_{OUT} = 6A, V_{SENSE} = 2V, T_A = +25℃	-5.5		5.5	%
Analog Sense Leakage Current	I_{SENSE0}	I_{OUT} = 0A, V_{SENSE} = 0V, V_{IN} = 0V			1	μA
		I_{OUT} = 0A, V_{SENSE} = 0V, V_{IN} = 5V			18	μA
Max Analog Sense Output Voltage	V_{SENSE}	V_{CC} = 24V, I_{OUT} = 6A, R_{SENSE} = 3.9kΩ	8			V
Analog Sense Output Voltage in Fault Condition (4)	V_{SENSEH}	V_{CC} = 24V, R_{SENSE} = 3.9kΩ	7.8	9	10.1	V
Analog Sense Output Current in Fault Condition (4)	I_{SENSEH}	V_{CC} = 24V, V_{SENSE} = 5V	3.6	7.35	11	mA
Delay Response Time from Rising Edge of INx Pin	$t_{DSENSE2H}$	V_{SENSE} < 4V, 0.07A < I_{OUT} < 6A, I_{SENSE} = 90% of I_{SENSE_MAX} (see Figure 7)		140	200	μs
Delay Response Time from Falling Edge of INx Pin	$t_{DSENSE2L}$	V_{SENSE} < 4V, 0.07A < I_{OUT} < 6A, I_{SENSE} = 10% of I_{SENSE_MAX} (see Figure 7)		5	20	μs
Delay Response Time between Rising Edge of Output Current and Rising Edge of Current Sense	$\Delta t_{DSENSE2H}$	V_{SENSE} < 4V, I_{SENSE} = 90% of I_{SENSE_MAX}, I_{OUT} = 90% of I_{OUTMAX}, I_{OUTMAX} = 1.5A (see Figure 8)			150	μs

NOTES:
1. PowerMOS leakage included.
2. Not include lifetime drift.
3. Reset temperature is about to release the fault and reset the I_{LIM} from I_{LIML_CX} to I_{LIMH}.
4. Fault condition includes: open-load in off-state, over-temperature and power-limiting condition.

TIMING DIAGRAM

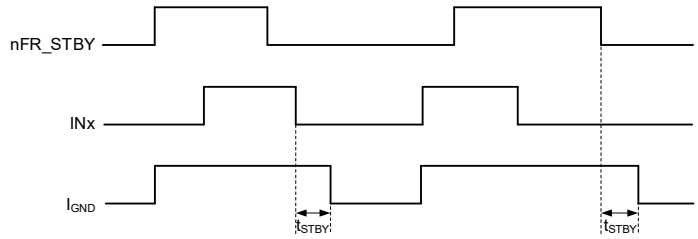


Figure 2. Standby Delay

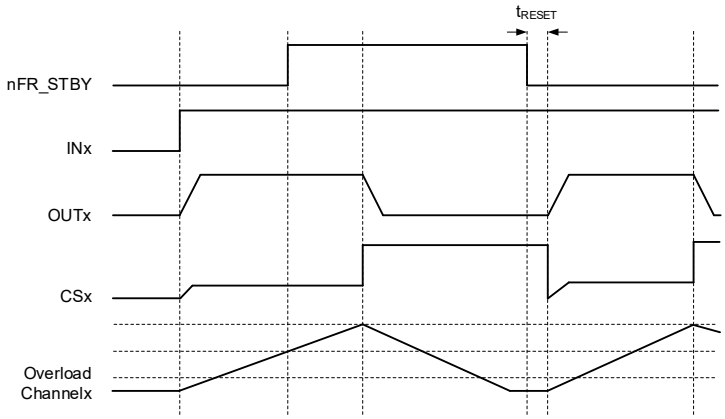


Figure 3. Overload Latch-Off Reset Time

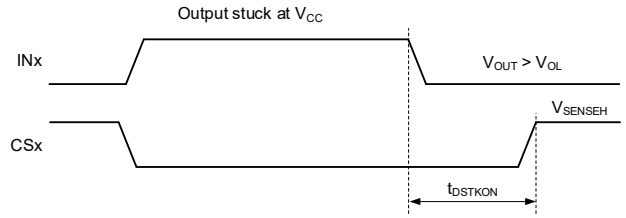
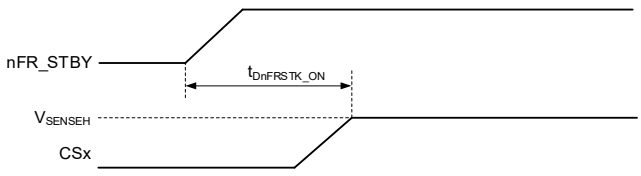


Figure 4. Open-Load Off-State Delay Timing



NOTE: The INx are logic low.

Figure 5. Output Stuck to V_{CC} Detection Delay Time at nFR_STBY Activation

TIMING DIAGRAM (continued)

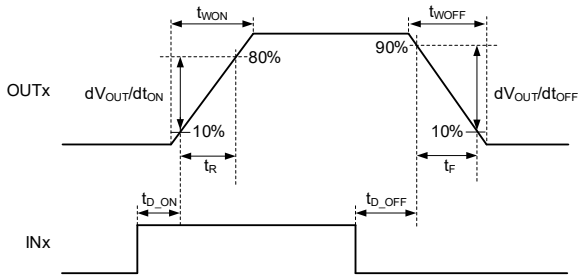


Figure 6. Switching Characteristics

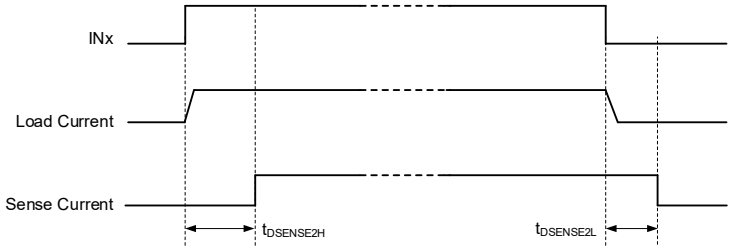


Figure 7. Current Sense Delay Timing

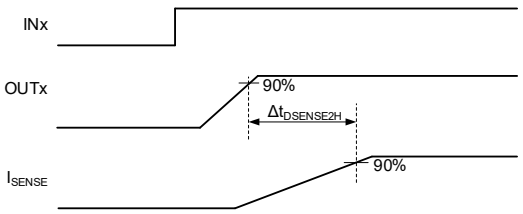


Figure 8. Delay Response Time between Rising Edge of Output Current and Rising Edge of Current Sense

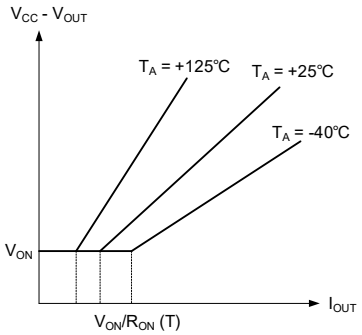
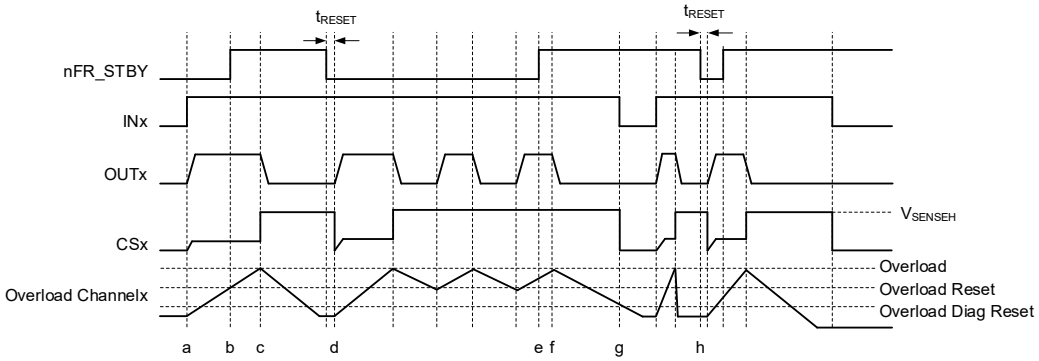


Figure 9. Output Voltage Drop Limitation

TIMING DIAGRAM (continued)

The device behavior in overload condition is shown in Figure 10.

At point a, the input is set to high, output is on and CS senses the load current. At point b, the nFR_STBY is set to high. At point c, when nFR_STBY is high and over-current event happens, output is latched off, and CS is high to report the fault. At point d, nFR_STBY is set low, and the over-current latch is reset after t_{RESET} time. During d to e term, nFR_STBY is low and input is high, the device keeps thermal cycling, and CS keeps high. At point e, nFR_STBY is high, the latch-off reset function is disabled. During f to g term, when nFR_STBY is high and over-current event happens, output is latched off. During g to h term, the CS pin is high, diagnostic function is transfered between enabled and disabled by INx pin. At point h, nFR_STBY is low, latch-off reset function is enabled.



NOTE: Overload is thermal shutdown or power-limiting.

Figure 10. Device Behavior in Overload Condition

Table 1. Truth Table

Conditions	nFR_STBY	INx	OUTx	CSx
Standby	L	L	L	0
Under-Voltage	X	X	L	0
Normal	X	L	L	0
	X	H	H	Nominal
Overload	X	L	L	0
	X	H	H	V_{SENSEH}
Short-to-VCC	L	L	H	0
	H	L	H	V_{SENSEH}
	X	H	H	< Nominal
Over-Temperature/Short-to-Ground	X	L	L	0
	L	H	Cycling	V_{SENSEH}
	H	H	Latched	V_{SENSEH}
Open-Load Off-State (with Pull-Up)	L	L	H	0
	H	L	H	V_{SENSEH}
	X	H	H	0
Negative Output Voltage Clamp	X	L	Negative	0

ELECTRICAL TRANSIENT REQUIREMENTS

Table 2. Electrical Transient Requirements (Part 1)

ISO 7637-2: 2004(E) Test Pulse	Test Levels (1)		Number of Pulses or Test Times	Burst Cycle/Pulse Repetition Time		Delays and Impedance
	III	IV				
1	-450V	-600V	5000 pulses	0.5s	5s	1ms, 50Ω
2a	+37V	+50V	5000 pulses	0.2s	5s	50μs, 2Ω
3a	-150V	-200V	1h	90ms	100ms	0.1μs, 50Ω
3b	+150V	+200V	1h	90ms	100ms	0.1μs, 50Ω
3b	+150V	+200V	1h	90ms	100ms	0.1μs, 50Ω
4	-12V	-16V	1 pulse			100ms, 0.01Ω
5b (2)	+123V	+174V	1 pulse			350ms, 1Ω

Table 3. Electrical Transient Requirements (Part 2)

ISO 7637-2: 2004(E) Test Pulse	Test Level Results	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b (1)	E	E
3b (2)	C	C
4	C	C
5b (3)	C	C

NOTES:

1. There is no capacitor between VCC and GND.
2. Connect a 10nF capacitor from VCC to GND.
3. External load dump clamp, 58V (MAX), referred to ground.

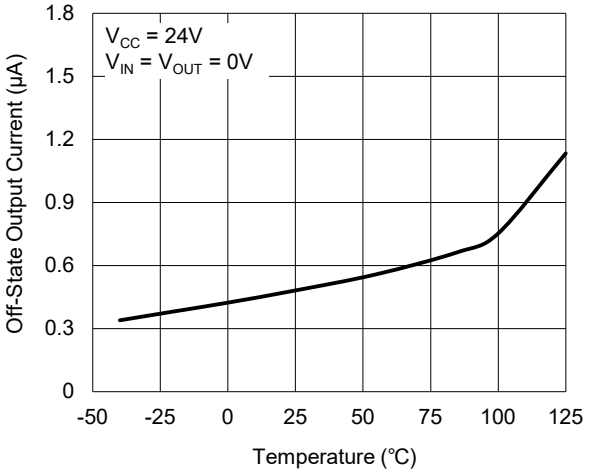
Table 4. Electrical Transient Requirements (Part 3)

Class	Contents
C	After the device is disturbed, all functions can be performed as designed.
E	After the device is disturbed, all functions can not be performed as designed. And it can not be recovered if the device is not replaced.

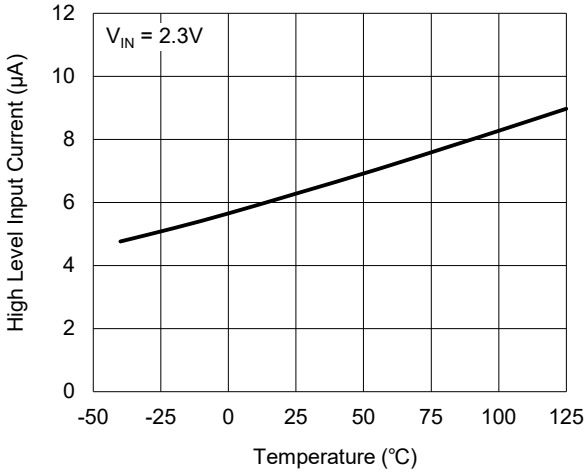
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, unless otherwise noted.

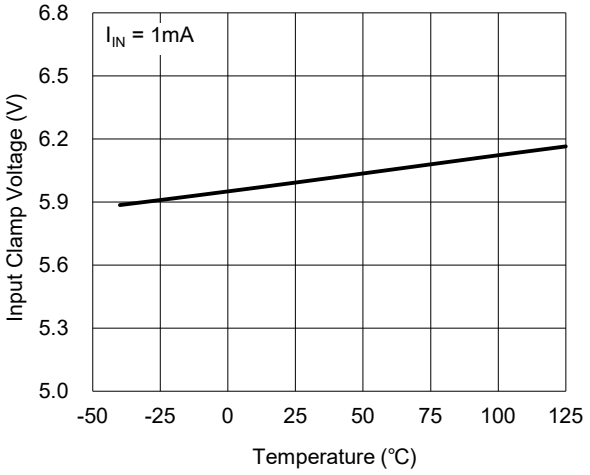
Off-State Output Current vs. Temperature



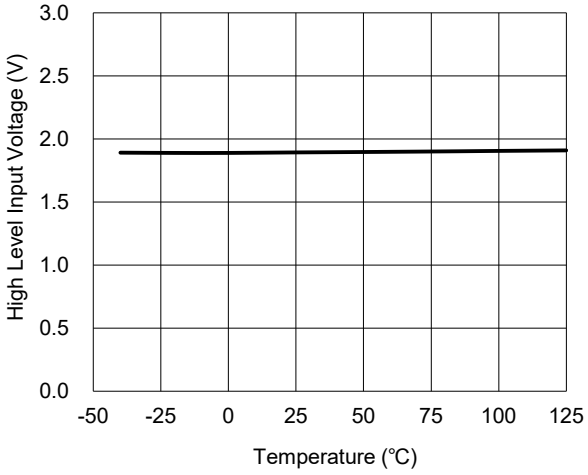
High Level Input Current vs. Temperature



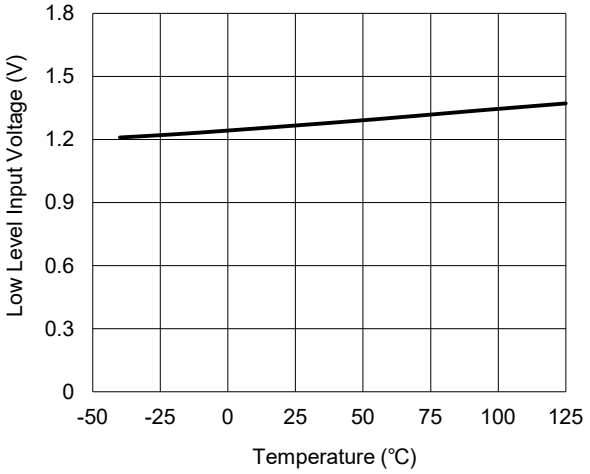
Input Clamp Voltage vs. Temperature



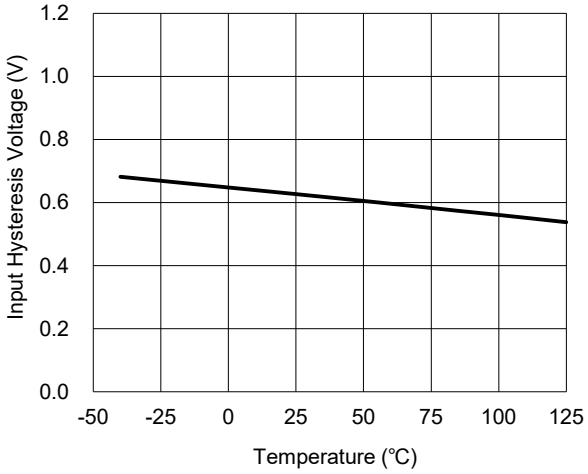
High Level Input Voltage vs. Temperature



Low Level Input Voltage vs. Temperature



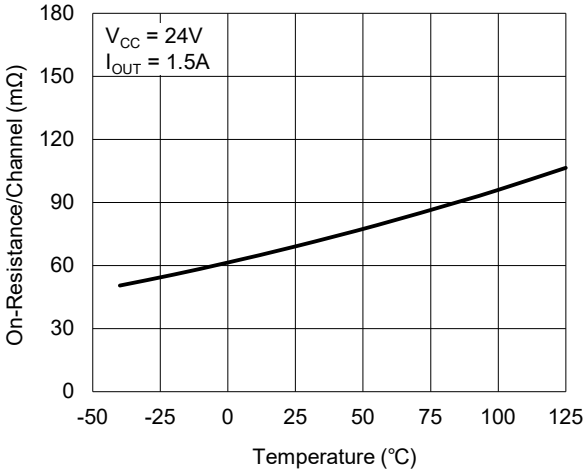
Input Hysteresis Voltage vs. Temperature



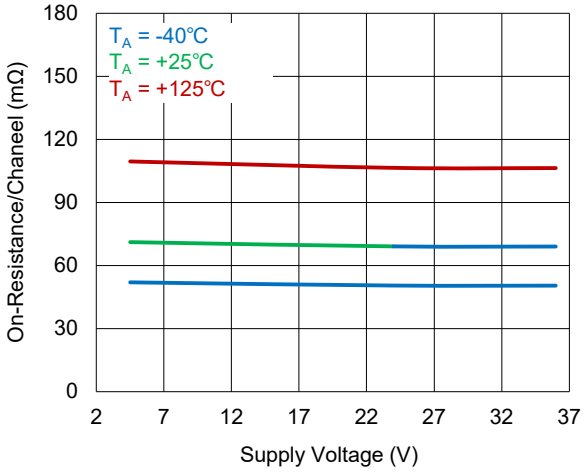
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

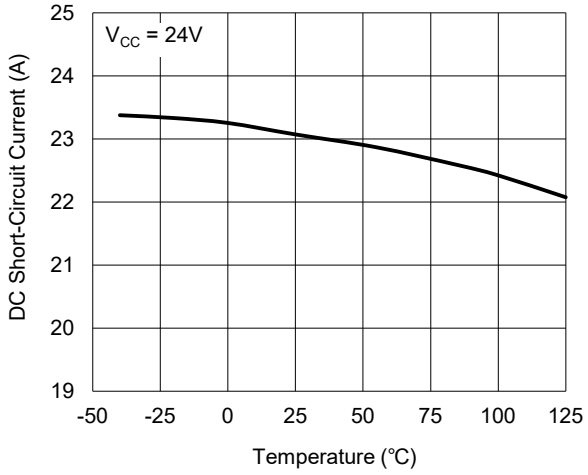
On-Resistance/Channel vs. Temperature



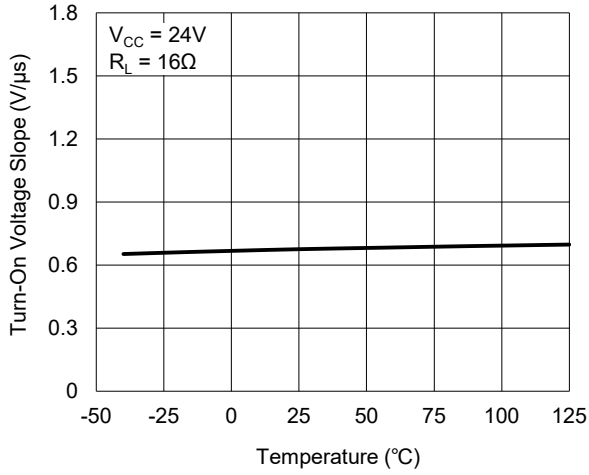
On-Resistance/Channel vs. Supply Voltage



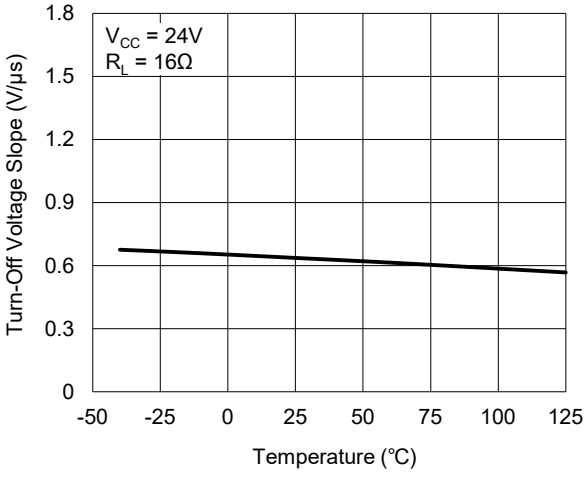
DC Short-Circuit Current vs. Temperature



Turn-On Voltage Slope vs. Temperature



Turn-Off Voltage Slope vs. Temperature



FUNCTIONAL BLOCK DIAGRAM

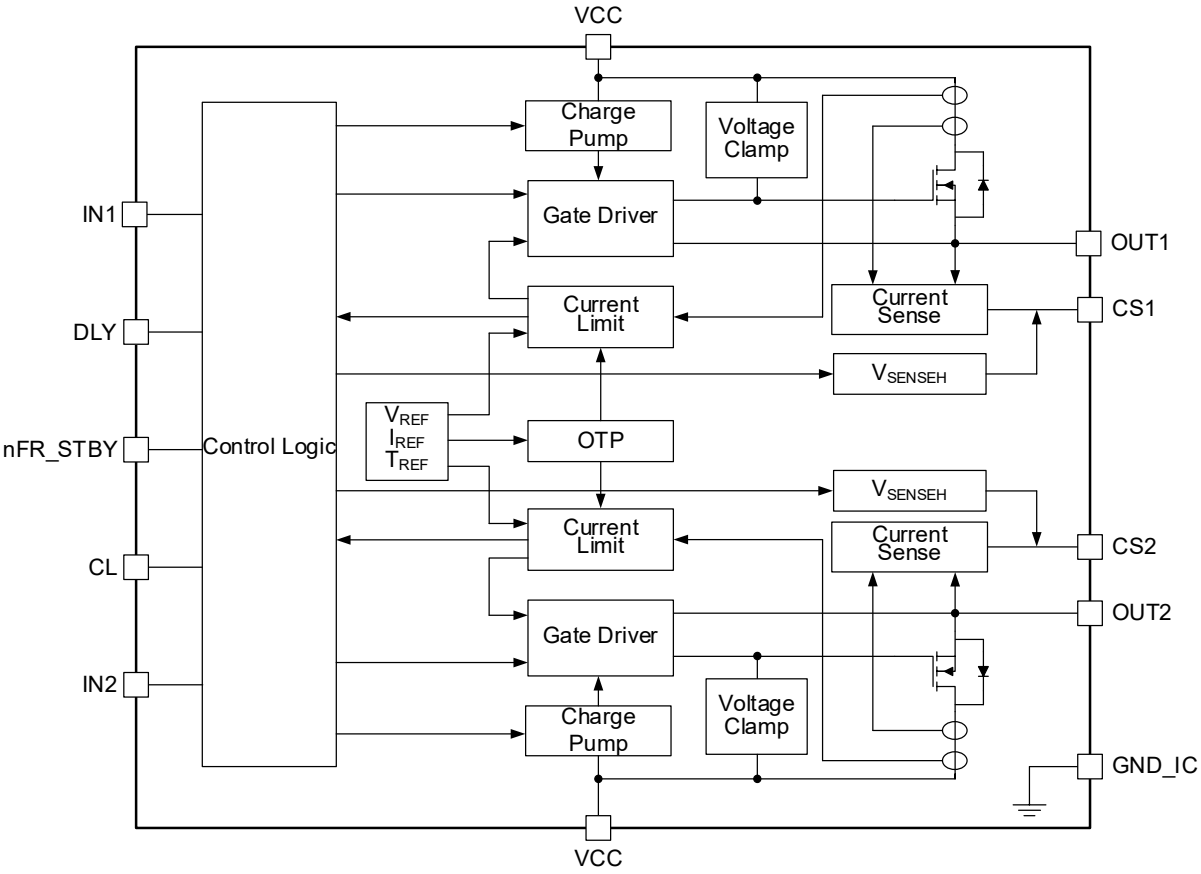


Figure 11. Block Diagram

DETAILED DESCRIPTION

Adjustable Current Limit

The device has two current limit functions. Internal over-current limit (I_{LIMH}): the internal current limit is fixed at I_{LIMH} for protecting the device. External variable current limit: an external resistor connected to CL pin is used to set the current limit threshold. Variable over-current limit (I_{LIM_CX}) is used to protect the load. The over-current mask-time t_{DLY} is set by the capacitor connected between DLY and GND_IC. Please refer to fixed over-current setting (I_{LIMH}) to adjustable over-current limit (I_{LIM_CX}) shown in Figure 12.

C_{DLY} is charged by 10μA (TYP) when output current goes higher than I_{LIM_CX}. Output current is limited to I_{LIM_CX} when DLY voltage reaches about 1.4V (TYP).

Over-Current Detection in Both Channels

The device detects and protects over-current in both channels independently. Please refer to the timing diagram in Figure 13.

When the current of channel 1 goes higher than I_{LIM_CX}, the capacitor connected to DLY pin (C_{DLY}) is charged with 10μA (TYP). After the DLY voltage reaches about 1.4V (TYP), the current of channel 1 foldback to I_{LIM_CX}, and the C_{DLY} is discharged to GND_IC.

Then when the current of channel 2 current goes higher than I_{LIM_CX}, the C_{DLY} is charged with 10μA (TYP). After the DLY voltage reaches about 1.4V (TYP), the current of channel 2 foldback to I_{LIM_CX} and the C_{DLY} is discharged to GND_IC.

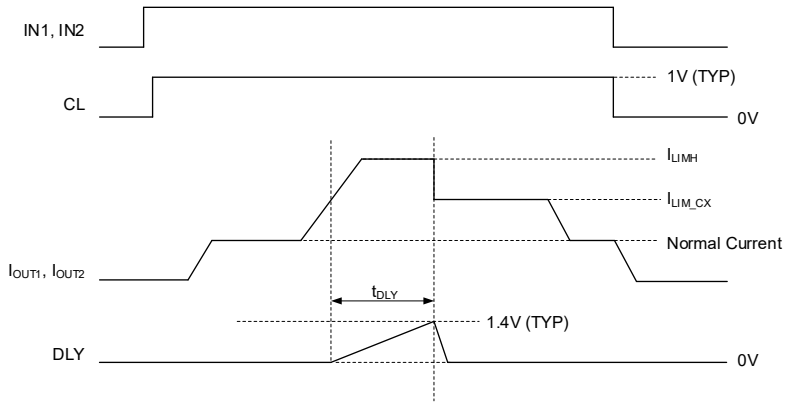


Figure 12. Timing Chart for Over-Current Detected in One Side Channel

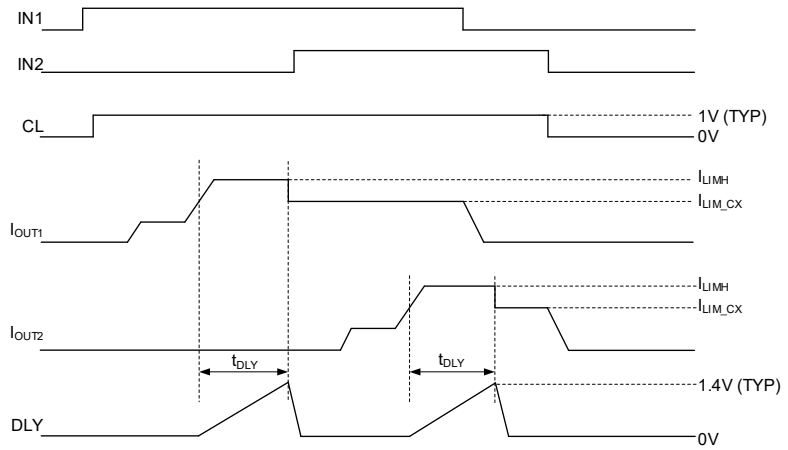


Figure 13. Timing Chart for Over-Current Detection in Both Outputs

DETAILED DESCRIPTION (continued)

Over-Current Detection by Other Channel while C_{DLY} is Charging (t_{DLY})

When C_{DLY} is charged, if the output current of another channel is higher than I_{LIM_CX}, then the adjustable over-current mask-time for the channel can reach I_{LIM_CX}, and the time can reaches up to 2 × t_{DLY} + t_{DISC} later. Please refer to the timing chart in Figure 14.

When the current of channel 1 goes higher than I_{LIM_CX}, the C_{DLY} is charged with 10μA (TYP). After the DLY voltage reaches about 1.4V (TYP), the current of channel 1 returns to I_{LIM_CX}, and the C_{DLY} is discharged.

When the current of channel 2 is still higher than I_{LIM_CX} after t_{DISC} (0.2μs, TYP), the C_{DLY} is recharged again with 10μA (TYP). After the DLY voltage reaches about 1.4V (TYP), the current of channel 2 returns to I_{LIM_CX} and the C_{DLY} is discharged.

Adjustable Over-Current Limit Mask-Time

The t_{DLY} adjustable over-current mask-time is set by the capacitor from DLY pin to GND_IC.

$$t_{DLY} = 140000 \times C_{DLY}\ (s) \quad (1)$$

C_{DLY} is the capacitor connected from DLY pin to GND_IC. And t_{DLY} is the adjustable over-current mask-time.

The CL Pin and the DLY Pin Setting

Besides connecting a capacitor to GND_IC, the DLY pin can also be open or short-to-GND_IC.

DLY = GND_IC: when DLY pin is short-to-GND_IC, the adjustable over-current limit foldback function is disabled.

DLY = Open: when DLY pin is open, the mask-time is 10μs or less.

The CL pin has 10μA out-bias current.
For CL pin is short-to-GND_IC, the I_{LIMIT} is 2.5A.
For 0.2V ≤ V_{CL} < 0.45V, the I_{LIMIT} is 5A.
For 0.45V ≤ V_{CL} < 1V, the I_{LIMIT} is 10A.
For CL pin is open, the I_{LIMIT} is 15A.

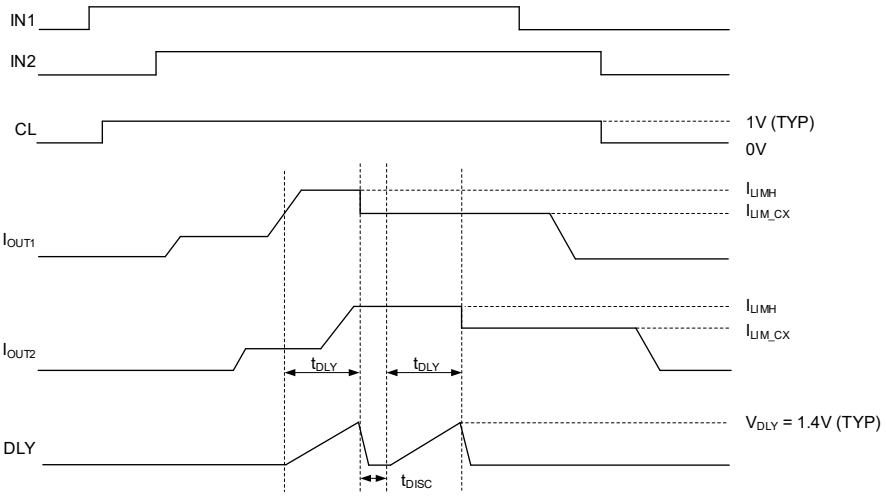


Figure 14. Timing Chart for Over-Current Detected by Other Channel during C_{DLY} Charging (t_{DLY})

DETAILED DESCRIPTION (continued)

Inductive Load Switch-Off Clamp

When an inductive load is turned off, the stored magnetic energy of the inductor tends to keep the inductor current flowing. This induces a large voltage across drain-source because switch resistance is increasing during turn-off and results in a negative output voltage. If the negative voltage is too large, it can break down and damage the MOSFET. An internal clamp is activated across the switch to limit the voltage to V_{DS_CLAMP} (60V) and circulate and damp the current until inductor stored energy is dissipated. The V_{DS_CLAMP} results in a negative load voltage (see Figure 15 and Figure 16).

$$V_{DS_CLAMP} = V_{CC} - V_{OUT} \quad (2)$$

During demagnetization (t_{DEMAG}), the high-side driver is kept on in active region (but not saturated) to dissipate the magnetic energy. In the clamping period, the total energy dissipated in the high-side driver (E_{HSD}), includes the inductor energy (E_L), and the energy coming from the power supply (E_{VCC}), but a portion of the load energy is dissipated in its own series resistance, E_R (that is $E_{LOAD} = E_L - E_R$), so:

$$E_{HSD} = E_{VCC} + E_L - E_R \quad (3)$$

E_{HSD} causes thermal stress on the switch and the whole device during turn-off. The maximum power that the device can dissipate depends on its thermal capacity, ambient temperature, and PCB heat sinking capability. E_{HSD} can be calculated from Equation 4:

$$E_{HSD} = \int_0^{t_{DEMAG}} V_{DS_CLAMP} \times I_{OUT}(t)dt$$

where,

$$t_{DEMAG} = \frac{L}{R} \times \ln\left(\frac{R \times I_{OUT} + |V_{OUT}|}{|V_{OUT}|}\right)$$

So

$$E_{HSD} = L \times \frac{V_{CC} + V_{OUT}}{R^2} \times \left[R \times I_{OUT} - |V_{OUT}| \ln\left(\frac{R \times I_{OUT} + |V_{OUT}|}{|V_{OUT}|}\right)\right] \quad (4)$$

When R is insignificant (R ≈ 0), E_{HSD} simplifies as:

$$E_{HSD} = \frac{1}{2} \times L \times I_{OUT}^2 \frac{V_{CC} + |V_{OUT}|}{|V_{OUT}|} \quad (5)$$

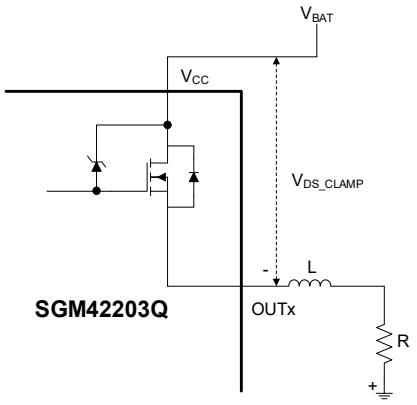


Figure 15. Drain-to-Source Clamping to V_{DS_CLAMP}

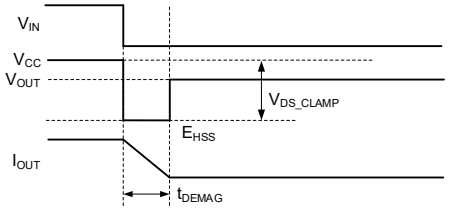


Figure 16. Inductive Load Switch-Off and Clamping

High Accurate Proportional Load Current Sense

The device integrates high-precision current sensing, which provides the voltage across the external resistor (R_{SENSE}) under normal conditions, and the N/N ratio is proportional to the load current (so-called K coefficient, specified in the reference datasheet):

$$V_{SENSE} = R_{SENSE} \times I_{SENSE} = R_{SENSE} \times (I_{OUT}/K) \quad (6)$$

The CS pin allows monitoring the current flowing through the load and detecting fault conditions, such as open-load, overload, over-current and thermal shutdown. In case of thermal shutdown or power limit, the CS pin will output voltage source V_{SENSEH} (9V, TYP), I_{SENSEH} (7.35mA, TYP) and keep it in the thermal shutdown or latch-off mode.

Example of R_{SENSE} resistance selection:

When device under the nominal load current, I_{NOM} = 1.5A, V_{SENSE} = 2V refer to typical value K_3 = 1655 (specification):

$$R_{SENSE} = K \times (V_{SENSE}/I_{OUT}) = 1655 \times (2V/1.5A) = 2.2k\Omega$$

APPLICATION INFORMATION

Reverse Battery Protection with External Ground Network

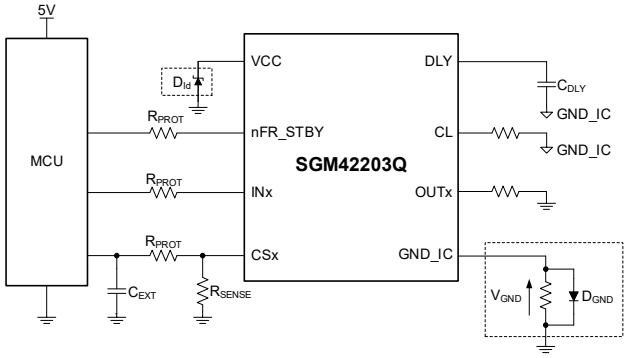


Figure 17. Reverse Battery Protection with External Ground Network

D_{GND} in the GND Line

Adding a GND network. The reverse current through the GND_IC is blocked. The reverse current through the FET is limited by the load itself. A resistor in parallel with the diode is recommended as a GND network. The recommended selection is 4.7kΩ resistor in parallel with the diode.

The reverse current protection diode will bring about 0.6V level shift on the input voltage threshold.

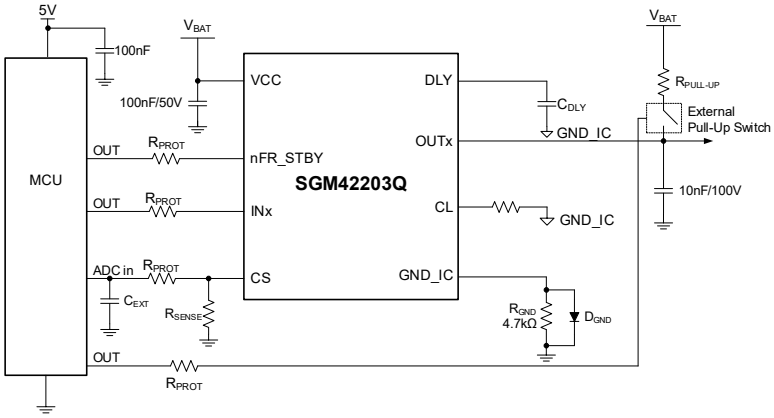


Figure 18. Open-Load Detection in Off-State

APPLICATION INFORMATION (continued)

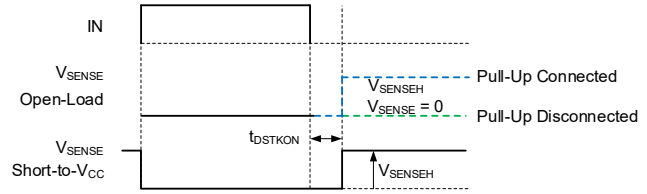


Figure 19. Open-Load/Short-to-VCC

Table 5. Current Sense Pin Levels in Off-State

Condition	Output	CS
Open-Load	$V_{OUT} > V_{OL}$	V_{SENSEH}
	$V_{OUT} < V_{OL}$	0
Short-to-VCC	$V_{OUT} > V_{OL}$	V_{SENSEH}
Nominal	$V_{OUT} < V_{OL}$	0

Short-to-Battery

In off-state, short-to-battery has the same detection mechanism and behavior as open-load detection.

Off-State Open-Load Pull-Up Resistor

There is always a leakage current I_{L_OFF} present on the output due to internal logic control path or external humidity, corrosion, and so forth. In off-state, external pull-up resistor is needed for open-load detection. R_{PU} should be selected to make sure that $V_{OUT} > V_{OL_MAX}$, please refer to the calculation below:

$$R_{PU} < \frac{V_{PU} - 4}{I_{L_OFF_MIN}@4V} \quad (7)$$

Application Note

NOTE: If there is a level shift between the GND_IC of the device and the GND of the system board when the GND network is used, for example, the device GND_IC and the system GND are protected against reversing battery through a diode parallel resistor. At this time, to set the current limit level and current limit mask time function, it is necessary to ensure that the CL and DLY pins refer to the GND_IC of device.

When abrupt short-to-ground event happens after the channel is turned on, a fast current limit will kick in right away to limit the inrush current peak to around 40A. Then in usually less than 40μs, the current will be downward regulated to the I_{LIMH} level. With this fast current limit, more robust short-circuit performance is achieved.

The automotive application environment of high-side driver is very complex, it involves variety of loads (resistive, capacitive, inductive), and variety of fault events (short-circuit, loss-of-power, loss-of-GND, battery reverse). It is recommended to add external measures to ensure stability and robustness of the system.

For inductive load controlled by PWM switch, it is recommended to add an external freewheeling circuitry loop as shown in Figure 20 below, to protect the high-side driver device from repeated power stress shock during repeated switching.

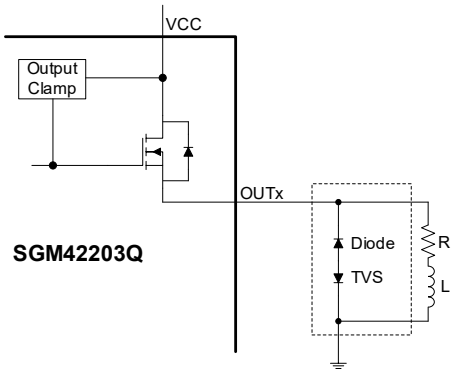


Figure 20. External Circuit Protection Inductive Load Turn-Off

A TVS device in series with a diode realize inductive load turn-off demagnetization with relatively fast decay time.

When the large inductive load is directly driven to turn off, and the high-side driver is not enough to withstand the demagnetization heat, it is recommended to add the external freewheeling diode circuit as shown in Figure 21. It provides re-circulating current path for the large inductive load when the high-side driver is cut-off. However, due to the low forward-voltage of the freewheeling diode, the decay time of the inductive load current is slow.

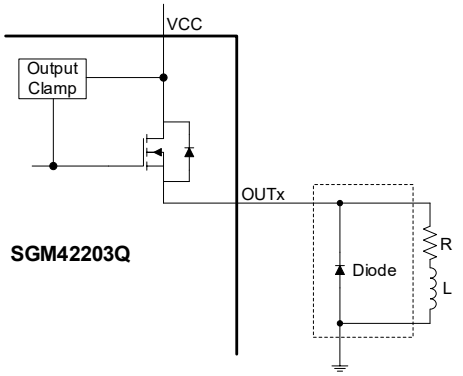


Figure 21. Freewheeling Circuitry Protects the Inductive Load Turn-Off Demagnetization

APPLICATION INFORMATION (continued)

Selection and recommendation of freewheeling diode:

- The reverse voltage value of the diode is selected to be greater than the V_{CC} supply voltage to avoid breakdown of the diode during normal use.
- To select the maximum forward rectified current of the diode, it is necessary to ensure that the current of the inductive load discharged through the freewheeling diode does not exceed the maximum forward rectified current, so as not to burn out the diode.
- For freewheeling diodes, fast recovery diodes or Schottky diodes are recommended.
- TVS diode reverse voltage withstand value is less than 60V - V_{CC}, to avoid damage the chip internal clamping circuit.

In the event of a power loss failure, the output of the high-side driver will turn off the protection regardless of whether the INx pin is high or low. For resistive or capacitive loads, loss of power failure does not pose a great risk. However, for the inductive load of charging and storing energy, the inductive current cannot change to zero when the power is lost, and it needs to be driven to maintain the inductive current. To protect the system in this case, it is recommended to add two kinds of external protection circuits: GND network or external freewheeling diode, as shown in Figure 22 and Figure 23 below.

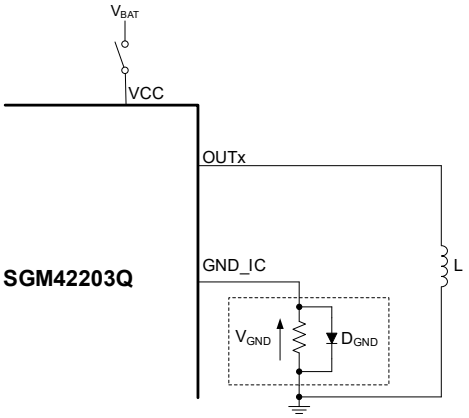


Figure 22. GND Network Protections for Loss of Power

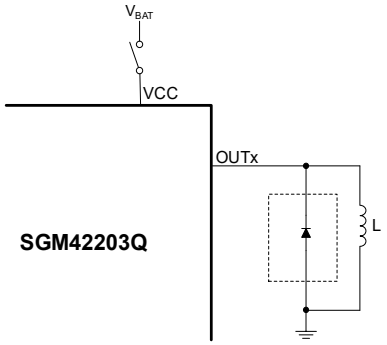


Figure 23. Loss of Power Protection Added Freewheeling Diode Protection

In some harsh conditions, such as ISO 7637-2: 2004(E) test pulse or the loss of power with inductive load, and a pulse appears on the negative GND pin, which can cause damage to the connected microcontroller. It is recommended to add the serial resistor protecting the microcontroller to the input pin of the high-side driver.

$$\frac{V_{PEAK}}{I_{(\mu C)LATCHUP}} \le R_{PROT} \le \frac{V_{OH} - (V_{IH} + V_{GND})}{I_{IH}} \quad (8)$$

Example:

$$\frac{600V}{20mA} \le R_{PROT} \le \frac{4.5V - (2.3V + 0.6V)}{12\mu A}$$

$$30k\Omega \le R_{PROT} \le 133.3k\Omega$$

As shown in Figure 24 below, the 56kΩ resistor is used for microcontroller.

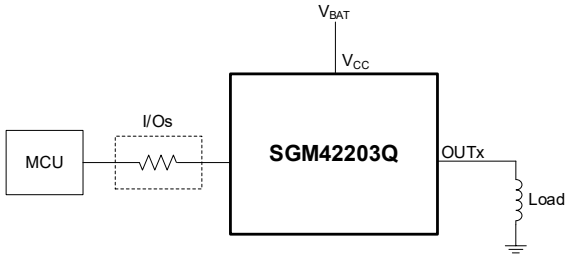


Figure 24. External Protections of Controller I/O Pins

APPLICATION INFORMATION (continued)

Due to complex wiring environment inside the automotive system, abrupt short may happen after long haul wiring. When that happens, high parasitic inductance of long-haul wiring generates high negative voltage spikes to the output of the high-side driver. To protect the high-side driver from damaging by the uncontrolled high negative voltage spikes, it is recommended to add two kinds of external protection circuits to provide safe re-circulating current path for the parasitic inductance of the wiring to de-energize.

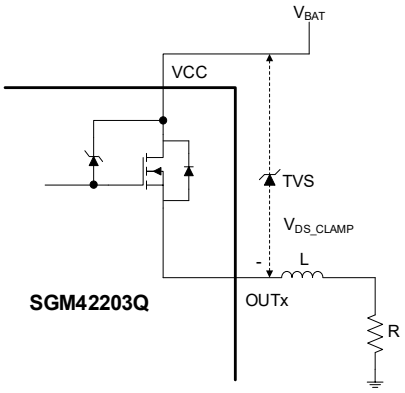


Figure 25. Increase TVS Diode Breakdown Release Output Negative Voltage

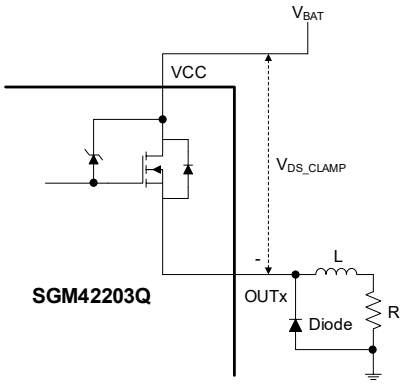


Figure 26. Freewheeling Diode Provides Output Negative Voltage Release Loop

As shown in Figure 27, the CSx Pin voltage is usually connected to the ADC input or I/O interface of the microcontroller through a protection resistor of 56kΩ. For the V_{SENSEH} level, the voltage of 9V (TYP) will be limited and protected by the internal ESD of the microcontroller pin, or you can refer to Figure 27 to add Zener diode to protect the pin for voltage stabilization. The Zener diode is selected according to the actual MCU pin withstand voltage. Capacitor (C_{EXT}) is used to improve the accuracy of V_{SENSE} measurement. Together with the 56kΩ series resistor, a low-pass filter (cutoff frequency of about 2.8kHz) is formed to detect the potential HF noise on the CS line. The capacitor should be connected close to the pin of the microcontroller.

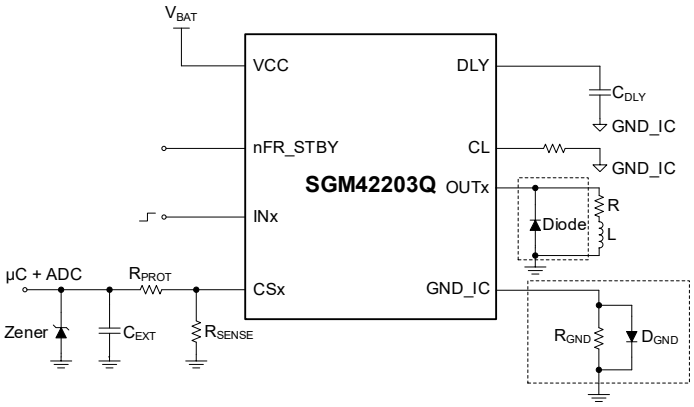


Figure 27. CS Output for Current Sense and Fault State

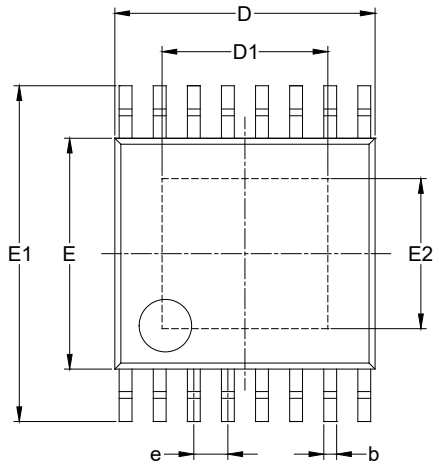
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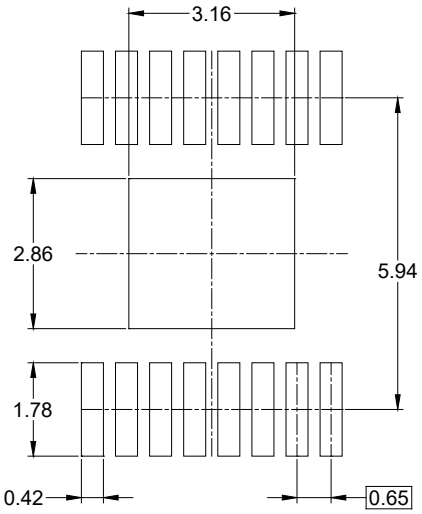
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (FEBRUARY 2025) to REV.A	Page
Changed from product preview to production data	All

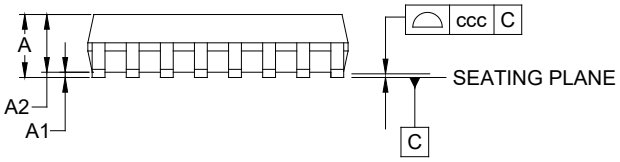
PACKAGE OUTLINE DIMENSIONS

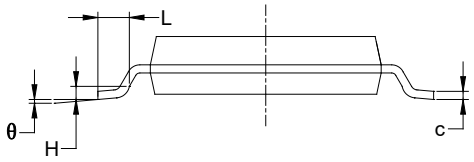
TSSOP-16A (Exposed Pad)





RECOMMENDED LAND PATTERN (Unit: mm)



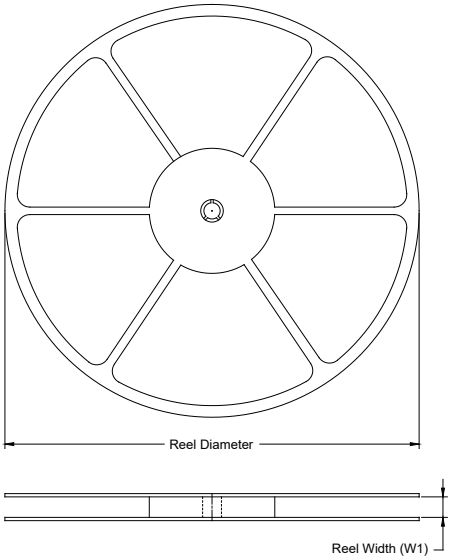


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.200
A1	0.000	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	4.860	-	5.100
D1	2.960	-	3.360
E	4.300	-	4.500
E1	6.200		6.600
E2	2.660	-	3.060
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

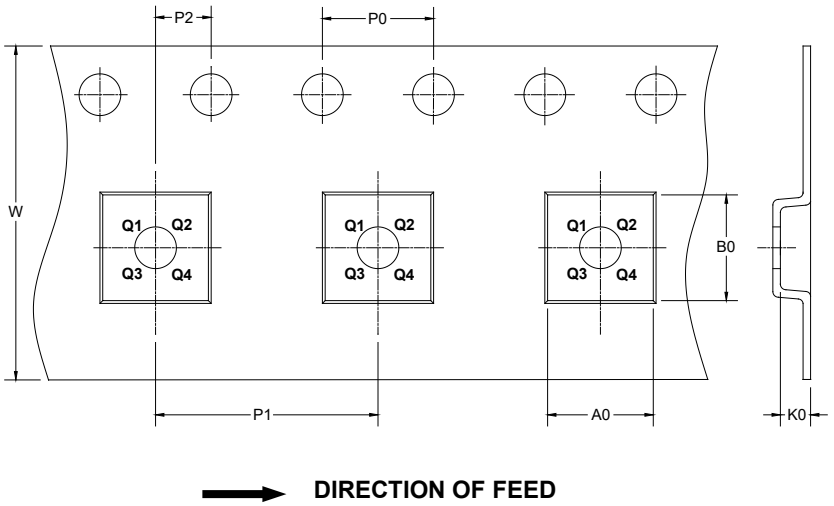
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

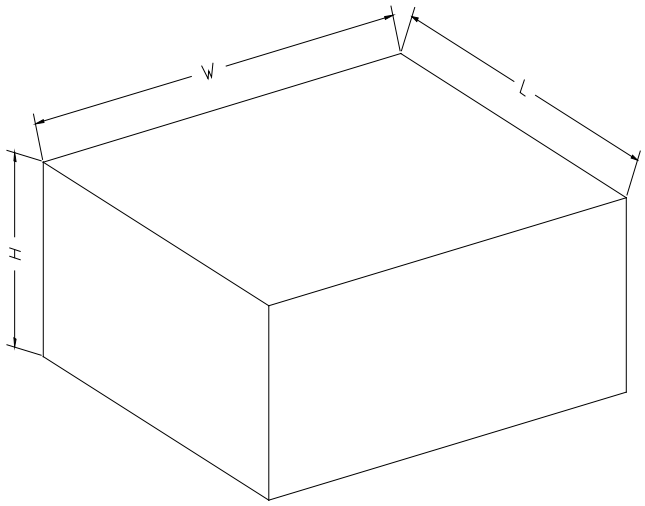
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-16A (Exposed Pad)	13"	12.4	6.80	5.40	1.50	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002