SGM37460Q
Automotive 6-CH, 150mA (MAX) Each, Boost WLED Driver with 15000:1 Dim Ratio and I²C Interface

GENERAL DESCRIPTION

The SGM37460Q is a 6-channel high current LCD backlight display driver with integrated Boost converter.

The SGM37460Q adopts peak current mode control for the output voltage regulation of the Boost converter. The device implements an external PMOS gate control for load disconnect. The device integrates 6 well-matched constant current sinks to control the LED string's brightness, and each channel can provide up to 150mA constant current. The SGM37460Q provides PWM, mix and analog dimming modes. It can be set either via MIX/AD pin or I²C interface. It also has a phase-shift function to eliminate noise during PWM dimming.

The SGM37460Q integrates a 90mΩ Boost power, combined with adaptive Boost output voltage adjustment to achieve excellent efficiency. The device implements a standard I²C interface to maximize user programmability. The Boost converter's switching frequency can be programmed by a resistor up to 2.2MHz, or via I²C interface. External clock signal can also be synchronized with SGM37460Q to set the Boost converter's switching frequency.

The SGM37460Q integrates various protection features such as Boost over-current protection (OCP), Boost over-voltage protection (OVP), over-temperature protection (OTP), LED open protection, LED short protection and short LEDx-to-GND protection. In addition, the device integrates a sink current fold-back feature to reduce the sink channel current when device temperature rises above +140℃.

The device is AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and it is suitable for automotive applications.

The SGM37460Q is available in a Green TQFN-4×4-24EL package with wettable flank.

FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
  Device Temperature Grade 1
  T_A = -40℃ to +125℃
- **Input Voltage Range: 3.5V to 36V**
- **I²C Interface**
- **Dedicated Fault Status Pin**
- **Device Thermal Shutdown**

Boost Converter:

- **Internal 90mΩ Power MOSFET**
- **Programmable f_{SW} up to 2.2MHz**
- **External Frequency Synchronization**
- **Low EMI Frequency Spread Spectrum**
- **Load Disconnect Switch Control**
- **Cycle-by-Cycle Current Limit**
- **Short Inductor Protection**
- **Programmable OVP Threshold**

LED Sink:

- **Up to 6 High-Precision Current Sinks, and Support:**
  - **6 Channel, 10 LEDs in series at 150mA Each**
  - **6 Channel, 12 LEDs in series at 120mA Each**
  - **4 Channel, 12 LEDs in series at 150mA Each**
- **Programmable Dimming Options:**
  - **Direct PWM Dimming**
  - **Analog Dimming**
  - **Mix Dimming with 25%/12.5% Transfer Point**
- **Phase-Shift Function**
- **15000:1 Dim Ratio in PWM Dim at f_{PWM} ≤ 200Hz**
- **255:1 Dim Ratio at Analog Dim through PWM Dim Signal Input**
- **2.5% Channel-to-Channel Matching**
- **Optional Over-Temperature LED Current Reduction**
- **LED Short and Open Protections**
- **Programmable LED Short Threshold**
- **Available in a Green TQFN-4×4-24EL Package with Wettable Flank**

APPLICATIONS

LCD Backlight Display Driver

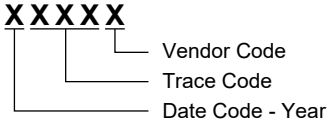
代理商 威尔逊 www.visvie.com 联系电话 138 2526 5270

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM37460Q	TQFN-4×4-24EL	-40℃ to +125℃	SGM37460QTVX24G/TR	1GETVX24 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage, V_{IN} ..... -0.3V to 42V
SW, LED1 to LED6 Pin Voltages ..... -0.5V to 45V
SW Pin Voltage ..... -1.0V for < 100ns
DIS Pin Voltage ..... V_{IN} - 6V to V_{IN}
All Other Pins ..... -0.3V to 5.5V
Package Thermal Resistance
TQFN-4×4-24EL, θ_{JA} ..... 29.4℃/W
TQFN-4×4-24EL, θ_{JB} ..... 8.5℃/W
TQFN-4×4-24EL, $\theta_{JC\ (TOP)}$ ..... 21.5℃/W
TQFN-4×4-24EL, $\theta_{JC\ (BOT)}$ ..... 3.0℃/W
Package Thermal Characterization Parameter
TQFN-4×4-24EL, ψ_{JT} ..... 0.8℃/W
TQFN-4×4-24EL, ψ_{JB} ..... 8.1℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±3000V
CDM ..... ±2000V

NOTES:

1. For human body model (HBM), all pins comply with AEC-Q100-002 specification.

2. For charged device model (CDM), all pins comply with AEC-Q100-011 specification.

RECOMMENDED OPERATING CONDITIONS

Input Voltage, V_{IN} ..... 3.5V to 36V
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

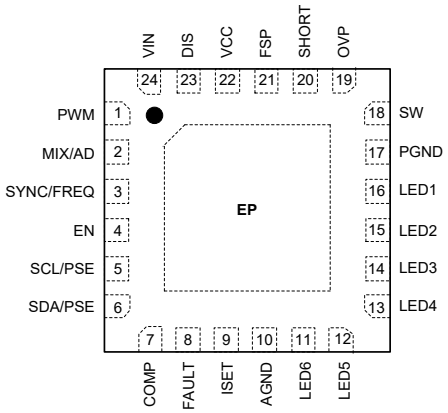
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-4×4-24EL

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	PWM	PWM Signal Input Pin for Brightness Control. Recommended PWM frequency: 100Hz to 20kHz. The high/low time of the PWM signal should be ≥ 150ns.
2	MIX/AD	Dimming Mode Program Pin. The dimming mode is programmed by MODE register when this pin is left floating.
3	SYNC/FREQ	Boost Switching Frequency and External Frequency SYNC Pin. Connect a resistor from this pin to AGND to program the Boost switching frequency. Connect an external clock to synchronize the Boost switching frequency. Leave this pin floating if the switching frequency is programmed in I²C register.
4	EN	Device Enable Pin.
5	SCL/PSE	I²C Interface Clock Input Pin. When SCL/PSE and SDA/PSE are pulled to 0.75V to 1V, the PWM phase-shift function can be activated. Pull it to AGND to disable this multiplexing feature. When I²C is used, it is recommended to add a small capacitor (e.g. 47pF) capacitor from this pin to AGND.
6	SDA/PSE	I²C Interface Data Input Pin. When SDA/PSE and SCL/PSE are pulled to 0.75V to 1V, the PWM phase-shift function can be activated. Pull it to AGND to disable this multiplexing feature. When I²C is used, it is recommended to add a small capacitor (e.g. 47pF) capacitor from this pin to AGND.
7	COMP	Boost Converter Compensation Pin for Loop Response.
8	FAULT	Device Fault Indication Pin. Open-drain output, pulled to logic low if fault condition occurs.
9	ISET	LED Full-Scale Current Program Pin.
10	AGND	Analog Ground.
11, 12, 13, 14, 15, 16	LED6, LED5, LED4, LED3, LED2, LED1	LED Strings Cathode Connection with Internal Current Sink.
17	PGND	Power Ground.
18	SW	Drain Connection of Internal Boost Power FET.
19	OVP	Boost Over-Voltage Protection Threshold Adjustment Pin.
20	SHORT	LED Short Protection Threshold Program Pin. Connect a resistor from this pin to ground. Leave this pin floating if short threshold is programmed in I²C.
21	FSP	Switching Frequency Spread Spectrum Pin. Leave this pin floating if spread spectrum is programmed in I²C register.
22	VCC	Internal LDO Output Pin. Connecting a ceramic capacitor (1μF to 2.2μF) between VCC and AGND pin is required.
23	DIS	Gate Connection Pin for External Load Disconnect PMOS. Leave this pin floating if not used.
24	VIN	IC Power Supply Input Pin.
—	EP	Exposed Pad. LED sinks GND.

TYPICAL APPLICATION

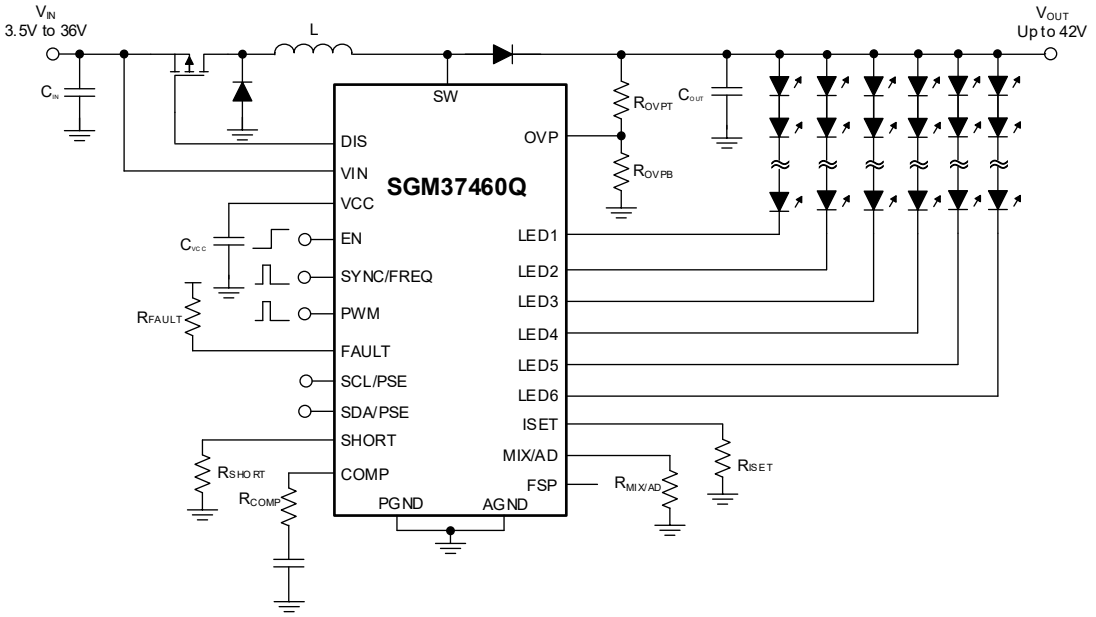


Figure 1. Typical Application

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, V_{EN} = 2V, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	V_{IN}		3.5		36	V
Quiescent Supply Current	I_Q	No switching		3.5		mA
Shutdown Supply Current	I_{SD}	V_{EN} = 0V, V_{IN} = 12V			1.5	μA
Input UVLO Threshold	V_{IN_UVLO}	Rising edge		3.1		V
Input UVLO Hysteresis				110		mV
LDO Output Voltage	V_{CC}	V_{EN} = 2V, 6V < V_{IN} < 24V, 0 < I_{VCC} < 10mA		5.1		V
EN On-Threshold	V_{EN_ON}	V_{EN} rising	1.2			V
EN Off-Threshold	V_{EN_OFF}	V_{EN} falling			0.4	V
EN Pull-Down Resistance	R_{EN}			1		MΩ
Boost Converter						
Low-side MOSFET On-Resistance	R_{DSON_LS}	V_{IN} = 12V		90		mΩ
SW Leakage Current	I_{SW_LK}	V_{SW} = 45V			1	μA
Switching Frequency	f_{SW}	R_{FREQ} = 10kΩ	1.98	2.2	2.42	MHz
		R_{FREQ} = 40kΩ	495	550	605	kHz
		FSW[1:0] bits = 01, SYNC/FREQ pin floating	340	400	460	kHz
FREQ Voltage	V_{FREQ}		0.57	0.6	0.63	V
FSP Pull-up Current	I_{FSP}			18		μA
Maximum Duty Cycle	D_{MAX}	f_{SW} = 1MHz	90			%
Cycle-by-Cycle Current Limit	I_{SW_LIM}	Initial accuracy	4.3	5		A
Current Limit Protection (1)	I_{LIM}	To trigger current limit protection	6.45	7.5		A
SYNC Input Low Threshold	V_{SYNC_L}	V_{SYNC} falling			0.4	V
SYNC Input High Threshold	V_{SYNC_H}	V_{SYNC} rising	1.2			V
PSE Active Threshold	V_{PSE}	Phase-shift enabled	0.75	0.9	1	V
COMP Trans-Conductance	G_{COMP}	ΔI_{COMP} ≤ 10μA		110		μA/V
COMP Source Current Limit	I_{COMP_SOR}			95		μA
COMP Sink Current Limit	I_{COMP_SIN}			95		μA
Current Dimming						
PWM Input Low Threshold	V_{PWM_L}	V_{PWM} falling			0.4	V
PWM Input High Threshold	V_{PWM_H}	V_{PWM} rising	1.2			V
MIX/AD Input Low Threshold	V_{MIX_L}	Mix dimming threshold			0.3	V
MIX/AD Input Middle Threshold	V_{MIX_MID}	PWM dimming threshold	0.5		0.8	V
MIX/AD Input High Threshold	V_{MIX_H}	Analog dimming threshold	1.0		1.3	V
MIX/AD Pull-up Current	I_{MIX}	MIX/AD pull-up current		18		μA
Mix Dimming Transfer Point		MIXTP bit = 0		25		%
Transfer Point Hysteresis				0.5		%
Mix Dimming Output Dimming Frequency	f_{MIX}	MIXFR bit = 0		200		Hz

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, V_{EN} = 2V, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LED Current Regulator						
LEDx Regulation Voltage	V_{HD}	I_{LED} = 20mA		410		mV
		I_{LED} = 100mA, T_J = +25℃		930	1050	
		I_{LED} = 100mA		930	1250	
Current Matching (2)		I_{LED} = 20mA, initial accuracy	-2.5		2.5	%
		I_{LED} = 100mA	-2.5		2.5	%
ISET Voltage	V_{ISET}			1.2		V
LEDx Current	I_{LED}	R_{ISET} = 24.9kΩ, T_J = +25℃	48.75	50	51.25	mA
		I_{LED} = 1/50 × 50mA = 1mA, T_J = +25℃	0.85	1.05	1.25	mA
Phase-Shift Degree		LED1 to 6 enabled		60		°
		LED1 to 4 enabled		90		°
Protection						
OVP Threshold	V_{OVP}		1.9	2	2.1	V
OVP Hysteresis				210		mV
OVP UVLO Threshold	V_{OVP_UV}	Boost converter fails		100		mV
LEDx Over-Voltage Threshold	V_{LEDx_OV}	TH_S[1:0] bits = 01		5		V
LEDx Over-Voltage Fault Timer				8.8		ms
LEDx UVLO Threshold	V_{LEDx_UV}			100		mV
Thermal Shutdown Threshold (1)	T_{SD}	Rising edge		160		℃
		Hysteresis		20		℃
DIS Pull-Down Current	I_{DIS}			60		μA
DIS Voltage (respective to V_{IN})	V_{DIS_IN}	V_{IN} = 12V, V_{IN} - V_{DIS}		6		V
SHORT Pull-up Current	I_{SHORT}	SHORT pull-up current		18		μA
I²C Interface						
Logic Low Input Voltage	V_{IL}				0.4	V
Logic High Input Voltage	V_{IH}		1.2			V
Logic Low Output Voltage	V_{OL}	I_{LOAD} = 3mA			0.4	V
SCL/PSE Clock Frequency	$f_{SCL/PSE}$				400	kHz

NOTES:
1. Specified by design and characterization, not production tested.
2. Matching refers to the difference of the maximum to minimum current divided by 2 times the average current.

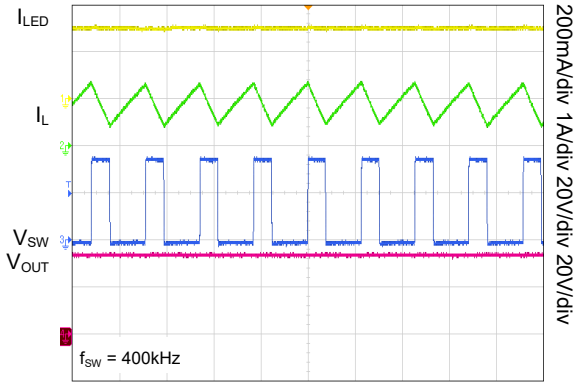
I²C TIMING REQUIREMENTS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL/PSE High Time	t_{HIGH}		0.6			μs
SCL/PSE Low Time	t_{LOW}		1.3			μs
Data Set-up Time	t_{SU_DAT}		100			ns
Data Hold Time	t_{HD_DAT}		0		0.9	μs
Set-up Time for Repeated Start	t_{SU_STA}		0.6			μs
Hold Time for Start	t_{HD_STA}		0.6			μs
Bus Free Time between Start and Stop Condition	t_{BUF}		1.3			ms
Set-up Time for Stop Condition	t_{SU_STO}		0.6			μs
Rise Time of SCL/PSE and SDA/PSE	t_R		20		300	ns
Fall Time of SCL/PSE and SDA/PSE	t_F		20		300	ns
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns
Capacitance Bus for Each Bus Line	C_B				400	pF

TYPICAL PERFORMANCE CHARACTERISTICS

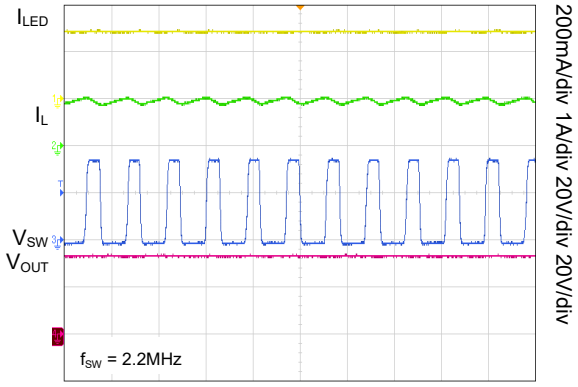
T_A = +25℃, V_{IN} = 12V, L = 22μH, f_{SW} = 400kHz, f_{PWM_IN} = 200Hz, C_{IN} = 4.7μF × 2, C_{OUT} = 4.7μF × 2, LED = 6P12S, I_{SET} = 50mA, unless otherwise noted.

Steady State



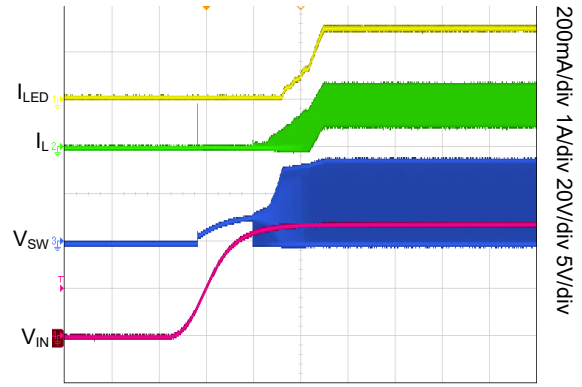
Time (2μs/div)

Steady State



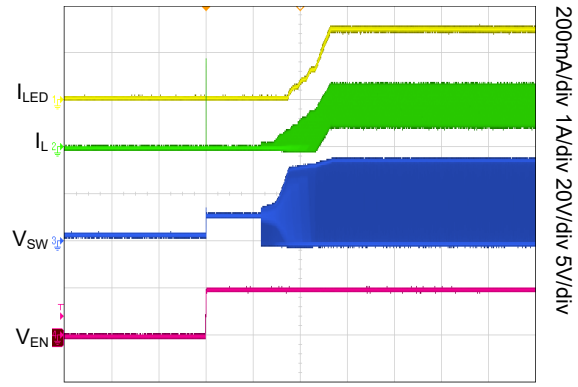
Time (500ns/div)

VIN Power On



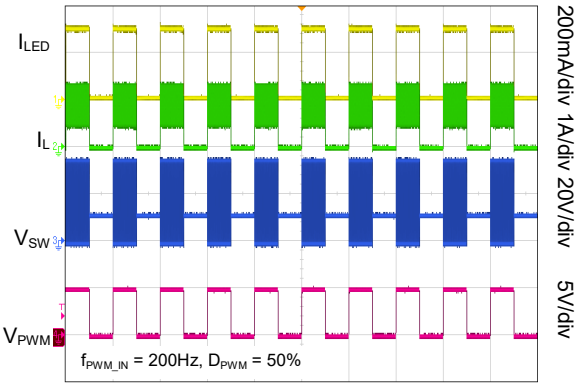
Time (10ms/div)

EN Power On



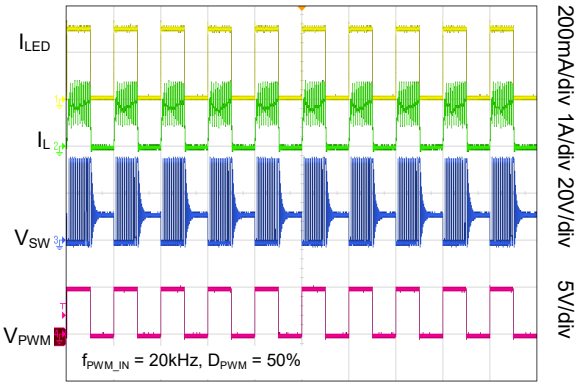
Time (10ms/div)

PWM Dimming



Time (5ms/div)

PWM Dimming

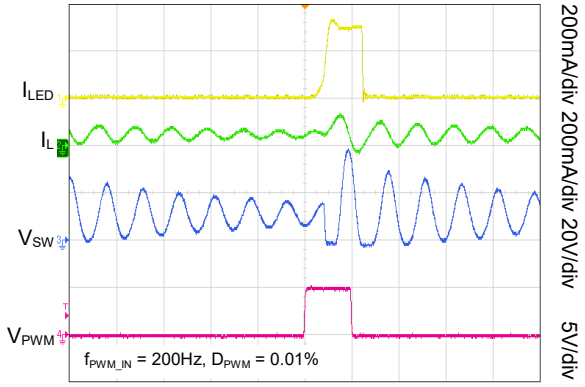


Time (50μs/div)

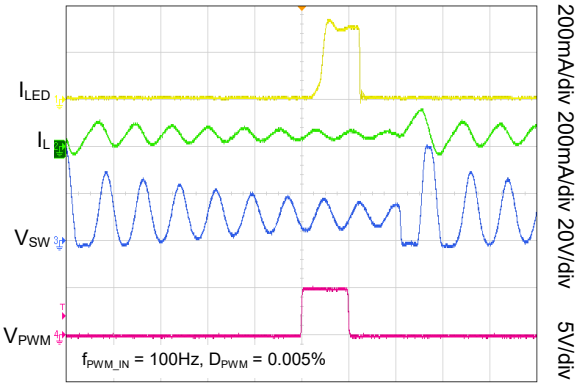
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, L = 22μH, f_{SW} = 400kHz, f_{PWM_IN} = 200Hz, C_{IN} = 4.7μF × 2, C_{OUT} = 4.7μF × 2, LED = 6P12S, I_{SET} = 50mA, unless otherwise noted.

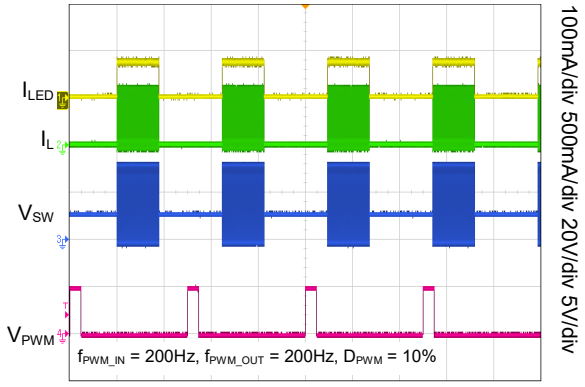
PWM Dimming



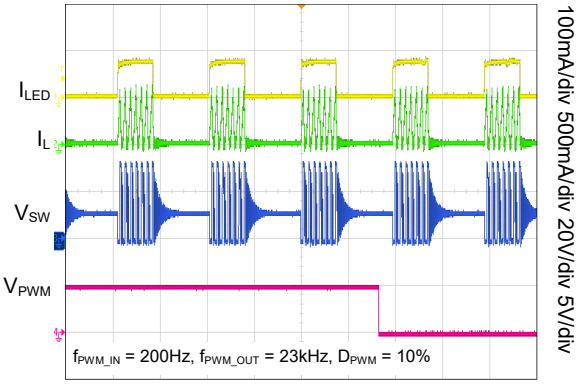
PWM Dimming



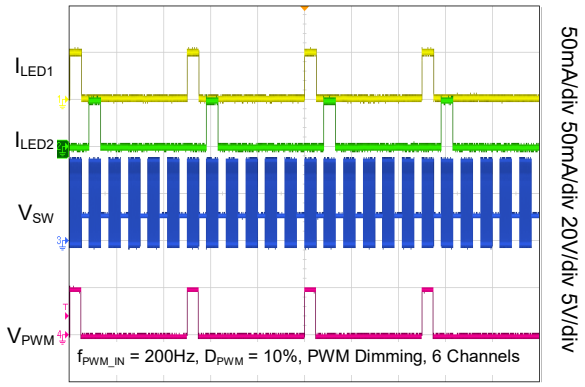
Mix Dimming



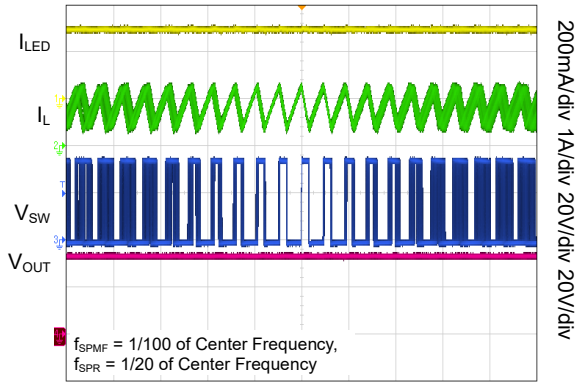
Mix Dimming



Phase-Shift Function



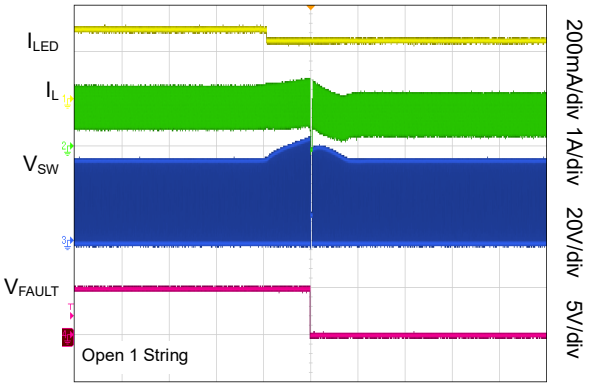
Frequency Spread Spectrum



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

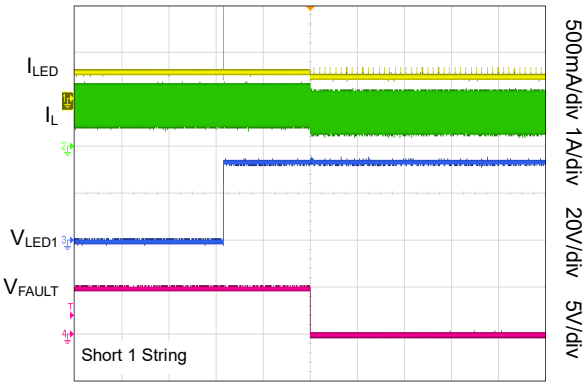
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LED Open Protection



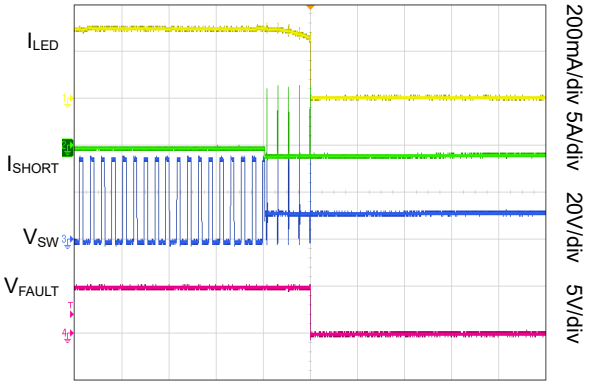
Time (1ms/div)

LED Short Protection



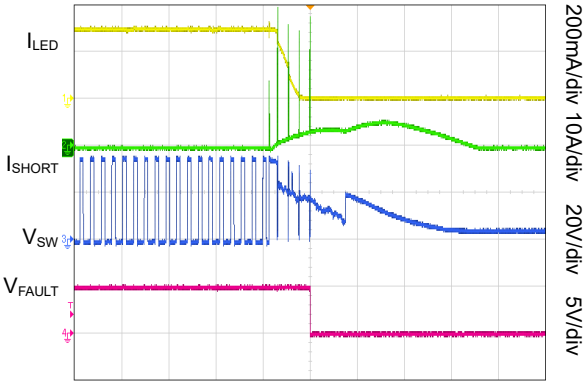
Time (5ms/div)

Short Inductor Protection



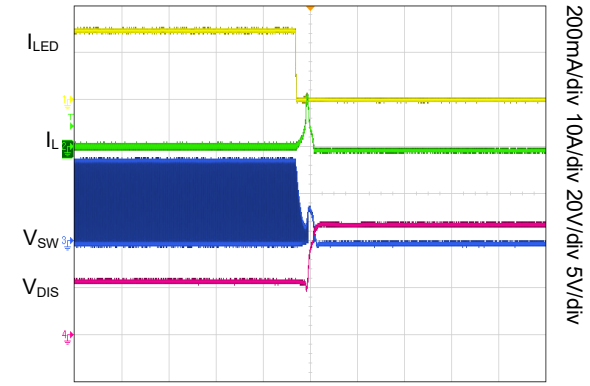
Time (10μs/div)

Short Diode Protection



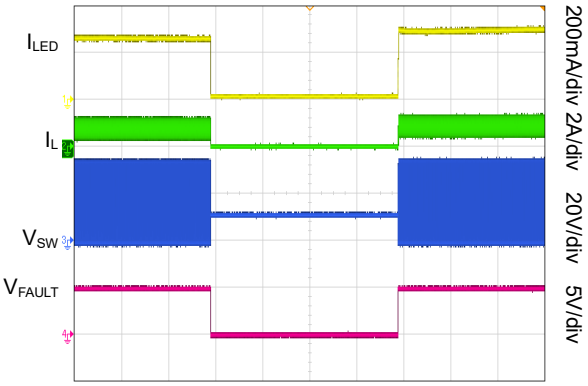
Time (10μs/div)

Short VOUT-to-GND Protection



Time (200μs/div)

Thermal Protection



Time (1s/div)

FUNCTIONAL BLOCK DIAGRAM

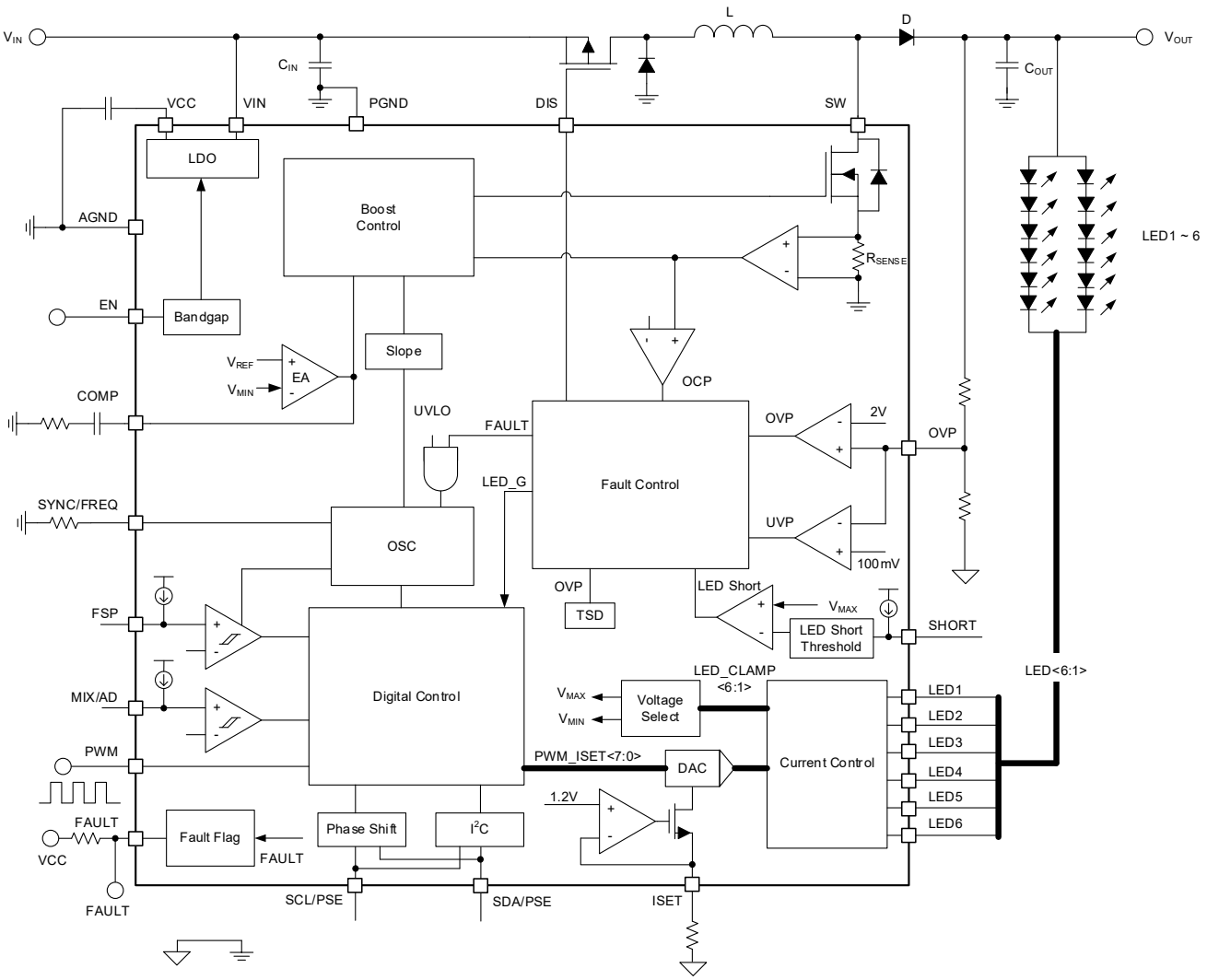


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM37460Q is a programmable Boost converter that operates at a constant frequency using peak current mode control. It supports up to 6 regulated current channels to drive white LED arrays.

The SGM37460Q provides flexible brightness control via PWM input (100Hz to 20kHz). The 6 LED strings can drive up to 150mA per channel through an external resistor at ISET pin. Dimming modes (mix, PWM, analog) are selectable through the MIX/AD pin or internal register. The switching frequency is programmable through I^2C or an external resistor at FREQ/SYNC pin. It can also be clocked by the external clock signal on the FREQ/SYNC pin.

V_{CC} 5V Internal Regulator

The SGM37460Q integrates an internal linear voltage regulator (V_{CC}) that provides a stable 5V supply to power the MOSFET gate driver and control circuits whenever the input voltage (V_{IN}) exceeds 6V. A ceramic capacitor ranging from 1μF to 2.2μF is required to connect between VCC and AGND pin for stability. If the chip shuts down, the V_{CC} drops to 0V, and the IC remains disabled until V_{CC} exceeds the under-voltage lockout (UVLO) threshold.

Boost Controller

The SGM37460Q utilizes peak current mode control to regulate output power. The internal clock turns on the N-MOSFET at the beginning of every switching cycle. Under normal conditions, the minimum turn-on time is approximately 100ns. To prevent sub-harmonic oscillations when the duty cycle exceeds 50%, a stabilizing ramp is applied to the output of the current sense amplifier. This processed signal is then sent to the PWM comparator, and once the summed voltage matches the error amplifier's output, the MOSFET turns off.

Error amplifier output reflects the difference between the reference voltage and the feedback voltage. The system dynamically adjusts the output voltage based on the lowest active LEDx voltage, which selected as the feedback voltage. If the feedback voltage falls below the reference voltage, the error amplifier responds by increasing its output, causing more current to pass through the MOSFET, which in turn delivers additional power to the output. If the feedback voltage is higher than the reference voltage, the error amplifier responds by decreasing its output, causing less current to pass through the MOSFET.

In light load condition, especially when $V_{OUT} \approx V_{IN}$, the device operates in pulse skipping mode. The MOSFET turns on with minimum on-time, followed by long time output energy discharge. The MOSFET remains off until the output voltage requires further boosting.

Switching Frequency Configuration

The switching frequency can be adjusted by using a resistor, I^2C interface, or sending external clock to SYNC/FREQ pin.

When setting the switching frequency with a resistor at SYNC/FREQ pin, it follows the equation:

$$f_{SW}(kHz) = \frac{22000}{R_{OSC}(k\Omega)} \quad (1)$$

If the switching frequency is configured through I^2C by FSW[1:0] bits in **REG0x01** register, the available settings are:
00 = 200kHz,
01 = 400kHz,
10 = 1MHz,
11 = 2.2MHz.

For external synchronization, an external clock should be sent to the SYNC/FREQ pin. Then the switching frequency can be clocked by this signal. If the signal disappears later, the Boost continues operation at the frequency defined by FSW[1:0] bits.

LED Current Configuration

The LED current amplitude is set using an external resistor connected between ISET and GND. The current amplitude follows the equation:

$$I_{LED}(mA) = \frac{1245}{R_{ISET}(k\Omega)} \quad (2)$$

System Start-up

When enabled, the SGM37460Q verifies the circuit configuration. If an external PMOS switch is utilized for input disconnection, the IC draws current from the DIS pin to enable the PMOS. After a 500μs delay, the system checks the over-voltage protection (OVP) circuit to determine if the output is shorted to ground. If OVP falls below the 100mV threshold, the IC is disabled and latched. Following this, the SGM37460Q continues conducting safety diagnostics, including detecting open LED strings and verifying over-voltage conditions. If no faults are detected, the Boost converter starts and the soft-start phase begins. Once the Boost output voltage and LED current are established and within the normal operating range, the IC enters the normal operation phase.

DETAILED DESCRIPTION (continued)

For optimal start-up performance, the recommended power-up sequence is as follows: Apply V_{IN} → Enable EN → Configure via I²C (if required) → Send PWM dimming signal.

Dimming Control Modes

The SGM37460Q supports three different dimming methods: analog dimming, PWM dimming and mix dimming. The dimming mode can be configured via I²C or by connecting a specific resistor to the MIX/AD pin. The voltage at the MIX/AD pin is determined by the following formula:

$$V_{MIX/AD}(mV) = 18(\mu A) \times R_{MIX/AD}(k\Omega) \quad (3)$$

where, $V_{MIX/AD}$ is the voltage at the MIX/AD pin and $R_{MIX/AD}$ is the value of the resistor connected between the MIX/AD pin and GND.

Mix Dimming Mode

The SGM37460Q offers two options for the mix dimming mode, with transfer points set at 25% or 12.5%, it can be set through its internal register.

- Option 1: Connect a resistor to the MIX/AD pin to set its voltage below 0.3V for mix dimming.
- Option 2: Leave MIX/AD pin floating and configure the internal MODE[1:0] bits in **REG0x00** to 00 via I²C.

When operating in mix dimming mode with a PWM signal applied to the PWM pin, the system behaves as follows:

- Above 25% PWM duty cycle, analog dimming is adopted, with the LED current amplitude directly proportional to the PWM duty.
- Below 25% PWM duty cycle, the system utilizes PWM dimming, fixing the LED current at 25% of its maximum. The output dimming duty is then 4 times the input PWM duty.

The output dimming frequency, selectable between 200Hz (default) and 23kHz (for reduced audible noise, but with an increased minimum dimming duty), is independently controlled via the I²C frequency register, and is not tied to the input PWM frequency. This function minimizes audible noise and optimizes dimming performance at low brightness levels.

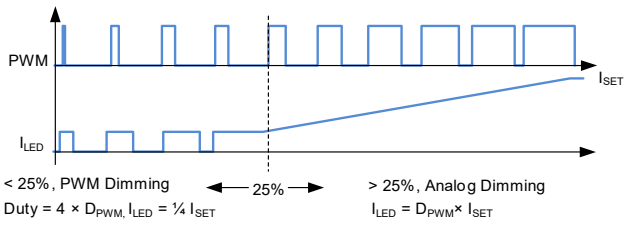


Figure 3. Mix Dimming with 25% Transfer Point

PWM Dimming Mode

PWM dimming is enabled by setting the MIX/AD pin voltage within the range of 0.5V to 0.8V using an external resistor, or by floating it and configuring the MODE[1:0] bits in **REG0x00** to 01 through I²C. In this mode, the LED current is directly chopped by the input PWM signal applied to the PWM pin, with the LED current frequency and duty mirroring that of the input PWM signal, while maintaining full-scale current.

Analog Dimming Mode

Analog dimming is enabled by setting the MIX/AD pin voltage within the range of 1V to 1.3V using an external resistor, or by floating it and configuring the MODE[1:0] bits in **REG0x00** to 10 through I²C. The input PWM signal is internally processed with an internal counter and its duty can be calculated. The LED current amplitude is determined by the following formula:

$$I_{LED} = I_{SET} \times D_{PWM} \quad (4)$$

where, I_{SET} represents the maximum LED current, and D_{PWM} is the duty cycle of the input PWM signal.

For optimal analog dimming performance, a PWM signal in the range of 100Hz to 20kHz is recommended. When the dimming duty cycle falls below 10%, the minimum LEDx voltage automatically shifts to 2V to maintain stability. Analog dimming provides a 255:1 dimming ratio, allowing for precise brightness adjustments.

Configuring Unused LED Channels

The SGM37460Q can automatically detect and disable unused LED channels during start-up if their LEDx pins are connected to GND. For instance, when using five LED strings, LED6 should be grounded. For four strings, both LED5 and LED6 should be tied to GND, and so forth.

Alternatively, unused LED channels can be disabled via the CH[2:0] bits in **REG0x01** register.

DETAILED DESCRIPTION (continued)

Phase-Shift Function

The SGM37460Q provides a phase-shift function to minimize inrush current and reduce audible noise during PWM dimming.

There are two ways to enable the phase-shift function:

Connect SCL/PSE and SDA/PSE pins together and adjust their voltage between 0.75V and 1V.

Enable the PSE bit in the internal register through I²C.

When PWM dimming is used and the phase-shift function is adopted, the current sources of the LED channels are automatically phase-shifted. The phase-shift angle is determined by the number of active LED channels as described in equation (5).

$$\text{Phase}\,(^\circ) = \frac{360}{n}(^\circ) \quad (5)$$

where n is the number of active LED channels. When all 6 channels are enabled, each channel is phase-shifted by 60°. When 5 channels are enabled, each channel is phase-shifted by 72°, and so on.

During phase-shift operation, LED channels should be disabled sequentially from the highest number downward. For instance, if only three LED strings are used, channels 6, 5, and 4 should be turned off. And if only four LED strings are used, channels 6 and 5 should be turned off.

When phase-shift function is used, it is not recommended to use two channels to drive a single LED string.

Frequency Spread Spectrum

The SGM37460Q employs switching frequency jitter to distribute the frequency spectrum, reducing spectrum spikes at the switching frequency and its harmonics frequency.

The dithering range can be configured by connecting a resistor at FSP pin. In this way, the modulation frequency remains fixed at 1/150 of the switching frequency. The voltage at the FSP pin is determined by the following formula:

$$V_{FSP}(mV) = 18(\mu A) \times R_{FSP}(k\Omega) \quad (6)$$

where, V_{FSP} is the voltage at the FSP pin and R_{FSP} is the value of the resistor connected between the FSP pin and GND.

If V_{FSP} < 0.3V, the jitter frequency is 1/20 of the switching frequency. If V_{FSP} is between 0.4V and 1.4V, the jitter frequency is 1/32 of the switching frequency.

The frequency spread spectrum function can also be set through I²C while floating the FSP pin.

The FSPR bit in **REG0x00** register determines the jitter range. The modulation frequency is set by FSPMF[1:0] bits in **REG0x00** register.

Deep Dimming Ratio for PWM Dimming

If the output dimming on-time falls below 8.7μs, the system automatically adjusts the output voltage to 93% of the over-voltage protection (OVP) threshold, ensuring stable performance at ultra-low brightness levels (see Figure 4).

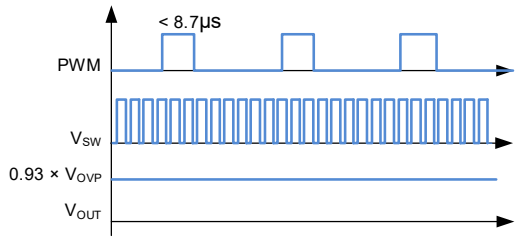


Figure 4. Deep Dimming Ratio for PWM Dimming

Protections

The SGM37460Q integrates multiple protection features, including LED open detection, LED short protection, short LEDx-to-GND protection, short VOUT-to-GND protection, over-current protection, and thermal shutdown protection.

When a fault is detected, the FAULT pin is pulled low (GND), and the corresponding FAULT bit is set to 1. Once the IC recovers, FAULT returns to high after a 750μs delay.

LED Open Protection

The IC detects open strings by monitoring the OVP and LEDx voltage levels. If a LED string fails and its LEDx voltage drops to ground, the SGM37460Q continues charging the output voltage until the OVP threshold is reached.

Then if OVP is triggered, the IC stops switching and isolates the faulty LED string, identified by a LEDx voltage lower than 100mV. The remaining active LED strings adjust the output voltage to a stable level. The output voltage is determined by the lowest LEDx voltage among all the active LED strings.

DETAILED DESCRIPTION (continued)

The isolated LED string periodically applies a 10μs pulse current every 500μs to determine if the LED open fault has been resolved, which allows for automatic recovery of the affected string. Under high-current conditions, if the LED open fault persists, repeated toggling of the FAULT pin may be observed.

LED Short Protection

The SGM37460Q continuously monitors LEDx voltages to detect LED short faults. When a string is shorted, its LEDx pin experiences high voltage stress. If the LEDx voltage exceeds the short protection threshold and this condition persists for 8.8ms at the period of V_{PWM} = high, the affected string is disabled until the short is resolved.

The LED short protection threshold can be configured in two ways:

The first way is to employ an external resistor from SHORT pin to GND. The SHORT pin provides a current source of 18μA (TYP), and the short string threshold is set to 10 times the voltage at SHORT pin, calculated as follow:

$$V_{SHORT}(mV) = 18(\mu A) \times R_{SHORT}(k\Omega) \quad (7)$$

where, V_{SHORT} is the voltage at the SHORT pin and R_{SHORT} is the value of the resistor connected between the SHORT pin and GND.

The second way is through the internal TH_S[1:0] bits in **REG0x01** register when the SHORT pin is floating.

If the LEDx voltage stays above the threshold for 480ms at the period of V_{PWM} = 100%, all strings are disabled, and the IC enters standby mode until the short condition clears. This function can be enabled or disabled through SEN bit in **REG0x02** register.

The disabled string applies a 10μs test pulse every 500μs to check if the fault has been resolved ensuring recoverable short string protection.

Short LEDx-to-GND Protection

If LEDx shorts directly to GND, the COMP voltage rises and saturates. If this saturation state persists for 20ms or 40ms (adjustable through the TCOMP bit), the short LEDx-to-GND protection activates.

If the short LEDx-to-GND protection is triggered, FAULT pulls low, indicating a fault. And DIS pulls high, turning off the external P-MOSFET to disconnect the faulty LED string. Then the IC latches off.

Short VOUT-to-GND Protection

During normal operation phase, the output voltage drops, if VOUT is shorted to ground. When the OVP pin voltage reaches the under-voltage lockout (UVLO) threshold for 10μs, the protection activates. Then DIS pulls high. This turns off the external P-MOSFET, so that VOUT is disconnected from VIN. The IC latches off.

Cycle-by-Cycle Current Limit Protection

To protect external components from excessive current stress, the SGM37460Q provides cycle-by-cycle current limit. If the current surpasses the limit, IC stops the switching until the next switching cycle.

Latch-Off Current Limit Protection

Under extreme fault conditions, such as short the inductor or short the diode, the SGM37460Q activates a latch-off protection by detecting the MOSFET current. If the MOSFET current exceeds 7.5A for 5 switching cycles, the IC latches off.

Over-Temperature LED Current Reduction

When the die temperature surpasses +140℃, the SGM37460Q automatically reduces the maximum LED current (see Figure 5), helping to prevent further temperature rise and enhance system reliability.

This feature is controlled by the over-temperature current decrement bit (OTID) in **REG0x00** register:

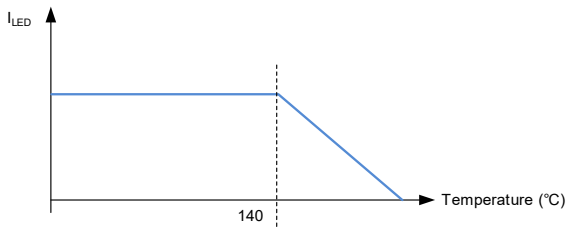


Figure 5. I_{LED} Decrease with Temperature

Thermal Shutdown

If the die temperature exceeds the thermal shutdown threshold, the IC shuts down. Once the temperature drops below the recovery threshold, normal operation resumes. The hysteresis for this process is typically 20℃, providing stable thermal management.

DETAILED DESCRIPTION (continued)

I²C Serial Interface and Data Communication

Standard I²C interface is used to program SGMXXXX parameters and get status reports. I²C is the well-known 2-wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The device that initiates a data transfer is a master. A master generates the SCL signal. Slave devices have unique addresses to identify. A master is typically a micro controller or a digital signal processor.

The SGM37460Q operates as a slave device that address is 0x38 (38H). It has three 8-bit registers, numbered from REG0x00 to REG0x02. A register read beyond REG02 (0x02) returns 0xFF.

Physical Layer

The standard I²C interface of SGMXXXX supports standard mode and fast mode communication speeds. The frequency of stand mode is up to 100kbits/s, while the fast mode is up to 400kbits/s. Bus lines are pulled high by weak current source or pull-up resistors and in logic high state with no clocking when the bus is free. The SDA/PSE pin is open-drain.

I²C Data Communication

START and STOP Conditions

A transaction is started by taking control of the bus by master if the bus is free. The transaction is terminated by releasing the bus when the data transfer job is done as shown in Figure 6. All transactions begin by master which applies a START condition on the bus lines to take over the bus and exchange data. At the end, the master terminates the transaction by applying one (or more) STOP condition. START condition is defined when SCL is high and a high to low transition on the SDA is generated by master. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. START and STOP are always generated by a master. After a START and before a STOP, the bus is considered busy.

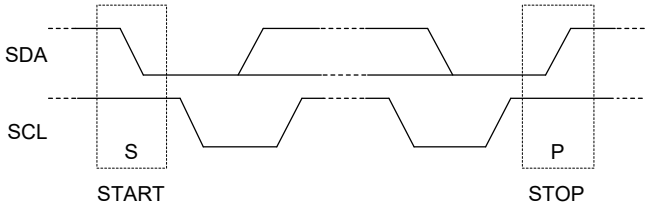


Figure 6. I²C Bus in START and STOP Conditions

Data Bit Transmission and Validity

The data bit (high or low) must remain stable during clock high period. The state of SDA can only change when SCL is low. For each data bit transmission, one clock pulse is generated by master. Bit transfer in I²C is shown in Figure 7.

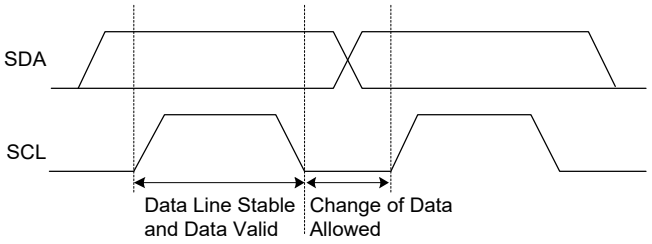


Figure 7. I²C Bus Bit Transfer

Byte Format

Data is transmitted in 8-bit packets (one byte at a time). The number of bytes in one transaction is not limited. In each packet, the 8 bits are sent successively with the Most Significant Bit (MSB) first. An acknowledge (or not-acknowledge) bit must come after the 8 data bits. This bit informs the transmitter whether the receiver is ready to proceed for the next byte or not. Figure 8 shows the byte transfer process with I²C interface.

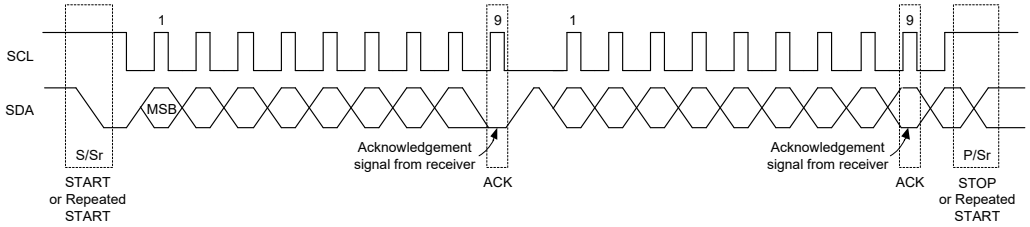


Figure 8. Byte Transfer Process

DETAILED DESCRIPTION (continued)

Acknowledge (ACK) and Not Acknowledge (NCK)

After transmission of each byte by transmitter, an acknowledge bit is replied by the receiver as the ninth bit. With the acknowledge bit, the receiver informs the transmitter that the byte is received, and another byte is expected or can be sent (ACK) or it is not expected (NCK = not ACK). Clock (SCL) is always generated by master, including the acknowledge clock pulse, no matter who is acting as transmitter or receiver. SDA line is released for receiver control during the acknowledge clock pulse. And the receiver can pull the SDA line low as ACK (reply a 0 bit) or let it be high as NCK during the SCL high pulse. After that, the master can either apply a STOP (P) condition to end the transaction or send a new START (S) condition to start a new transfer (called repeated start). For example, when master wants to read a register in slave, one start is needed to send the slave address and register address, and then, without a STOP condition, another start is sent by master to initiate the receiving transaction from slave. Master then sends the STOP condition and releases the bus.

Data Direction Bit and Addressing Slaves

The first byte sent by master after the START is always the target slave address (7 bits) and an eighth data-direction bit (R/$\overline{W}$). R/$\overline{W}$ bit is 0 for a WRITE transaction and 1 for READ (when master is asking for data). Data direction is the same for all next bytes of the transaction. To reverse it, a new START or repeated START condition must be sent by master (STOP will end the transaction). Usually the second byte is a WRITE sending the register address that is supposed to be accessed in the next byte(s). The data transfer transaction is shown in Figure 9.

WRITE: If the master wants to write in the register, the third byte can be written directly as shown in Figure 10 for a single write data transfer. After receiving the ACK, master may issue a STOP condition to end the transaction or send the next register data, which will be written to the next address in a slave as multi-write. A STOP is needed after sending the last data.

READ: If the master wants to read a single register (Figure 11), it sends a new START condition along with device address with R/$\overline{W}$ bit = 1. After ACK is received, master reads the SDA line to receive the content of the register. Master replies with NCK to inform slave that no more data is needed (single read) or it can send an ACK to request for sending the next register content (multi-read). This can continue until an NCK is sent by master. A STOP must be sent by master in any case to end the transaction.

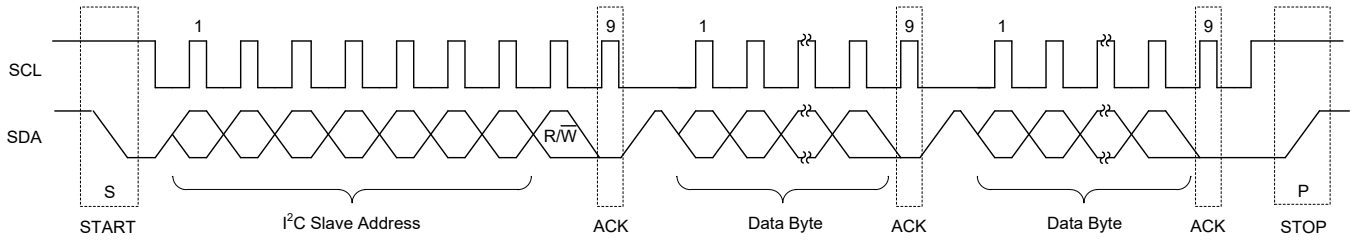


Figure 9. Data Transfer Transaction

DETAILED DESCRIPTION (continued)

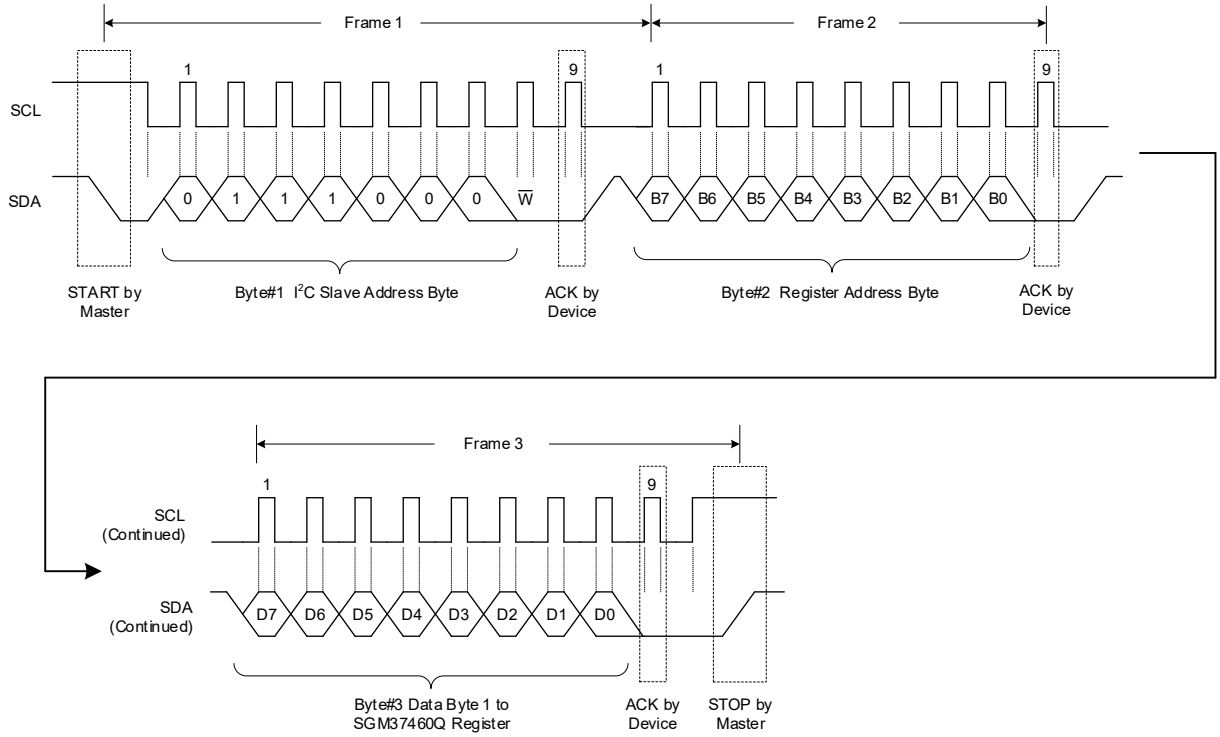


Figure 10. A Single Write Transaction

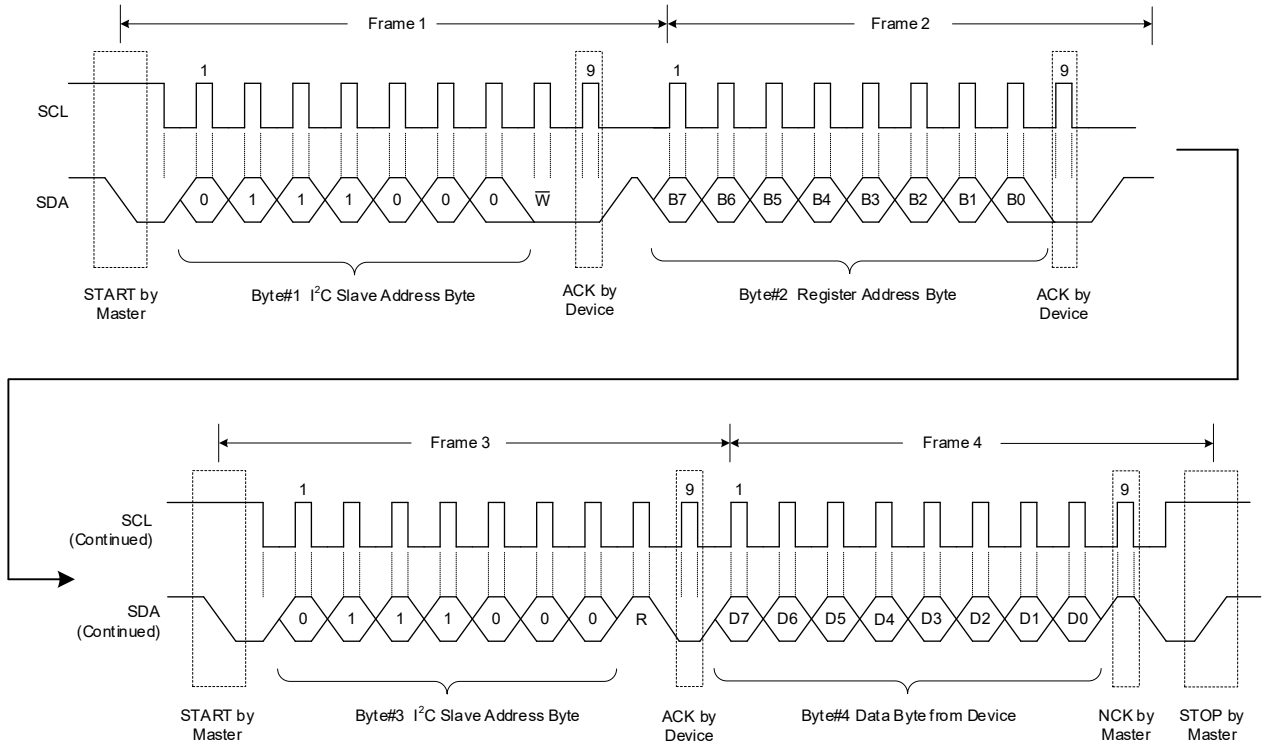


Figure 11. A Single Read Transaction

DETAILED DESCRIPTION (continued)

Data Transactions with Multi-Read or Multi-Write

Multi-read and multi-write are supported by SGM37460Q for REG0x00 through REG0x02 registers. In the multi-write, every new data byte sent by master is written to the next register of the device. A STOP is sent whenever master is done with writing into device registers.

In a multi-read transaction, after receiving the first register data (its address is already written to the slave), the master replies with an ACK to ask the slave to send the next register data. This can continue as much as it is needed by master. Master sends back an NCK after the last received byte and issues a STOP condition.

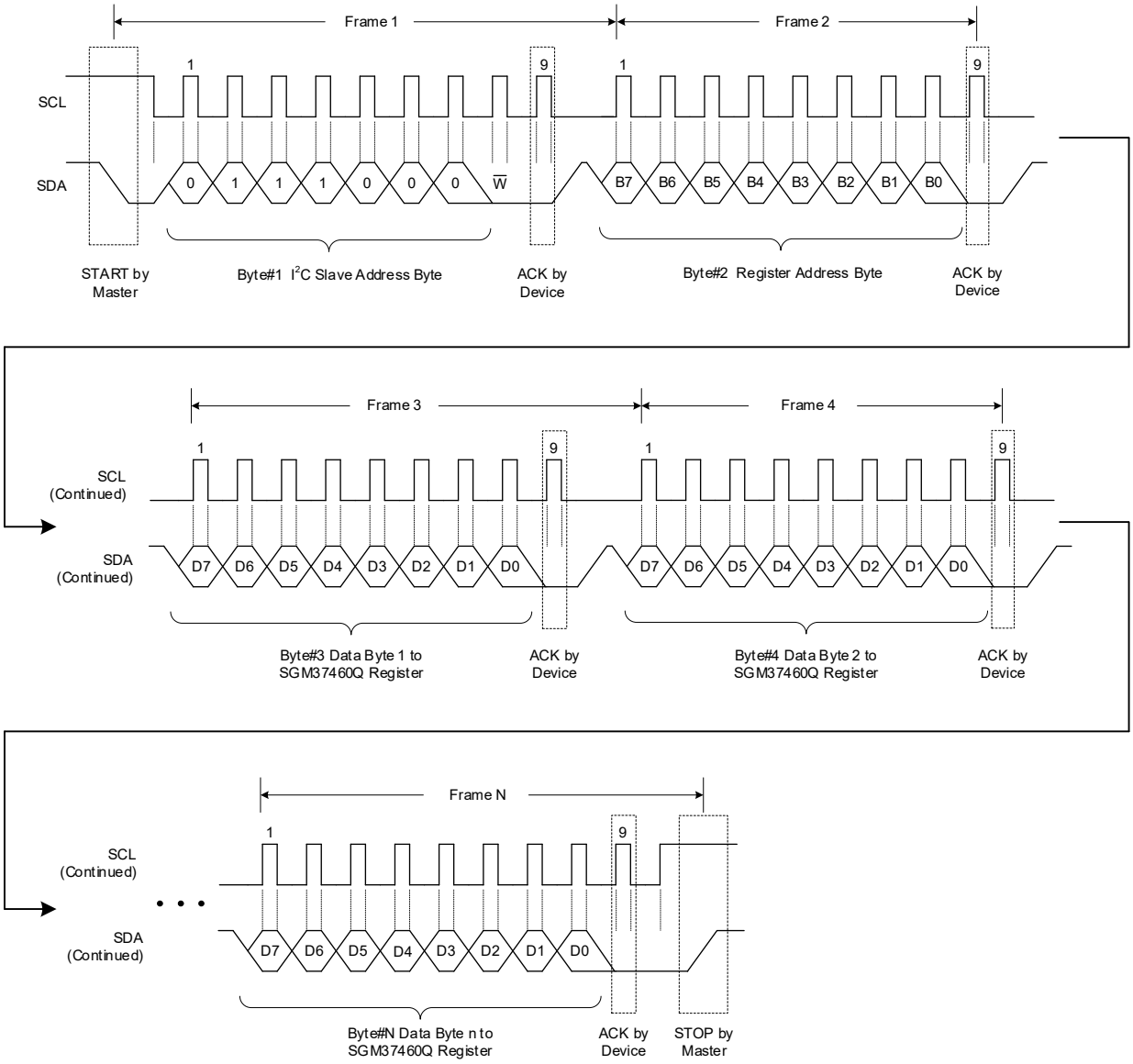


Figure 12. A Multi-Write Transaction

DETAILED DESCRIPTION (continued)

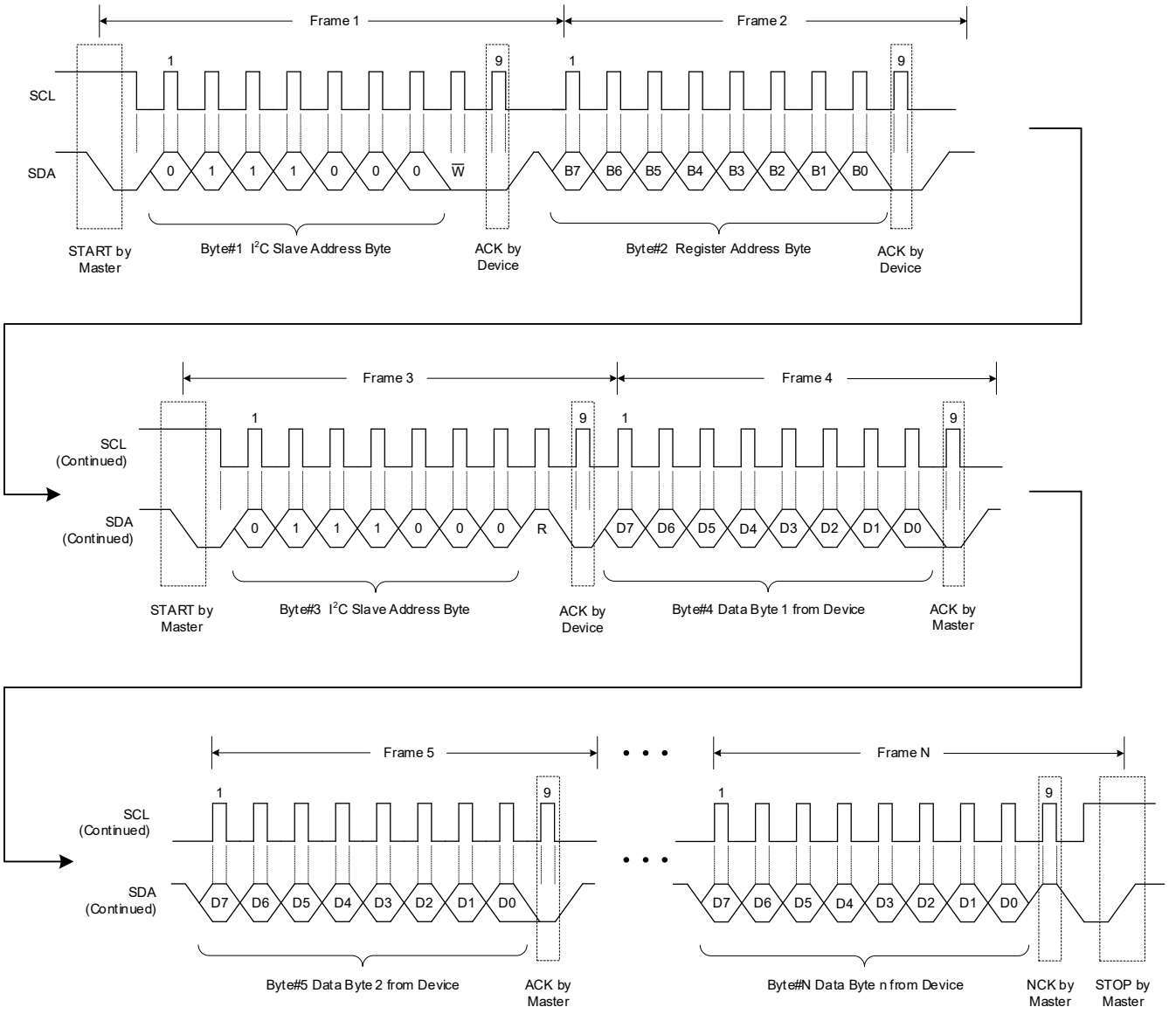


Figure 13. A Multi-Read Transaction

I²C PROGRAMMING

The SGM37460Q supports programming and status monitoring through a standard I²C interface. I²C is a well-known 2-wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named as serial data (SDA) and serial clock (SCL). Bus lines are pulled high by weak current source or pull-up resistors and in logic high state with no clocking when the bus is free. The SDA and SCL pins are open-drain.

SGM37460Q supports I²C timeout function which automatically detects and recovers from situations where the I²C bus is held in a busy state for an abnormal period of time. If the busy state lasts for 35ms, timeout function is triggered and internal I²C interface returns to the idle state.

REGISTER MAPS

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

I²C Slave Address of SGM37460Q: 0x38 (0b0111000 + R/W)

ADDRESS	REGISTER NAME	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x00	FUNC-SET 1	OTID	MODE[1:0]		MIXTP	MIXFR	FSPMF[1:0]		FSPR
0x01	FUNC-SET 2	PSE	TH_S[1:0]		FSW[1:0]		CH[2:0]		
0x02	FAULT	SEN	TCOMP	FT_LEDG	FT_OTP	FT_UVP	FT_OCP	FT_LEDS	FT_LEDO

Bit Types:
R: Read only
R/W: Read/Write

REG0x00: Function Set Register 1 [Reset = 0x86]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	OTID	1	R/W	Over-temperature LED current decrement function enable bit. 0 = Disabled 1 = Enabled (default)	N/A
D[6:5]	MODE[1:0]	00	R/W	Dimming mode selection bit. 00 = Mix dimming (default) 01 = PWM dimming 10 = Analog dimming 11 = Reserved Leave MIX/AD floating if this register is adopted.	N/A
D[4]	MIXTP	0	R/W	Mix dimming transfer point selection bit. 0 = 25% transfer point (default) 1 = 12.5% transfer point	N/A
D[3]	MIXFR	0	R/W	Mix dimming output frequency selection bit. 0 = 200Hz (default) 1 = 23kHz	N/A
D[2:1]	FSPMF[1:0]	11	R/W	Frequency spread spectrum modulation frequency selection bit. 00 = 1/100 of switching frequency 01 = 1/150 of switching frequency 10 = 1/200 of switching frequency 11 = Disable the frequency spread spectrum function (default) Leave FSP floating if this register is used.	N/A
D[0]	FSPR	0	R/W	Frequency spread spectrum jitter range selection bit. 0 = 1/20 of switching frequency (default) 1 = 1/32 of switching frequency Leave FSP floating if this register is used.	N/A

REGISTER MAPS (continued)

REG0x01: Function Set Register 2 [Reset = 0x28]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	PSE	0	R/W	Phase-shift enable bit. 0 = Phase-shift disabled (default) 1 = Phase-shift enabled	N/A
D[6:5]	TH_S[1:0]	01	R/W	LED Short protection threshold set bit. 00 = 2.5V 01 = 5V (default) 10 = 7.5V 11 = 10V Leave SHORT pin floating if this register is used.	N/A
D[4:3]	FSW[1:0]	01	R/W	Switching frequency set bit. 00 = 200kHz 01 = 400kHz (default) 10 = 1MHz 11 = 2.2MHz Leave FREQ floating if this register is used.	N/A
D[2:0]	CH[2:0]	000	R/W	Channel selection bit. 000 = All 6 channels active (default) 001 = LED1-5 enabled, LED6 disabled 010 = LED1-4 enabled, LED5-6 disabled 011 = LED1-3 enabled, LED4-6 disabled 100 = LED1-2 enabled, LED3-6 disabled 101 = Only LED1 enabled, LED2-6 disabled 110, 111 = Reserved	N/A

REG0x02: Fault Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	SEN	0	R/W	All LED short protection at D_{PWM} > 2%. 0 = Disable (default) 1 = Enable	N/A
D[6]	TCOMP	0	R/W	COMP-saturated time selection bit for short LEDx-to-GND. 0 = 20ms (default) 1 = 40ms	N/A
D[5]	FT_LEDG	0	R	LEDx short-to-GND protection fault indication bit. If fault, the fault bit remains 1 until read-back or power reset. 0 = No fault (default) 1 = Fault After this bit is read, the fault state can be latched until it is reset to 0.	N/A
D[4]	FT_OTP	0	R	Over-temperature protection fault indication bit. If fault, the fault bit remains 1 until read-back or power reset. 0 = No fault (default) 1 = Fault After this bit is read, the fault state can be latched until it is reset to 0.	N/A
D[3]	FT_UVP	0	R	Output under-voltage protection fault indication bit. If fault, the fault bit remains 1 until read-back or power reset. 0 = No fault (default) 1 = Fault After this bit is read, the fault state can be latched until it is reset to 0.	N/A
D[2]	FT_OCP	0	R	Over-current protection fault indication bit. If fault, the fault bit remains 1 until read-back or power reset. 0 = No fault (default) 1 = Fault After this bit is read, the fault state can be latched until it is reset to 0.	N/A
D[1]	FT_LEDS	0	R	LED strings short fault indication bit. If fault, the fault bit remains 1 until read-back or power reset. 0 = No fault (default) 1 = Fault After this bit is read, the fault state can be latched until it is reset to 0.	N/A
D[0]	FT_LEDO	0	R	LED strings open fault indication bit. If fault, the fault bit remains 1 until read-back or power reset. 0 = No fault (default) 1 = Fault After this bit is read, the fault state can be latched until it is reset to 0.	N/A

APPLICATION INFORMATION

Figure 14 shows the typical application circuit when I²C interface is used. It is recommended to add a small capacitor (e.g. 47pF) from SCL/PSE and SDA/PSE pins to AGND. The phase-shift function can be enabled through the PSE bit in **REG0x01**.

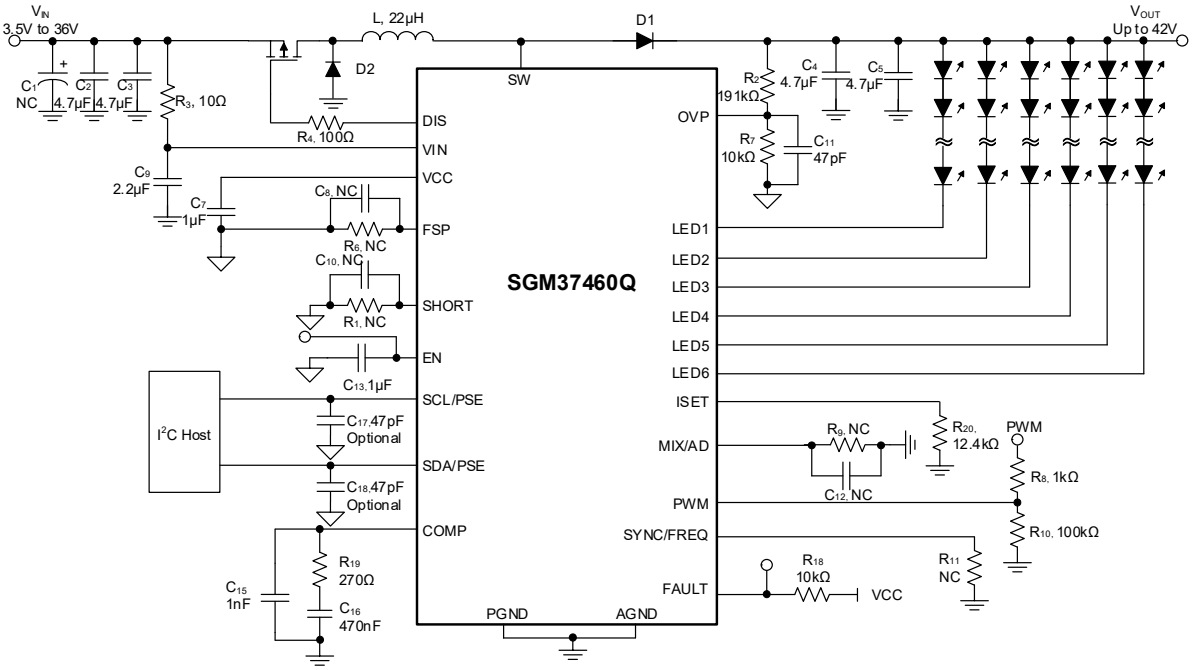


Figure 14. Typical Application Circuit with I²C Interface

Figure 15 shows the typical application circuit when phase-shift function is enabled through externally forcing voltage on SCL/PSE and SDA/PSE pins. Therefore, the I²C interface is automatically disabled.

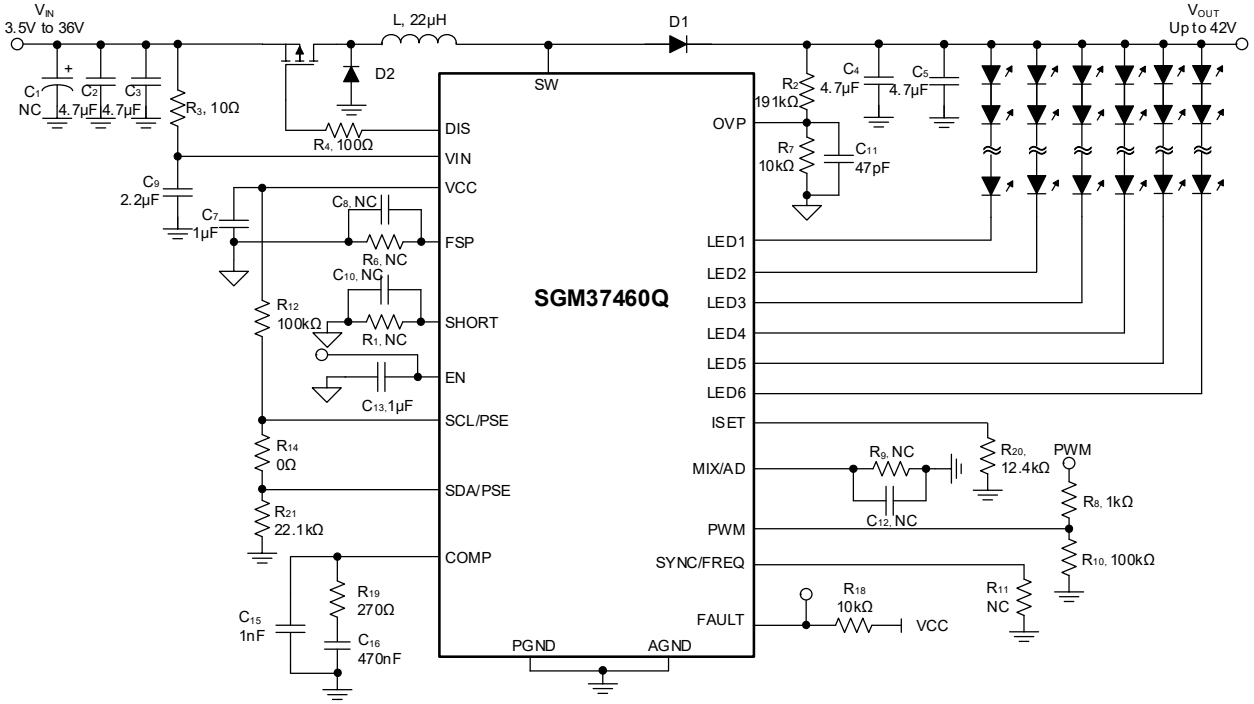


Figure 15. Typical Application Circuit with Phase-Shift Function Enabled Externally

APPLICATION INFORMATION (continued)

Figure 16 shows the typical application circuit when phase-shift function and I²C interface are disabled through connecting SCL/PSE and SDA/PSE pins to AGND.

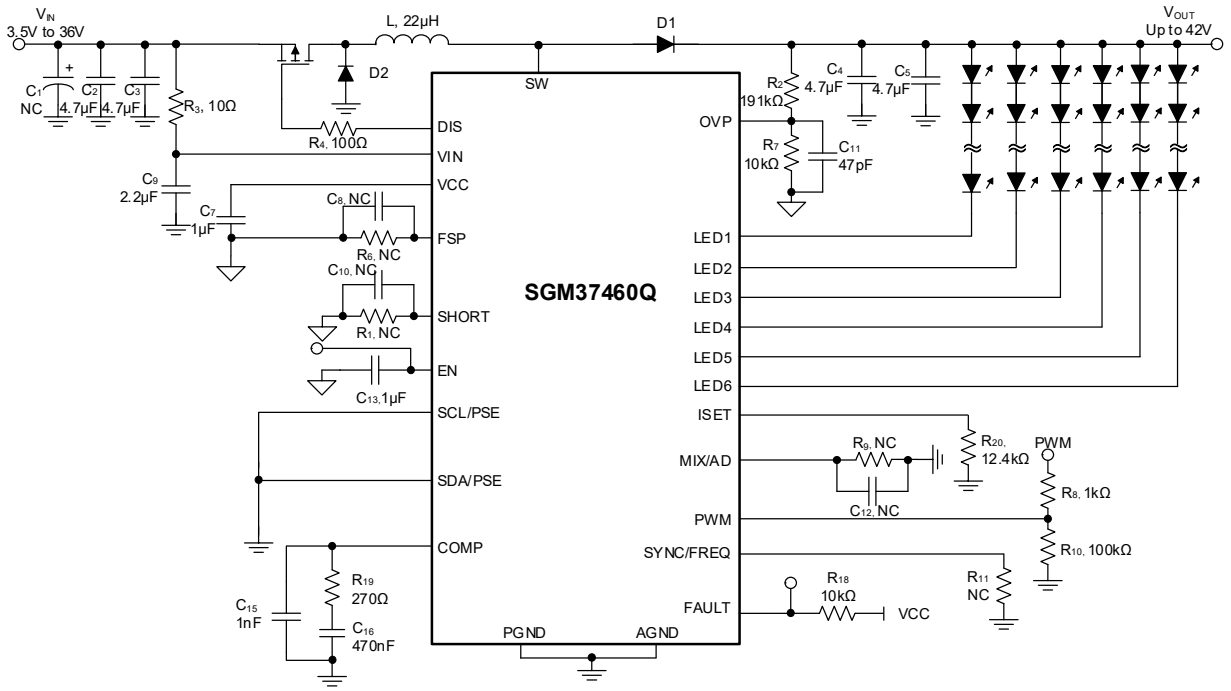


Figure 16. Typical Application Circuit without Phase-Shift Function and I²C Interface

Input Capacitor Selection

The input capacitor is a key component in the minimization of power supply surge currents and the reduction of switching noise. Input capacitance must ensure enough filtering for input power. For optimal performance, ceramic capacitors with X5R or X7R dielectrics are recommended due to their low ESR and stable temperature characteristics. In most cases, a 10μF ceramic capacitor is sufficient.

Output Capacitor Selection

The output capacitor voltage rating should be at least 50% higher than the maximum output voltage. Capacitance affects voltage ripple and Boost stability, but the DC bias effect can reduce actual capacitance by up to 80%. A target effective capacitance of 10μF is recommended for optimal phase and gain margin. X7R ceramic capacitors are recommended for their low ESR characteristics and good temperature performance.

Inductor Selection

The SGM37460Q requires an inductor to generate a higher output voltage from the input supply. Using a larger inductance value helps to reduce ripple current, lower peak inductor current but comes with downsides like bigger size and higher resistance. Ensure the inductor does not saturate under maximum load. The required inductance value can be determined using Equation 8 and Equation 9.

$$L \geq \frac{\eta \times V_{OUT} \times D \times (1-D)^2}{2 \times f_{SW} \times I_{LOAD}} \quad (8)$$

$$D = 1 - \frac{V_{IN}}{V_{OUT}} \quad (9)$$

where V_{IN} and V_{OUT} are the input and output voltages, f_{SW} is the switching frequency, I_{LOAD} represents the LED current, and η represents the overall system efficiency.

For optimum performance, select an inductor with a DC current rating at least 40% greater than the peak input current. It is recommended to use an inductor with low DCR to achieve good efficiency.

APPLICATION INFORMATION (continued)

Layout Guidelines

1. Place a small capacitor (e.g. 2.2μF) besides the VIN pin to prevent sudden VIN drops or negative spikes.
2. The external PMOS gate pins should be placed close to the IC's DIS pin to minimize the gate trace length and ensure that the gate drive is less susceptible to interference.
3. Place the inductor close to the SW node. Keep the connecting copper short and wide for minimal power loss and optimal EMI performance. Keep the SW node on a single copper layer. Do not use vias to route this node across multiple layers.
4. Keep the SW – power diode – output capacitors – GND path as short as possible to minimize the high-frequency current loop area and path length.
5. Place the external compensation capacitor and resistor as close as possible to the COMP pin.
6. Separate PGND (power ground) and AGND (analog ground) areas. Keep AGND isolated from high-current paths to minimize noise coupling.
7. Connect the PGND and AGND at a single point directly beneath the device, preferably at the thermal pad.
8. The thermal pad of the device must be properly soldered to the PCB for efficient heat dissipation. Use an adequate number of thermal vias beneath the pad to transfer heat to the backside ground plane and improve thermal performance.
9. Use an appropriate number and size of vias in each current path.

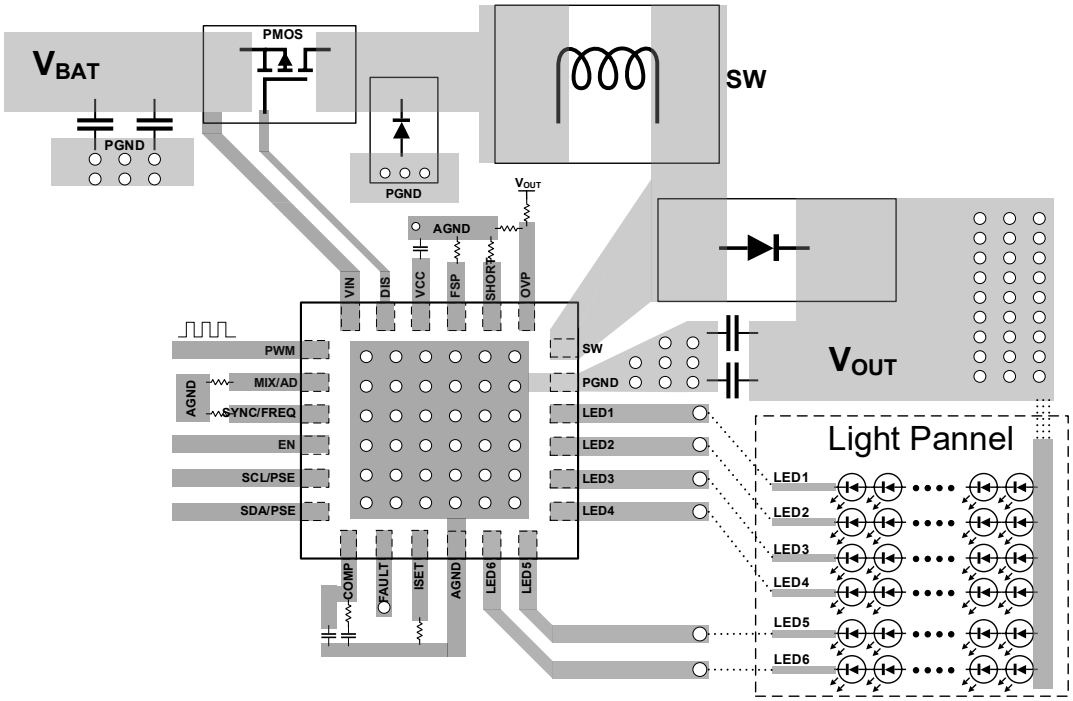


Figure 17. PCB Layout

REVISION HISTORY

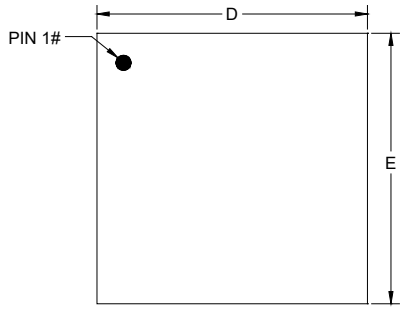
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

NOVEMBER 2025 – REV.A to REV.A.1	Page
Updated CDM value	2
Added Figure 15, 16 in Application Section	23, 24

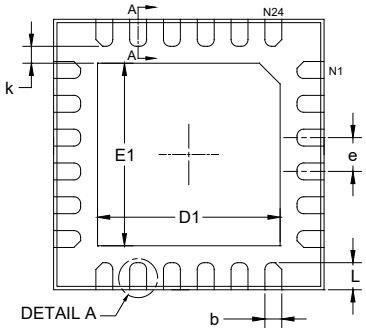
Changes from Original to REV.A (SEPTEMBER 2025)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

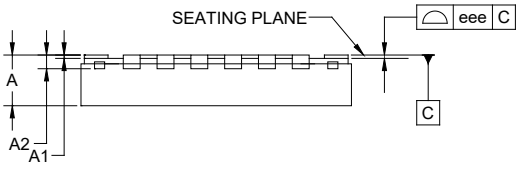
TQFN-4×4-24EL



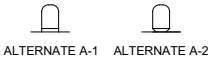
TOP VIEW



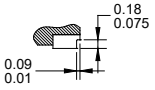
BOTTOM VIEW



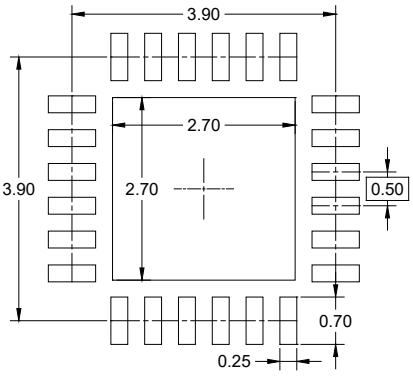
SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



SECTION A-A
TERMINAL CROSS SECTION



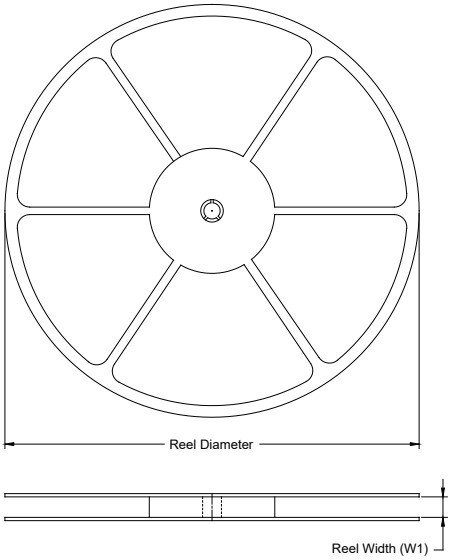
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2		0.203 REF	
b	0.200	-	0.300
D	3.900	-	4.100
D1	2.600	-	2.800
E	3.900	-	4.100
E1	2.600	-	2.800
e		0.500 BSC	
L	0.300	-	0.500
k		0.250 REF	
eee		0.080	

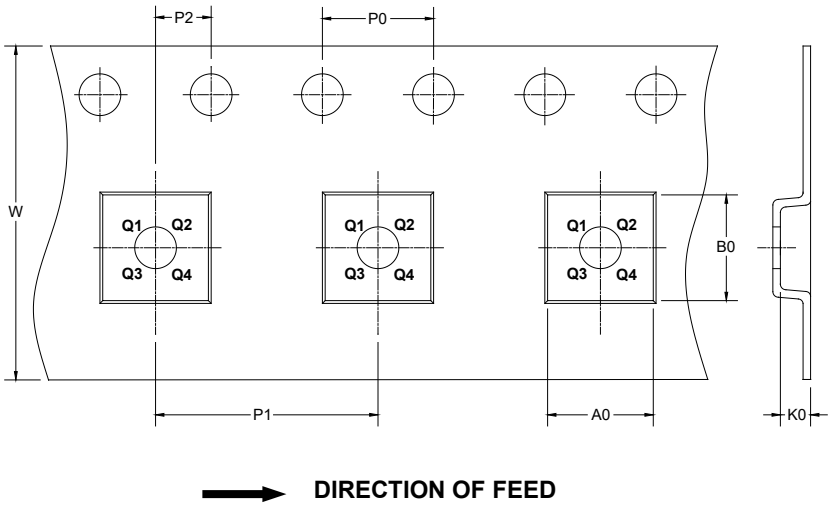
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



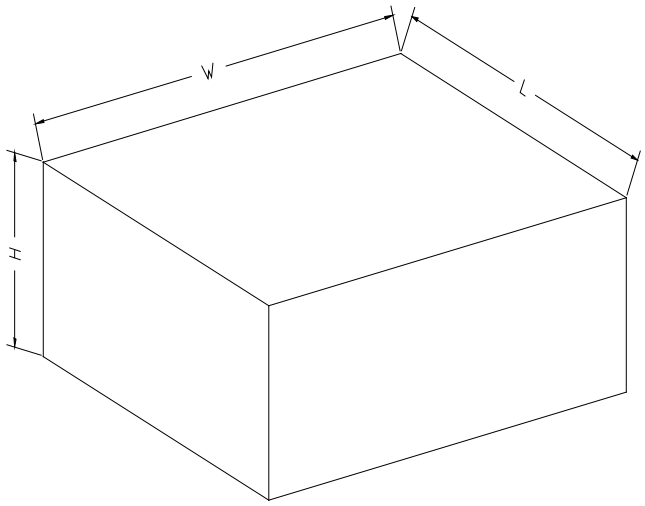
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-4×4-24EL	13"	12.4	4.30	4.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002