具有模拟和 PWM 调光功能的 TPS92630-Q1 三通道线性 LED 驱动器

1 特性

- 符合汽车类应用的 标准
- 具有符合 AEC-Q100 标准的下列结果：
  - 器件温度 1 级：–40°C 至 125°C 的环境运行温度范围
  - 器件 HBM ESD 分类等级 H2
  - 器件 CDM ESD 分类等级 C3B
- 3 通道 LED 驱动器（具有模拟和 PWM 调光功能）
- 宽输入电压范围：5V - 40V
- 由基准电阻器设定的可调恒定输出电流
  - 最大电流：每通道 150mA
  - 最大电流：并联运行模式下为 450mA
  - 精度：当 $I_{(IOUTx)}$ > 30mA 时，每通道 ±1.5%
  - 精度：当 $I_{(IOUTx)}$ > 30mA 时，每器件 ±2.5%
- 使用多个 IC 或者单个 IC 的多个通道的并联输出，以实现更高电流
- 低压降电压
  - 最大压降：电流为 60mA 时每通道 400mV
  - 最大压降：电流为 150mA 时每通道 0.9V
- 每个通道独立进行 PWM 调光
- 具有抗毛刺脉冲计时器的开路和短路 LED 检测
- 每条通道的 LED 灯串电压反馈，用于单个 LED 短路检测
- 针对单个 LED 短路故障的独立故障引脚
- 用于报告开路、短路和热关断故障的故障引脚，可通过一条总线并行连接最多 15 个器件
- 器件可适应慢输入电压 dV/dt（0.5V/分），而不会出现任何问题
- 运行结温范围：-40°C 至 150°C
- 封装：16 引脚耐热增强型 PWP 封装 (HTSSOP)

2 应用

汽车 LED 照明 应用，例如：

- 日间行车灯
- 驻车灯
- 雾灯
- 后灯
- 停车灯或尾灯
- 车内照明

3 说明

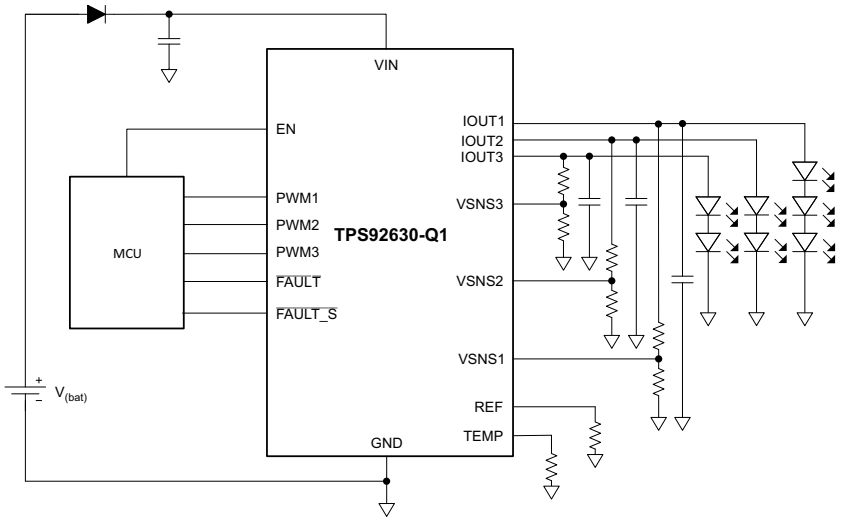
TPS92630-Q1 器件是一款具有模拟和 PWM 调光控制功能的三通道线性 LED 驱动器。该器件的全面诊断和内置保护功能使其成为可变强度 LED 照明（可达到中等功率范围） 应用 的理想之选。

器件信息(1)

器件号	封装（引脚）	封装尺寸（标称值）
TPS92630-Q1	HTSSOP (16)	4.40mm × 5.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

典型应用原理图



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4 修订历史记录

Changes from Revision D (January 2018) to Revision E **Page**

- 在典型应用原理图上增加了输出电容器 ... 1
- Changed V_{IH} and V_{IL} logic-level values for the PWMx pins ... 7
- Changed parameter description for $I_{(pullup)}$ from strong to weak pullup current ... 8
- Added capacitors to the outputs on Figure 26 ... 24
- Added the *Input and Output Capacitors* section ... 25
- Added capacitors to the outputs on Figure 28 ... 26
- Added the *Input and Output Capacitors* section ... 27
- Added capacitors to the outputs on Figure 29 ... 28
- Added the *Input and Output Capacitors* section ... 29
- Added capacitors to the outputs on Figure 30 ... 30
- Added the *Input and Output Capacitors* ... 31
- Added capacitors to the outputs on Figure 31 ... 31
- Added the *Input and Output Capacitors* section ... 32

Changes from Revision C (November 2017) to Revision D **Page**

- Changed pinout diagram ... 4
- Changed text for the *Thermal pad* row in the DESCRIPTON column ... 5

Changes from Revision B (January 2015) to Revision C **Page**

- 在产品说明书标题中将 TPS9263x-Q1 更改成了 TPS92630-Q1 ... 1
- 从页眉中删除了 TPS92630-Q1 部件号 ... 1
- 在*特性* 列表中删除了“两个选项”项目 ... 1
- 在*器件信息* 表中删除了 TPS92631-Q1 器件 ... 1
- Changed pinout diagram ... 4

- Deleted the COMMENT column and moved the comment text to the DESCRIPTION column 4
- Added a row for thermal pad information 5
- Deleted specifications pertaining to the TPS92631-Q1 device 8
- Changed figure reference in the $\overline{FAULT}$ *Diagnostics* section to Figure 19 15
- 添加了*接收文档更新通知* 和*社区资源* 部分 34

Changes from Revision A (December 2014) to Revision B **Page**

- Changed pin numbers for IOUT1 and IOUT3 in *Pin Functions* table 4

Changes from Original (February 2014) to Revision A **Page**

- Changed pin numbers and comments in *Pin Functions* table for pins 14 and 16 4
- Changed Changed the *Handling Ratings* table to *ESD Ratings* and moved storage temperature to the *Absolute Maximum Ratings* table 6
- Changed the MAX value for the EN internal pulldown parameter from 2.5 to 5 µA in the *Electrical Characteristics* table 7
- Added MAX value for $T_{(shutdown)}$ 8
- Changed Figure 24 22
- Changed Figure 25 22
- Changed voltage on pullup resistor from 3 V to 3.3 V 22
- Changed board layout diagram 33

5 说明（续）

这款器件的设计非常适合于在其功率能力范围内驱动被配置为单个灯串或多个灯串的 LED。单个器件能够驱动多达 3 个灯串（每个灯串中有 1 到 3 个 LED），每通道的总电流高达 150mA。为了提供达到 450mA 的更高电流驱动能力，可将输出并联。

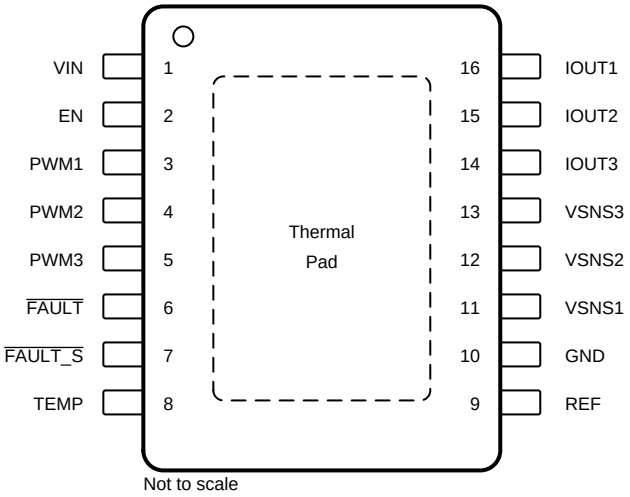
在多灯串 应用中，该器件的优势在于支持 LED 灯串进行共阴极连接。因此，此类应用仅需一条回线，无需像进行低侧电流感应的系统那样为每个 LED 灯串都配备一条回线。

单个 LED 短路比较器可检测出发生短路故障的单个 LED。故障输出能够支持多个器件之间的总线连接拓扑结构。

该器件包含温度监控器，可在器件结温超过温度阈值时降低 LED 驱动电流。用户可通过一个外部电阻器对温度阈值进行编程。将 TEMP 引脚接至地面可禁用热电流监视功能。该器件提供了将结温以模拟电压形式输出的出厂程序选项。

6 Pin Configuration and Functions

PWP Package
16-Pin HTSSOP With PowerPAD™ Package
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	2	I	Enable and shut down
$\overline{\text{FAULT}}$	6	I/O	Fault pin. Leave floating if not used.
$\overline{\text{FAULT_S}}$	7	I/O	Single-LED short fault. Leave floating if not used.
GND	10	—	Ground
IOUT1	16	O	Current output pin. Connect to VSNS1 if not used.
IOUT2	15	O	Current output pin. Connect to VSNS2 if not used.
IOUT3	14	O	Current output pin. Connect to VSNS3 if not used.
PWM1	3	I	PWM input and channel ON or OFF. Tie to GND if this channel is not used.
PWM2	4	I	PWM input and channel ON or OFF. Tie to GND if this channel is not used.
PWM3	5	I	PWM input and channel ON or OFF. Tie to GND if this channel is not used.
REF	9	O	Reference resistor pin for normal current setting
TEMP	8	I/O	Temperature foldback threshold program. Tie to GND if not used.
VIN	1	—	Input pin – VBAT supply
VSNS1	11	I	String voltage sense. Connect to IOUT1 if not used.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
VSNS2	12	I	String voltage sense. Connect to IOUT2 if not used.
VSNS3	13	I	String voltage sense. Connect to IOUT3 if not used.
Thermal pad	—	—	Connect to GND

7 Specifications

7.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
VIN, IOUTx, PWMx, EN, VSNSx	Unregulated input(2) (3) (4)	–0.3	45	V
$\overline{\text{FAULT}}$, $\overline{\text{FAULT_S}}$	See (2)	–0.3	22	V
Others	See (2)	–0.3	7	V
Virtual junction temperature, T_J		–40	150	°C
Operating ambient temperature, T_A		–40	125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Absolute maximum voltage 45 V for 200 ms
(4) V_{IOUTx} must be less than V_{VIN} + 0.3 V

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)		±2000	V
	Charged-device model (CDM), per AEC Q100-011	Corner pins (1, 8, 9, and 16)	±750	
		Other pins	±500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
VIN		5	40	V
PWMx, EN, VSNSx		0	40	V
$\overline{\text{FAULT}}$, $\overline{\text{FAULT_S}}$		0	20	V
Others		0	5	V
T_J	Operating junction temperature range	–40	150	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS92630-Q1 PWP (HTSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	41.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.4	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) The thermal data is based on JEDEC standard high-K profile – JESD 51-7. The copper pad is soldered to the thermal land pattern. Also, correct attachment procedure must be incorporated.

7.5 Electrical Characteristics

$V_{(VIN)}$ = 14 V, T_J = –40°C to 150°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT (VIN)						
V_I	Input voltage		5		40	V
$I_{(quiescent)}$	Quiescent current	All PWMx = high, $I_{(IOUTx)}$ = 100 mA, Not including I_{ref}	0.5	0.6	0.85	mA
$I_{O(sd)}$	Shutdown current	$V_{(EN)}$ = 0 V			10	µA
$I_{(fault)}$	Shutdown current in fault mode (device to GND)	PWM = EN = high, $\overline{FAULT}$ = low, $V_{(VIN)}$ = 5 V–40 V, I = 100 mA	0.5	0.6	0.85	mA
	Shutdown current in fault mode (from $V_{(VIN)}$)	PWM = EN = high, $\overline{FAULT}$ = low, $V_{(VIN)}$ = 5 V–40 V, I = 100 mA			2	
PWMx AND EN						
$V_{IL(EN)}$	Logic input, low level	IOUTx disabled	0		0.7	V
$V_{IH(EN)}$	Logic input, high level	IOUTx enabled	2			V
$I_{(EN-pd)}$	EN internal pulldown	$V_{(EN)}$ = 0 V to 40 V	0.35		5	µA
$V_{IL(PWMx)}$	Logic input, low level	IOUTx disabled	1.135	1.195	1.255	V
$V_{IH(PWMx)}$	Logic input, high level	IOUTx enabled	1.161	1.222	1.283	V
$V_{hys(PWM)}$	Hysteresis			44		mV
$I_{(PWM-pd)}$	PWMx internal pulldown current	$V_{(PWMx)}$ = 40 V	100	180	250	nA
CURRENT REGULATION (IOUTx)						
$I_{(IOUTx)}$	Regulated output current range	Each channel	10		150	mA
		Three channels in parallel mode	30		450	
$\Delta I_{O(channel)}$	Channel accuracy	10 mA < $I_{(IOUTx)}$ < 30 mA, $V_{(VIN)}$ = 5 V–40 V; Channel accuracy = $\frac{I_{(IOUTx)} - I_{(avg)}}{I_{(avg)}}$ (1)	–3%		3%	
		30 mA ≤ $I_{(IOUTx)}$ < 150 mA, Vin = 5 V–40 V; Channel accuracy = $\frac{I_{(IOUTx)} - I_{(avg)}}{I_{(avg)}}$ (1)	–1.5%		1.5%	
$\Delta I_{O(device)}$	Device accuracy	10 mA < $I_{(IOUTx)}$ < 30 mA, $V_{(VIN)}$ = 5 V to 20 V(2); Device accuracy = $\frac{I_{(IOUTx)} - I_{(setting)}}{I_{(setting)}}$ (3)	–4%		4%	
		30 mA ≤ I_{OUT} < 150 mA, $V_{(VIN)}$ = 5 V to 20 V(2); Device accuracy = $\frac{I_{(IOUTx)} - I_{(setting)}}{I_{(setting)}}$ (3)	–2.5%		2.5%	
V_{ref}	Reference voltage		1.198	1.222	1.246	V
$K_{(I)}$	Ratio of $I_{(IOUTx)}$ to reference current			100		
$V_{(DROP)}$	Dropout voltage	At 150 mA load per channel		0.6	0.9	V
		At 60 mA load per channel		0.24	0.4	
SR	Current rise and fall slew rates	Current rising from 10% to 90% or falling from 90% to 10% at $I_{(IOUTx)}$ = 60 mA.(4)	4	8	15	mA/µs
		Current rising from 10% to 90% or falling from 90% to 10% at $I_{(IOUTx)}$ = 150 mA.(4)	7	14	25	mA/µs

(1) $I_{(AVG)} = [I_{(IOUT1)} + I_{(IOUT2)} + I_{(IOUT3)}] / 3$
(2) For $V_{(VIN)}$ voltages higher than 20 V, see Figure 2 and Figure 3.
(3) $I_{(setting)}$ is the target current set by R_{ref}.
(4) See Figure 17 for the load model for the slew-rate test and delay-time test.

Electrical Characteristics (continued)

$V_{(VIN)}$ = 14 V, T_J = –40°C to 150°C (unless otherwise stated)

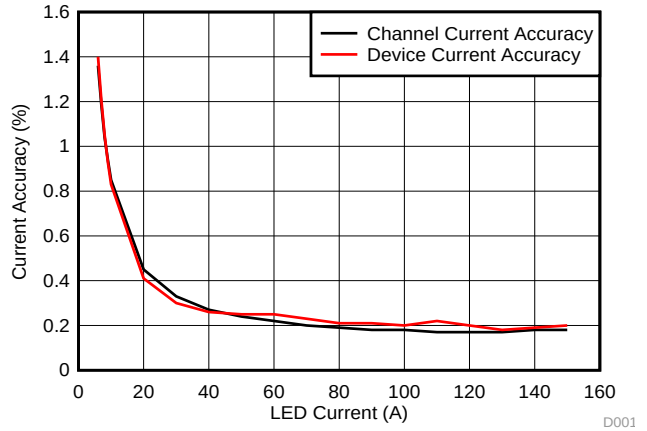
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FAULT ($\overline{FAULT}$)						
V_{IL}	Logic input low threshold				0.7	V
V_{IH}	Logic input high threshold		2			V
V_{OL}	Logic output low level	Tested with 500-µA external pullup			0.7	V
V_{OH}	Logic output high level	Tested with 1-µA external pulldown	2			V
$I_{(pulldown)}$	Strong pulldown current		500	750	1000	µA
$I_{(pullup)}$	Weak pullup current		4	8	16	µA
COMPARATOR (VSNSx)						
$V_{(VSNSx)}$	Internal comparator reference (for short circuit detection)	$V_{(VIN)} > V_{(th)}$	1.198	1.222	1.246	V
I_{lkg}	Leakage current	$V_{(VSNSx)}$ = 3 V			500	nA
$V_{(th)}$	Voltage at which the chip enables the single-short alarm function	Single-short detection enabled	8		9	V
	$V_{(th)\ hysteresis}$			145		mV
PROTECTION						
$V_{(OLV)}$	Open-load detection voltage	$V_{(OLV)} = V_{(VIN)} – V_{(IOUTx)}$	50	100	150	mV
$V_{(OL-hys)}$	Open-load detection hysteresis		100	200	300	mV
$V_{(SV)}$	Short-detection voltage		0.846	0.89	0.935	V
	Short-detection hysteresis		318	335	352	mV
	Short-detection deglitch		1	2	3	ms
		During PWM, count the number of continuous cycles when $V_{(IOUTx)} < V_{(SV)}$	7		8	Cycles
$R_{(REF_open)}$	REF pin resistor open detection	$\overline{FAULT}$ goes low	15	23	57	kΩ
$R_{(REF_short)}$	REF pin resistor short detection	$\overline{FAULT}$ goes low	350	470	800	Ω
THERMAL MONITOR						
$T_{(shutdown)}$	Thermal shutdown		155	170	170	°C
$T_{(hys)}$	Thermal shutdown hysteresis			15		°C
$T_{(th)}$	Thermal foldback activation temperature	90% of $I_{(IOUTx)}$ normal (TEMP pin floating)	95	110	125	°C
$I_{(TFCmin)}$	Minimum foldback current		40%	50%	60%	
$V_{(T-disable)}$	Thermal-foldback-function disable voltage			0	0.2	V

7.6 Timing Requirements

			MIN	NOM	MAX	UNIT
$t_{(startup)}$	Start-up time	$V_{(VIN)}$ > 5 V, $I_{(IOUTx)}$ = 50%, $I_{(setting)}$ = 60 mA (1)			200	µs
$t_{d(on)}$	Delay time between PWM rising edge to 10% of $I_{(IOUTx)}$	Two LEDs in series, 10-kΩ resistor in parallel		14	30	µs
$t_{d(off)}$	Delay time between PWM falling edge to 90% of $I_{(IOUTx)}$	Two LEDs in series, 10-kΩ resistor in parallel		25	45	µs
	Single-short detection deglitch		1	2	3	ms
		During PWM, count the number of continuous cycles when $V_{(VSNSx)}$ < 1.24 V	7		8	Cycles
	Open-load detection deglitch		1	2	3	ms
		During PWM, count the number of continuous cycles when $V_{(VIN)} – V_{(IOUTx)} < V_{(OLV)}$	7		8	Cycles
	Short-detection deglitch		1	2	3	ms
		During PWM, count the number of continuous cycles when $V_{(IOUTx)} < V_{(SV)}$	7		8	Cycles

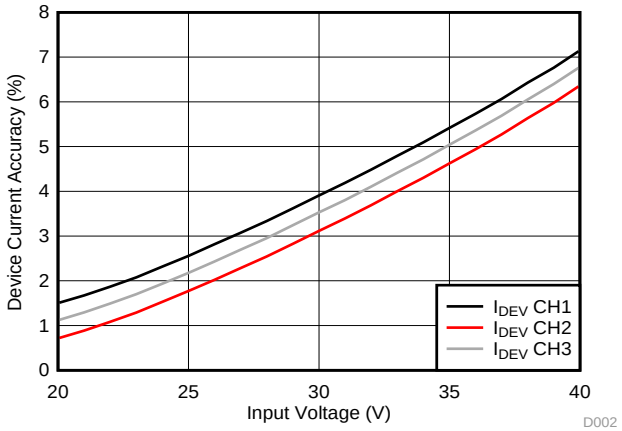
(1) Start-up is considered complete when $I_{(setting)}$ increases to 30 mA.

7.7 Typical Characteristics



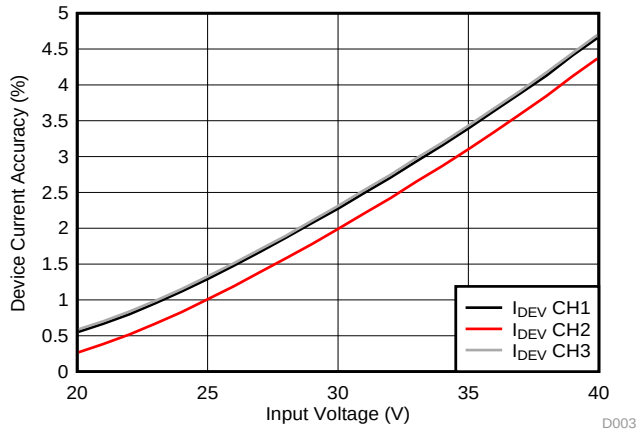
T_A = 25ºC $V_{(VIN)}$ = 14 V Three LEDs

Figure 1. Current Accuracy vs Current Setting



$V_{(VIN)}$ = 20 V $I_{(setting)}$ = 30 mA

Figure 2. Device Current Accuracy vs Input Voltage



$V_{(VIN)}$ = 20 V $I_{(setting)}$ = 150 mA

Figure 3. Device Current Accuracy vs Input Voltage

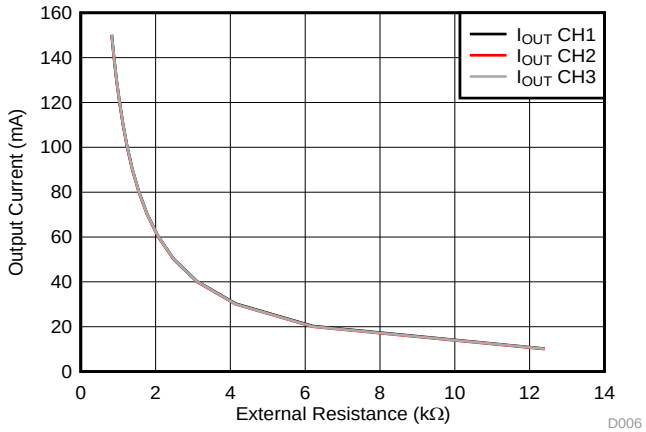
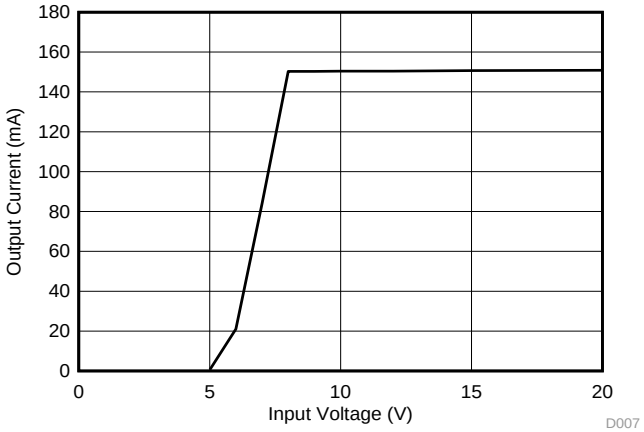
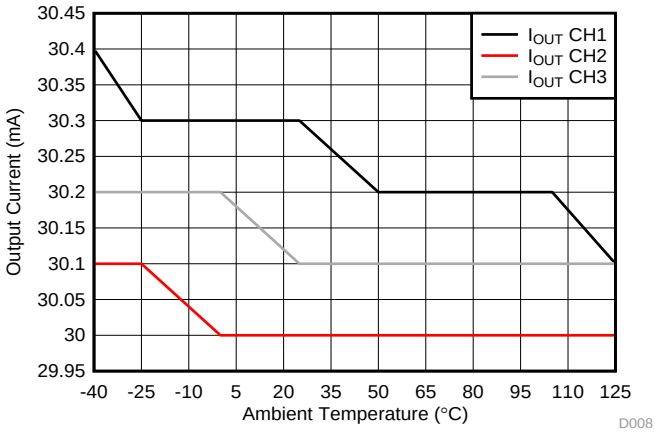


Figure 4. Output Current vs External Resistance



3 white LEDs LEDs in series $I_{(setting)}$ = 150 mA

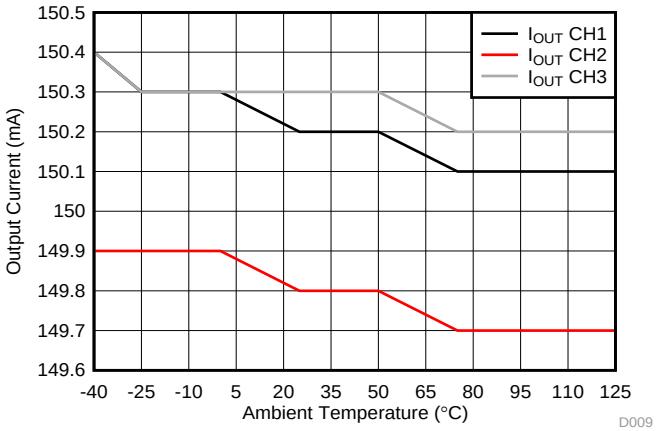
Figure 5. Output Current vs Input Voltage



$I_{(setting)}$ = 30 mA $V_{(VIN)}$ = 14 V

Figure 6. Output Current vs Ambient Temperature

Typical Characteristics (continued)



$I_{(setting)}$= 150 mA $V_{(VIN)}$ = 14 V

Figure 7. Output Current vs Ambient Temperature

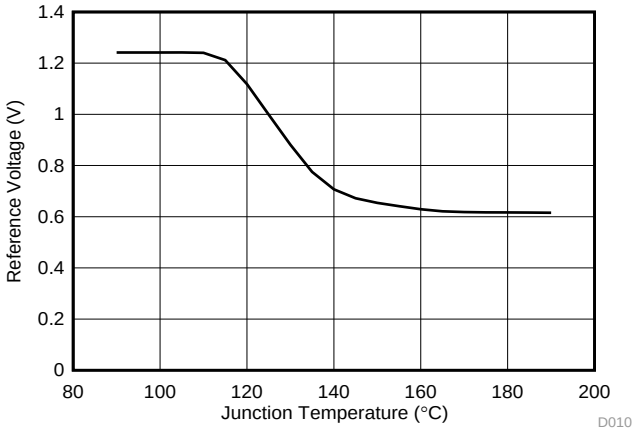
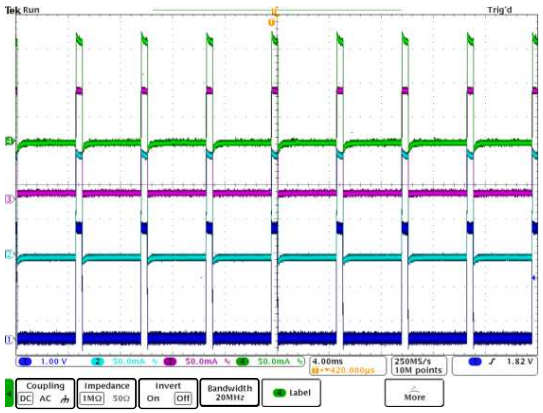
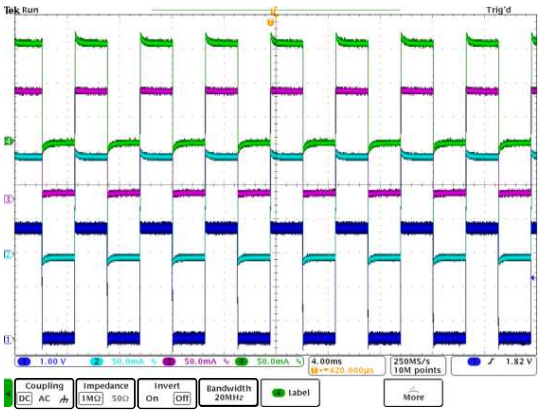


Figure 8. Reference Voltage vs Junction Temperature With Thermal Foldback



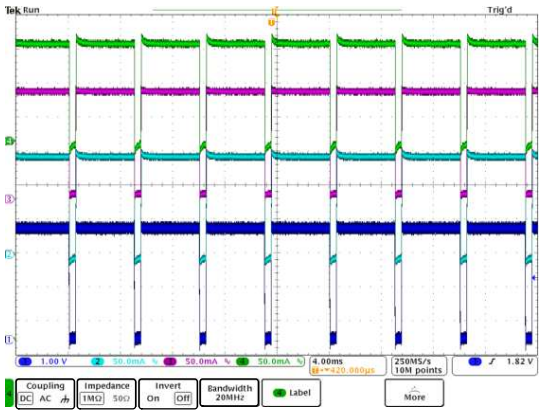
Ch. 1 = PWM input Ch. 2 = IOUT1 Ch. 3 = IOUT2
Ch. 4 = IOUT3 $f_{(PWM)}$ = 200 Hz Duty cycle = 10%

Figure 9. PWM Dimming



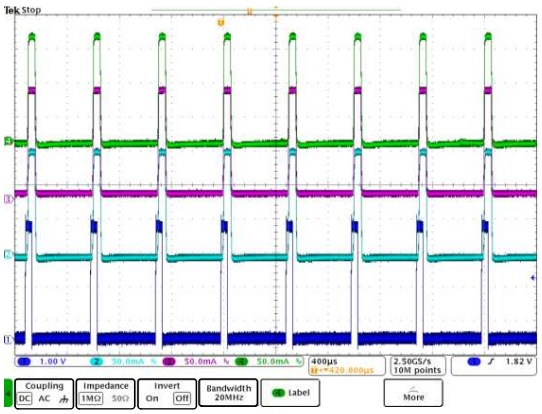
Ch. 1 = PWM input Ch. 2 = IOUT1 Ch. 3 = IOUT2
Ch. 4 = IOUT3 $f_{(PWM)}$ = 200 Hz Duty cycle = 50%

Figure 10. PWM Dimming



Ch. 1 = PWM input Ch. 2 = IOUT1 Ch. 3 = IOUT2
Ch. 4 = IOUT3 $f_{(PWM)}$ = 200 Hz Duty cycle = 90%

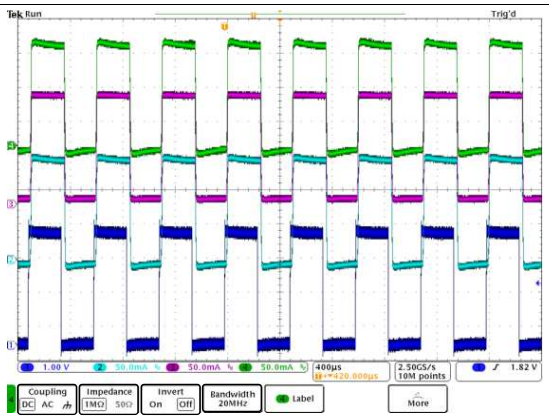
Figure 11. PWM Dimming



Ch. 1 = PWM input Ch. 2 = IOUT1 Ch. 3 = IOUT2
Ch. 4 = IOUT3 $f_{(PWM)}$ = 2000 Hz Duty cycle = 10%

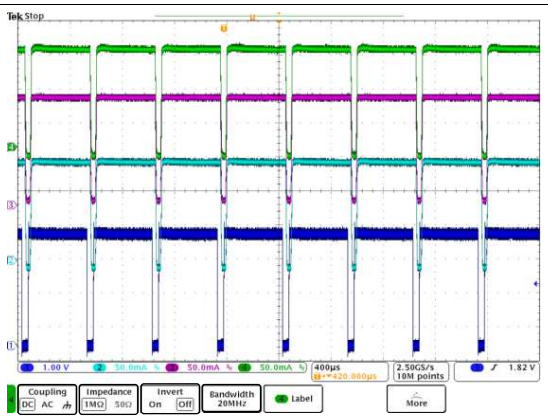
Figure 12. PWM Dimming

Typical Characteristics (continued)



Ch. 1 = PWM input
Ch. 2 = IOUT1
Ch. 3 = IOUT2
Ch. 4 = IOUT3
$f_{(PWM)}$ = 2000 Hz
Duty cycle = 50%

Figure 13. PWM Dimming



Ch. 1 = PWM input
Ch. 2 = IOUT1
Ch. 3 = IOUT2
Ch. 4 = IOUT3
$f_{(PWM)}$ = 2000 Hz
Duty cycle = 90%

Figure 14. PWM Dimming

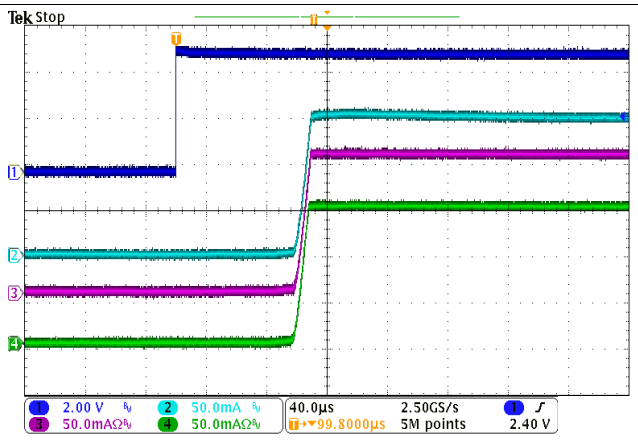
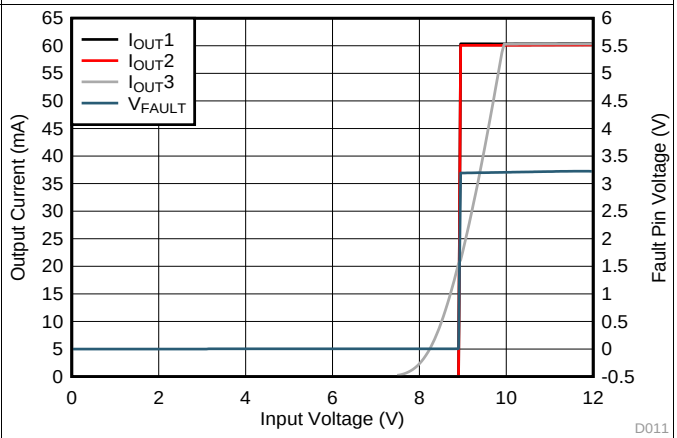


Figure 15. Fast Power-Up Waveform



$V_{(VIN)}$ = $V_{(EN)}$
3 white LEDs
$V_{(VIN)}$ = 0 V to 12 V
dV/dt = 0.5 V/min
$I_{(setting)}$ = 60 mA

Figure 16. Slow Power-Up Waveform

8 Parameter Measurement Information

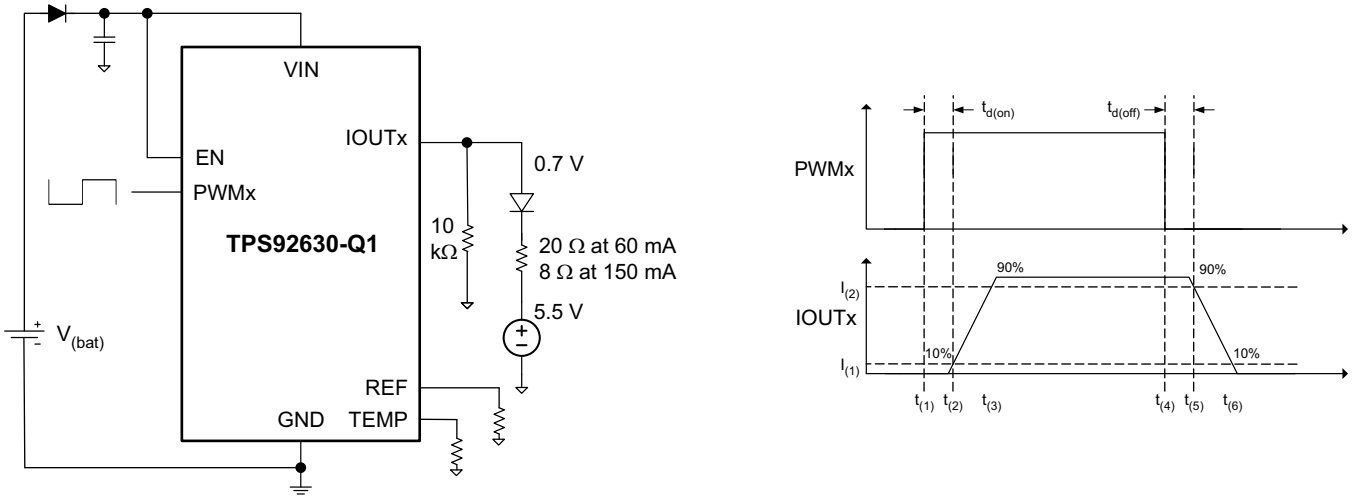


Figure 17. Load Model for Slew-Rate and Delay-Time Tests

9 Detailed Description

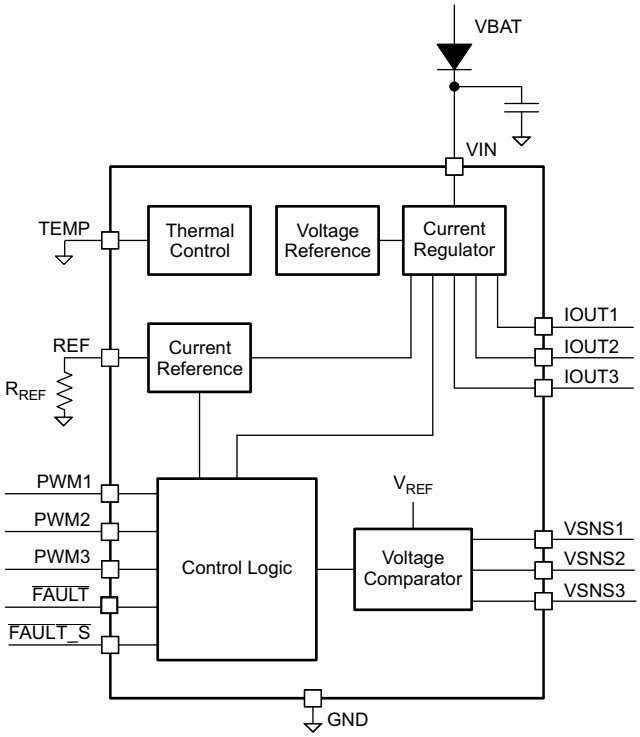
9.1 Overview

The TPS92630-Q1 device is a three-channel constant-current regulator with individual PWM dimming, designed for high brightness red or white LEDs in automotive lighting applications. Each channel has up to 150-mA current capability, giving a combined 450-mA current capability when paralleled. The device provides excellent current matching between channels and devices. A high-side current source allows LED common-cathode connections. The advanced control loop allows high accuracy between channels, even when different numbers of LEDs are connected on the output. Use of a separate PWM channel dims or disables each channel.

The TPS92630-Q1 device monitors fault conditions on the output and reports its status on the $\overline{\text{FAULT}}$ and $\overline{\text{FAULT_S}}$ pins. It features single-shorted-LED detection, output short-to-ground detection, open-load detection, and thermal shutdown. Two separate fault pins allow maximum flexibility of fault-mode reporting to the MCU in case of an error. In case there is no MCU, one can connect multiple TPS92630-Q1 devices in a bus mode.

Integrated thermal foldback protects the devices from thermal shutdown by reducing the output current linearly when reaching a preset threshold. Use an external resistor to program the temperature foldback threshold. Tying the TEMP pin to ground disables this function.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Constant LED-Current Setting

Control of the three LED output channels is through separate linear current regulators. A common external resistor sets the current in each channel. The device also features two current levels with external circuitry, intended for stop- and tail-light applications.

See Equation 1 on how to set the current:

Feature Description (continued)

$$I_{(IOUTx)} = \frac{V_{ref} \times K_{(I)}}{R_{(REF)}}$$

$$R_{(REF)} = \frac{V_{ref} \times K_{(I)}}{I_{(IOUTx)}} \quad (1)$$

9.3.2 PWM Control

The device features a separate PWM dimming control pin for each output channel. PWM inputs also function as shutdown pin when an output is unused. Tying PWM to ground disables the corresponding output. The PWM signal has a precise threshold, which one can use to define the start-up voltage of LED as an undervoltage-lockout (UVLO) function with the divider resistor from the VIN pin.

9.3.3 $\overline{\text{FAULT}}$ Diagnostics

The TPS92630-Q1 device has two fault pins, $\overline{\text{FAULT}}$ and $\overline{\text{FAULT_S}}$. $\overline{\text{FAULT_S}}$ is a dedicated fault pin for single-LED short failure and $\overline{\text{FAULT}}$ is for general faults, that is, short, open, and thermal shutdown. The dual pins allow maximum flexibility based on all requirements and application conditions.

The device fault pins can be connected to an MCU for fault reporting. Both fault pins are open-drain transistors with a weak internal pullup. See Figure 19.

Feature Description (continued)

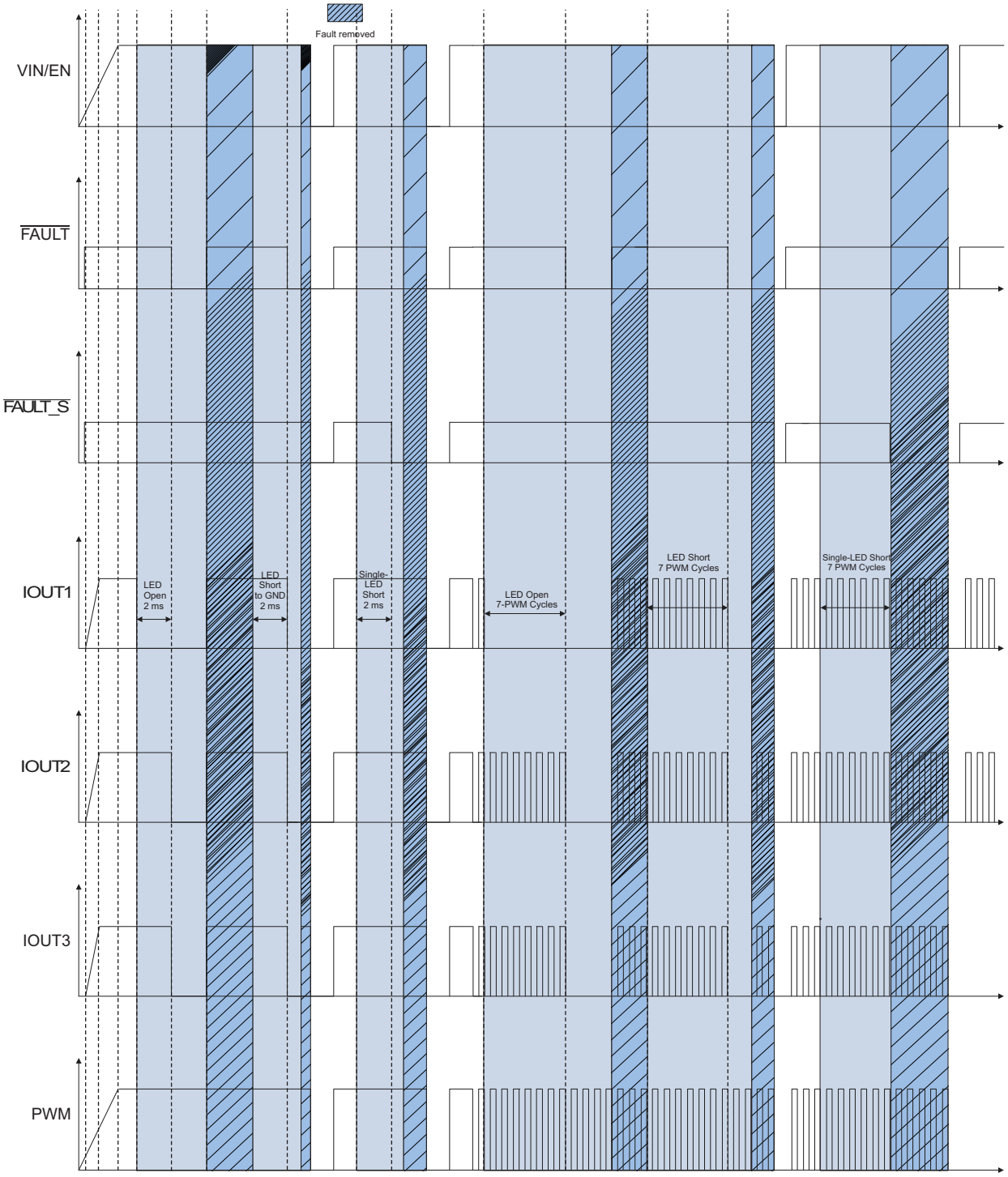


Figure 18. Detailed Timing Diagram

In case there is no MCU, one can connect up to 15 TPS92630-Q1 $\overline{\text{FAULT}}$ and $\overline{\text{FAULT_S}}$ pins together. When one or more devices have errors, the respective $\overline{\text{FAULT}}$ pins go low, pulling the connected $\overline{\text{FAULT}}$ bus down and shutting down all device outputs. Figure 19 shows the fault-line bus connection.

Feature Description (continued)

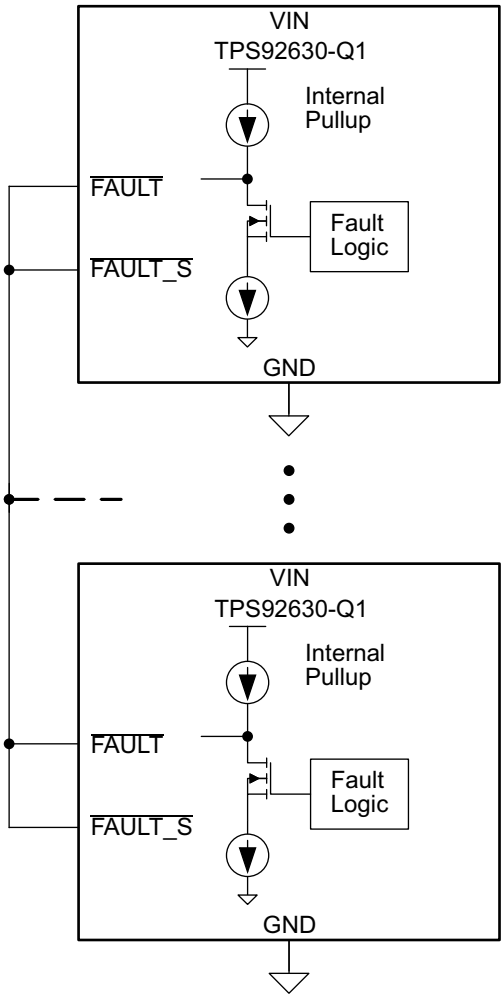


Figure 19. Fault-Line Bus Connection

The device releases the FAULT bus when external circuitry pulls the $\overline{\text{FAULT}}$ pin high, on toggling of the EN pin, or on a power cycle of the device. In case there is no MCU, only a power cycle clears the fault. See Figure 20.

Feature Description (continued)

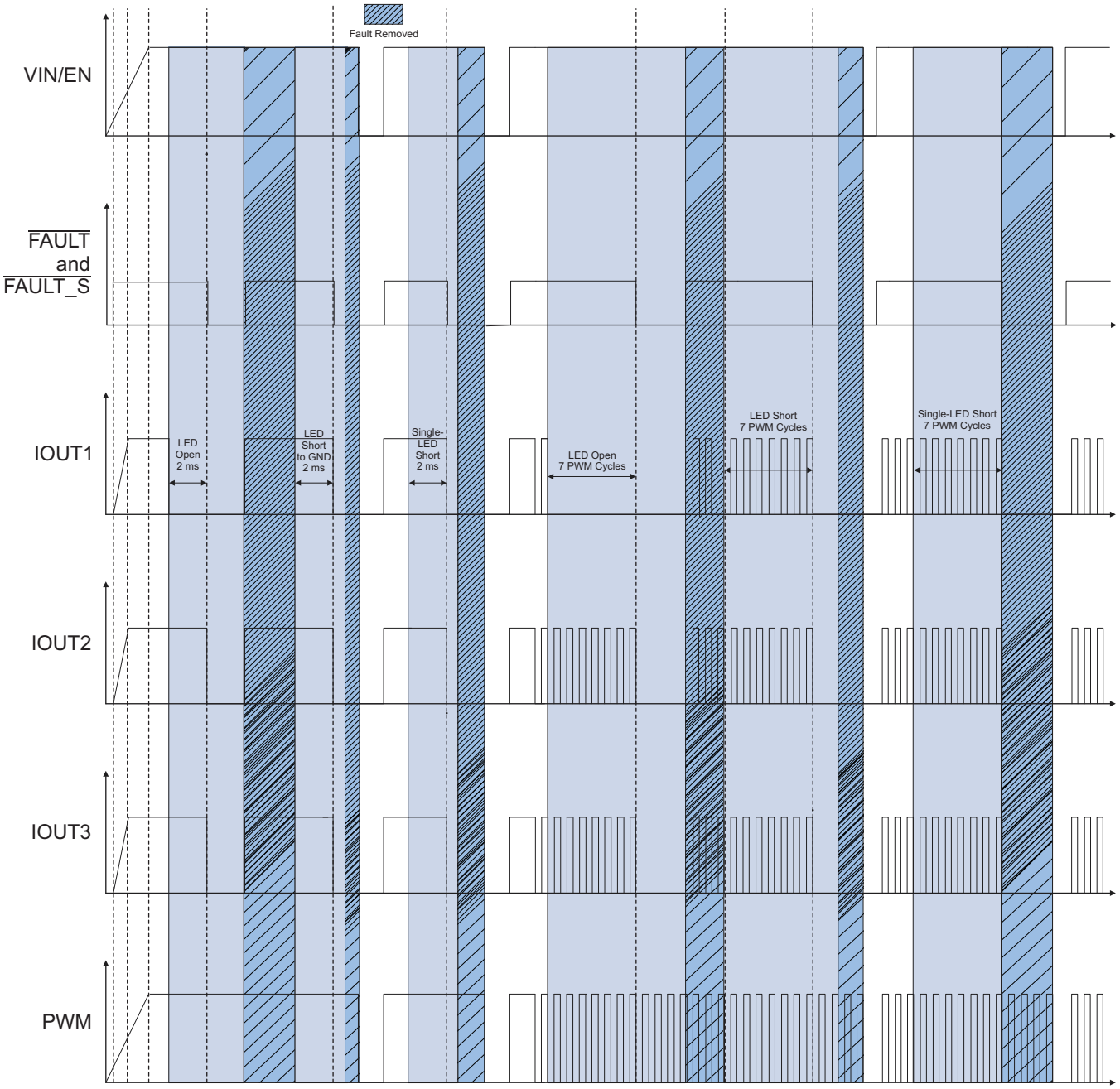


Figure 20. Detailed Timing Diagram

The following faults result in the $\overline{\text{FAULT}}$ or $\overline{\text{FAULT_S}}$ pin going low: thermal shutdown, open load, output short circuit, single LED short, and REF open or shorted. For thermal shutdown or LED open, release of the $\overline{\text{FAULT}}$ pin occurs when the thermal-shutdown or LED-open condition no longer exists. For other faults, the $\overline{\text{FAULT}}$ and $\overline{\text{FAULT_S}}$ pins stay low even if the condition does not exist. Clearing the faults requires a power cycle of the device.

Feature Description (continued)

9.3.4 Short-Circuit Detection

The device includes three internal comparators for LED forward-voltage measurement. With external resistor dividers, the device compares total LED forward voltage with the internal reference voltage. This feature enables the detection of one or more shorted LEDs. Any LED cathode or IOUTx pin shorted to ground results in a short-circuit condition. The external resistor dividers control the detection-threshold-voltage setting.

Figure 21 illustrates different short-circuit conditions.

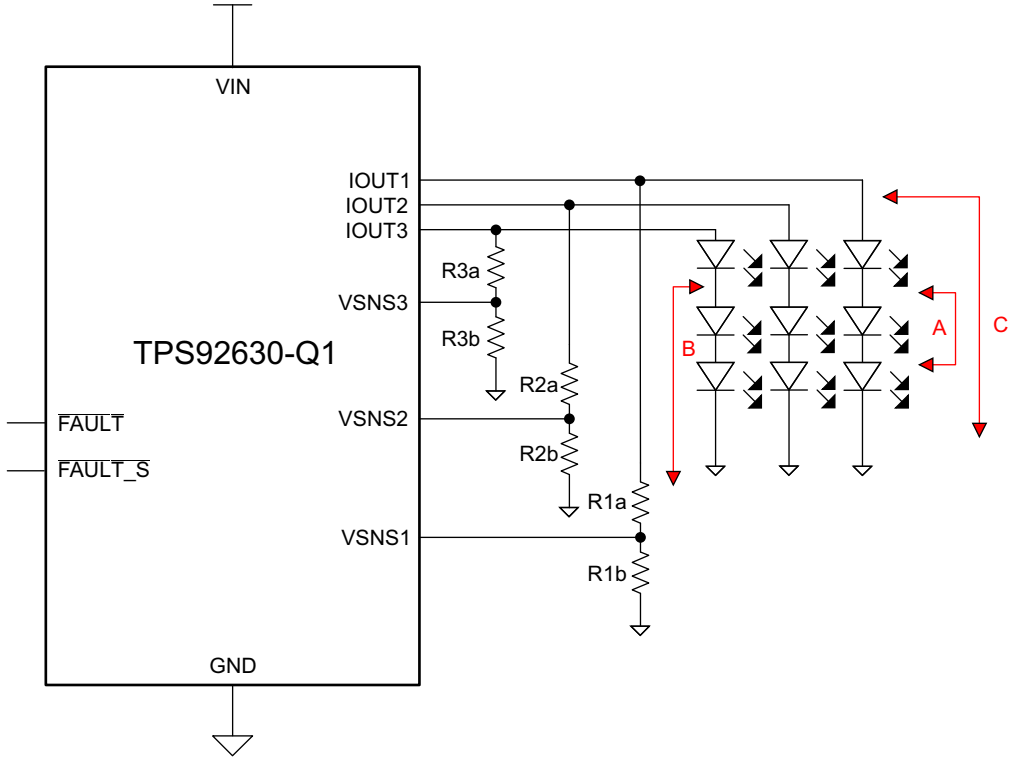


Figure 21. Short-Circuit Conditions

A short in one or more LEDs in a string (A and B as illustrated) registers as only a single-LED short when $V_{(VIN)}$ > 9 V.

- The device reports the failure to the MCU. The faulted channel continues sourcing current until the MCU takes actions to turn off channels through the EN or PWMx pin.
- No MCU: with $\overline{\text{FAULT_S}}$ floating, no action results. With $\overline{\text{FAULT_S}}$ tied to $\overline{\text{FAULT}}$, all output channels shut down together.

When an entire string of LEDs is shorted (C as illustrated), the device pulls $\overline{\text{FAULT}}$ low to shut down all channels. With the $\overline{\text{FAULT}}$ pin tied high, only the faulted channel turns off.

- $V_{F(max)}$ – maximum forward voltage of LED used
- $V_{F(min)}$ – minimum forward voltage of LED used
- N – Number of LEDs used in a string
- R – resistor divider ratio
- $V_{(VSNSx)}$ – internal reference voltage of comparators

When selecting R, observe the following relationship to avoid false triggering.

$$R = (Rxa + Rxb) / Rxb \quad (2)$$

$$(N - 1) \times V_{F(max)} < V_{(VSNSx)} \times R < N \times V_{F(min)} \quad (3)$$

Feature Description (continued)

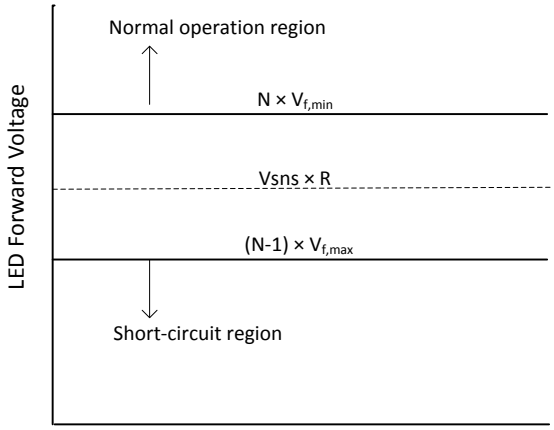


Figure 22. Single-LED Short-Trigger Calculation

9.3.5 Open-Load Detection

Detection of an open-load condition occurs when the voltage across the channel, $V_{(VIN)} – V_{(IOUTx)}$, is less than the open-load detection voltage, $V_{(OLV)}$. When this condition is present for more than the open-load-detection deglitch (2 ms when PWM is 100% on or one PWM on-time is more than 2 ms, or seven continuous PMW duty cycles when in PWM dimming mode), the $\overline{\text{FAULT}}$ pin goes low, keeping the open channel on and turning the other channel off. With the $\overline{\text{FAULT}}$ pin tied high, all channels remain turned on. The channel recovers on removal of the open condition. Note that the device can detect an open load if the sum of the forward voltages of the LEDs in a string is close to or greater than the supply voltage on VIN.

Table 1. Fault Table(1) (2)

FAILURE MODE	JUDGMENT CONDITION			DIAGNOSTIC OUTPUT PINS	ACTION	$\overline{\text{FAULT}}$ AND $\overline{\text{FAULT_S}}$ (3)	DEVICE REACTION	FAILURE REMOVED	SELF-CLEARING
	DETECTION VIN VOLTAGE	CHANNEL STATUS	DETECTION MECHANISM						
Short circuit: 1 or several LED strings	$V_{(VIN)}$ > 5 V	ON	$V_{(IOUTx)}$ < 0.9 V	$\overline{\text{FAULT}}$	Pulled low	Externally pulled high	Failing strings turned off, other channels on	Toggle EN, power cycle	No
						Floating	All strings turned OFF	Toggle EN, power cycle	
Single-LED short circuit: 1 or several LED strings	$V_{(VIN)}$ > 9 V	ON	$V_{(VSNSx)}$ < 1.222 V	$\overline{\text{FAULT_S}}$	Pulled low	Externally pulled high	All strings stay ON	Toggle EN, power cycle	No
						Floating	All strings stay ON	Toggle EN, power cycle	
Open load: 1 or several LED strings	$V_{(VIN)}$ > 5 V	ON	$V_{(VIN)} – V_{(IOUTx)}$ < 100 mV	$\overline{\text{FAULT}}$	Pulled low	Externally pulled high	All strings stay ON		Yes
						Floating	Failing string stays ON, other channels turned OFF		
Short to battery: 1 or several LED strings	$V_{(VIN)}$ > 5 V	ON or OFF	$V_{(VIN)} – V_{(IOUTx)}$ < 100 mV	$\overline{\text{FAULT}}$	Pulled low	Externally pulled high	All strings stay ON		Yes
						Floating	Failing string stays ON, other channels turned OFF		
Thermal shutdown	$V_{(VIN)}$ > 5 V	ON or OFF	Temperature > 170°C	$\overline{\text{FAULT}}$	Pulled low	Externally pulled high	All strings turned OFF	Temperature < 155°C	Yes
						Leave open			
Thermal foldback	$V_{(VIN)}$ > 5 V	ON or OFF	Temperature > 110°C	N/A	None	N/A	All strings with reduced current	Temperature < 100°C	Yes

(1) With diagnostic pins $\overline{\text{FAULT}}$ and $\overline{\text{FAULT_S}}$ tied high externally, pullup must be strong enough to override internal pulldown.
(2) To achieve single-LED short circuit to turn off all strings, $\overline{\text{FAULT_S}}$ and $\overline{\text{FAULT}}$ pins must be connected together.
(3) Pulling $\overline{\text{FAULT}}$ and $\overline{\text{FAULT_S}}$ high externally changes the behavior of the device reaction. If not externally forced high, the device pulls the pins low based on the failure mode.

Feature Description (continued)

Table 1. Fault Table(1) (2) (continued)

FAILURE MODE	JUDGMENT CONDITION			DIAGNOSTIC OUTPUT PINS	ACTION	$\overline{\text{FAULT}}$ AND $\overline{\text{FAULT_S}}$ (3)	DEVICE REACTION	FAILURE REMOVED	SELF-CLEARING
	DETECTION VIN VOLTAGE	CHANNEL STATUS	DETECTION MECHANISM						
Reference resistor open or shorted	$V_{(VIN)}$ > 5 V	ON or OFF	$R_{(REF)}$ > 57 kΩ or $R_{(REF)}$ < 350 Ω	$\overline{\text{FAULT}}$	Pulled low	N/A	All strings turned OFF	Toggle EN, power cycle	No

9.3.6 Thermal Foldback

The TPS92630-Q1 device integrates thermal shutdown protection to prevent the device from overheating. In addition, to prevent LEDs from flickering because of rapid thermal changes, the device includes a programmable thermal current-foldback feature to reduce power dissipation at high junction temperatures.

The TPS92630-Q1 device reduces the LED current as the silicon junction temperature of the TPS92630-Q1 device increases (see Figure 23). By mounting the TPS92630-Q1 device on the same thermal substrate as the LEDs, use of this feature can also limit the dissipation of the LEDs. As the junction temperature of the TPS92630-Q1 device increases, the device reduces the regulated current, reducing the dissipated power in the TPS92630-Q1 device and in the LEDs. The current reduction is from the 100% level at typically 2% of $I_{(setting)}$ per ºC until the point at which the current drops to 50% of the full value.

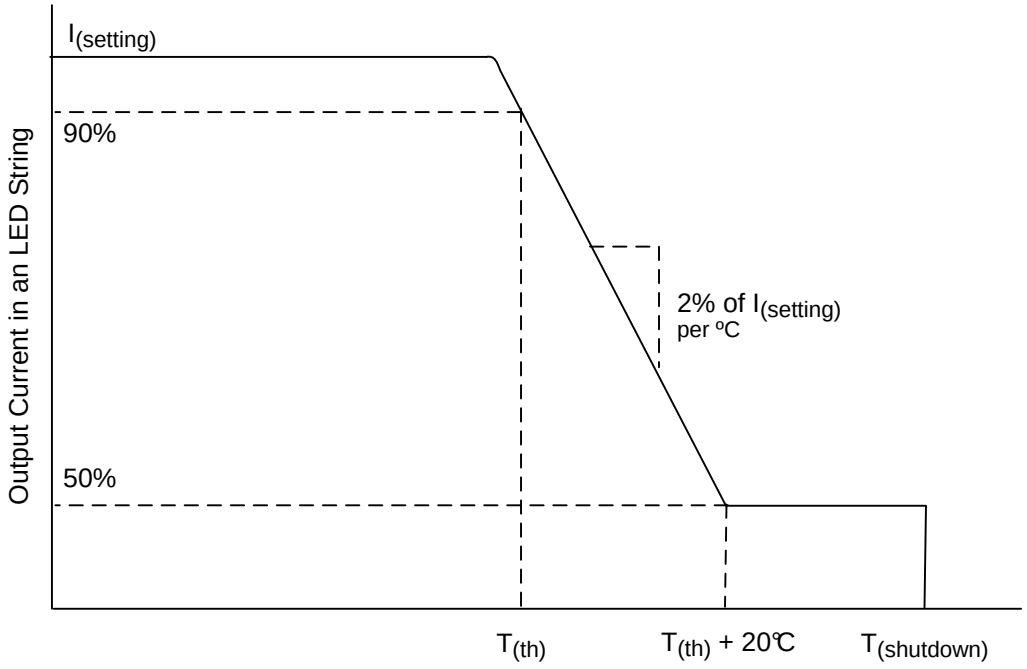


Figure 23. Thermal Foldback

Above this temperature, the current continues to decrease at a lower rate until the temperature reaches the overtemperature shutdown threshold temperature, $T_{(shutdown)}$. Changing the voltage on the TEMP pin adjusts the temperature at which the current reduction begins. With TEMP floating, the definition of thermal monitor activation temperature, $T_{(th)}$, is the temperature at which the current reduction begins. The specification of $T_{(th)}$ in the characteristics table is at the 90% current level. $T_{(th)}$ increases as the voltage at the TEMP pin, $V_{(TEMP)}$, declines and is defined as approximately:

$$T_{(th)} = –121.7\ V_{(TEMP)} + 228.32 \quad (4)$$

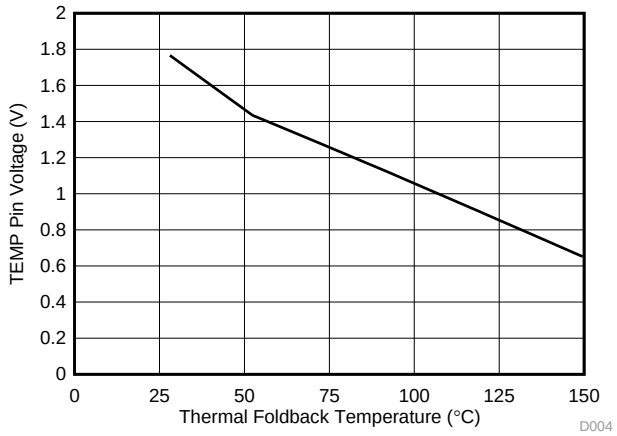


Figure 24. TEMP Pin Voltage vs Temperature

A resistor connected between TEMP and GND reduces $V_{(TEMP)}$ and increases $T_{(th)}$. A resistor connected between TEMP and a reference supply greater than 1 V increases $V_{(TEMP)}$ and reduces $T_{(th)}$.

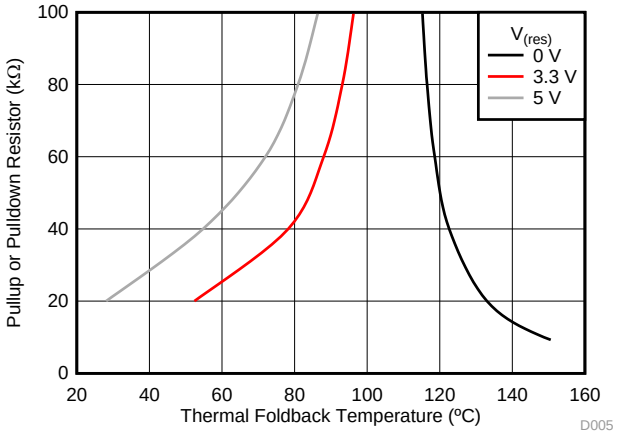


Figure 25. Pullup and Pulldown Resistors vs $T_{(th)}$

Figure 25 shows how the nominal value of the thermal-monitor activation temperature varies with the voltage at TEMP and with either a pulldown resistor to GND or with a pullup resistor to 3.3 V or 5 V.

In extreme cases, if the junction temperature exceeds the overtemperature limit, $T_{(shutdown)}$, the device disables all channels. Temperature monitoring continues, and channel reactivation occurs when the temperature drops below the threshold provided by the specified hysteresis.

Note the possibility of the TPS92630-Q1 device transitioning rapidly between thermal shutdown and normal operation. This can happen if the thermal mass attached to the exposed thermal pad is small and $T_{(th)}$ is increased to close to the shutdown temperature. The period of oscillation depends on $T_{(th)}$, the dissipated power, the thermal mass of any heatsink present, and the ambient temperature.

9.4 Device Functional Modes

9.4.1 Thermal Information

This device operates a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the thermal-shutdown trip point. If the junction temperature exceeds the thermal-shutdown trip point, the output turns off. When the junction temperature falls below the thermal-shutdown trip point, the output turns on again.

Calculate the power dissipated by the device according to the following formula:

Device Functional Modes (continued)

$$P_T = V_{(VIN)} \times I_{(VIN)} - n_1 \times V_{(LED1)} \times I_{(LED1)} - n_2 \times V_{(LED2)} \times I_{(LED2)} - n_3 \times V_{(LED3)} \times I_{(LED3)} - V_{ref}{}^2 / R_{(REF)} \quad (5)$$

where:

P_T = Total power dissipation of the device
n_x = Number of LEDs for channel x
$V_{(LEDx)}$ = Voltage drop across one LED for channel x
V_{ref} = Reference voltage, typically 1.222 V
$I_{(LEDx)}$ = Average LED current for channel x

After determining the power dissipated by the device, calculate the junction temperature from the ambient temperature and the device thermal impedance.

$$T_J = T_A + R_{\theta JA} \times P_T \quad (6)$$

9.4.2 Operation With $V_{(VIN)}$ < 5 V (Minimum $V_{(VIN)}$)

The devices operate with input voltages above 5 V. The devices start working when $V_{(VIN)}$ > 4 V, but while 4 V < $V_{(VIN)}$ < 5 V, the devices shield all the fault status. With fault status shielded, if any fault occurs the devices may not report the fault and take the correct action.

9.4.3 Operation With 5 V < $V_{(VIN)}$ < 9 V (Lower-Than-Normal Automotive Battery Voltage)

The devices operate with input voltages above 5 V. When the input voltage is lower than normal automotive 9 V, the devices shield single-LED-short fault status. With fault status shielded, if a single-LED-short fault occurs the devices do not report the fault with the $\overline{\text{FAULT_S}}$ pin.

10 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The following discussion includes several applications showing how to implement the TPS92630-Q1 device for automotive lighting such as stop lights and taillights. Some of the examples demonstrate implementation of the fault bus function or detail use of the device for higher-current applications.

10.2 Typical Applications

10.2.1 Stoplight and Taillight Application With PWM Generator

Another easy way to achieve the different brightness is dimming by pulse-width modulation (PWM), which holds the color spectrum of the LED over the whole brightness range. The maximum current that passes through the LED is programmable by sense resistor R_{REF}.

Figure 26 shows the application circuit of the stoplight and taillight including an automotive-qualified timer, TLC555-Q1, the duty cycle of which is programmable by two external resistors. One can see that driving the STOP signal high pulls the PWM pin constantly high, creating 100% duty cycle. Thus the LEDs operate at full brightness. When the TAIL signal is high, the LEDs operate at 50% brightness because the TLC555-Q1 timer is programmed at a fixed duty cycle of 50%.

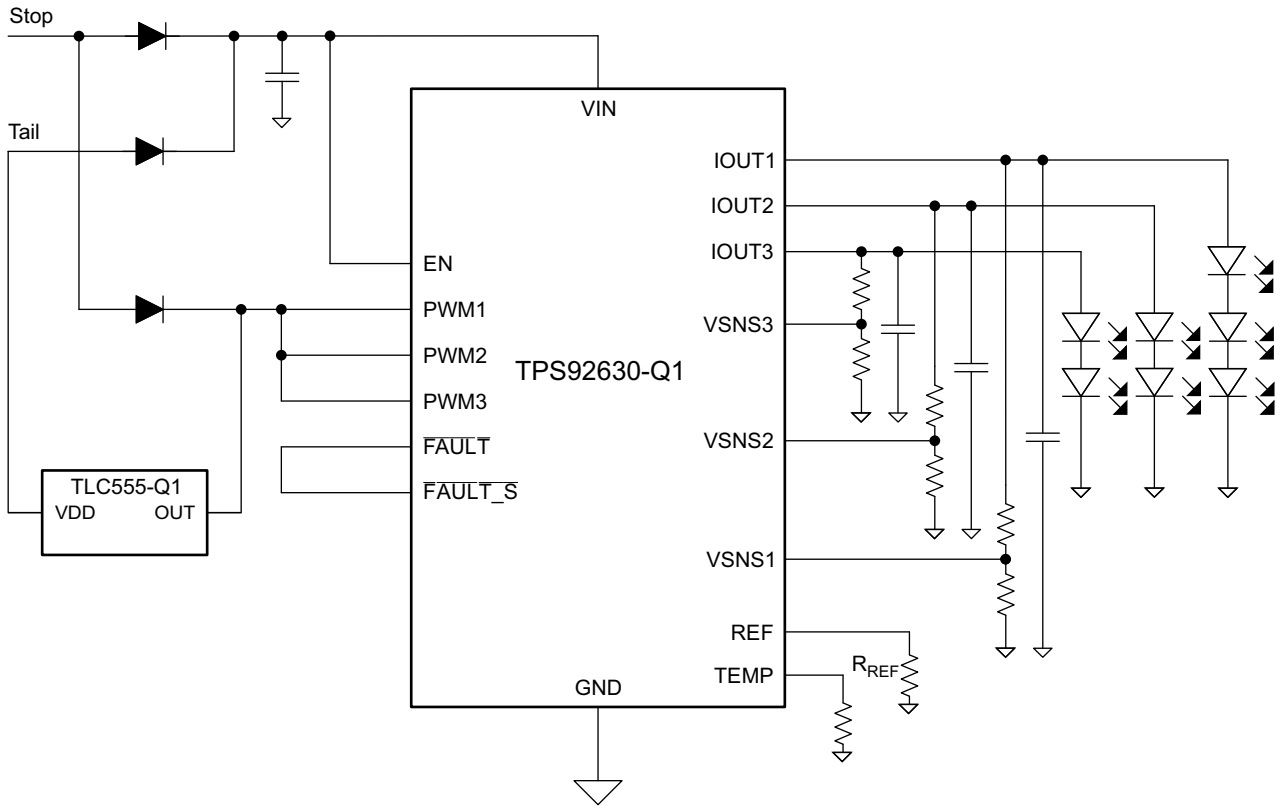


Figure 26. Two-Level Brightness Adjustment Using the TPS92630-Q1 With PWM

Typical Applications (continued)

10.2.1.1 Design Requirements

For this design example, use the following as the input parametrers.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
$I_{(tail)}$	75
$I_{(stop)}$	150

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Step-by-Step Design Procedure

To begin the design process, one must decide on a few parameters. The designer must know the following:

- $I_{(tail)}$ – Taillight current
- $I_{(stop)}$ – Stop-light current

10.2.1.2.1.1 $R_{(REF)}$

$$R_{(REF)} = V_{ref} \times K_{(I)} / I_{(stop)} = 1.222 \times 100 / 0.15 = 814\ \Omega \quad (7)$$

10.2.1.2.1.2 Duty Cycle

$$\text{Duty cycle} = I_{(tail)} / I_{(stop)} = 75 / 150 = 50\% \quad (8)$$

10.2.1.2.1.3 Input and Output Capacitors

TI recommends to add capacitors at VIN and IOUTx. TI recommends an input capacitor of at least 1 µF close to the VIN pin, and output capacitors of 10 nF close to the IOUTx pins. Larger capacitors are helpful for EMC and ESD; however, it takes a longer time to charge up the capacitor and could affect PWM dimming performance.

10.2.1.3 PWM Dimming Application Curve

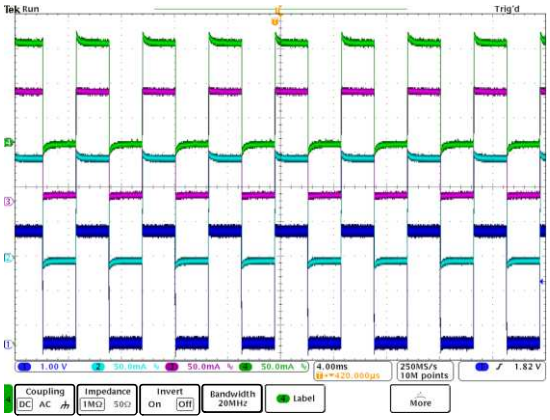


Figure 27. PWM Dimming Application Curve

10.2.2 Simple Stop-Light and Taillight Application

For many automobiles, the same set of LEDs illuminates both taillights and stop lights. Thus, the LEDs must operate at two different brightness levels. Figure 28 shows two-level brightness adjustment using the TPS92630-Q1 device with minimum external components. Set the dimming level with a parallel resistor in REF through an external MOS. See Equation 9 for details.

$$I_{(IOUTx)} = \frac{V_{ref} \times K_{(I)}}{R_{(REF)} \times R_{(Stop)} / (R_{(REF)} + R_{(Stop)})} \quad (9)$$

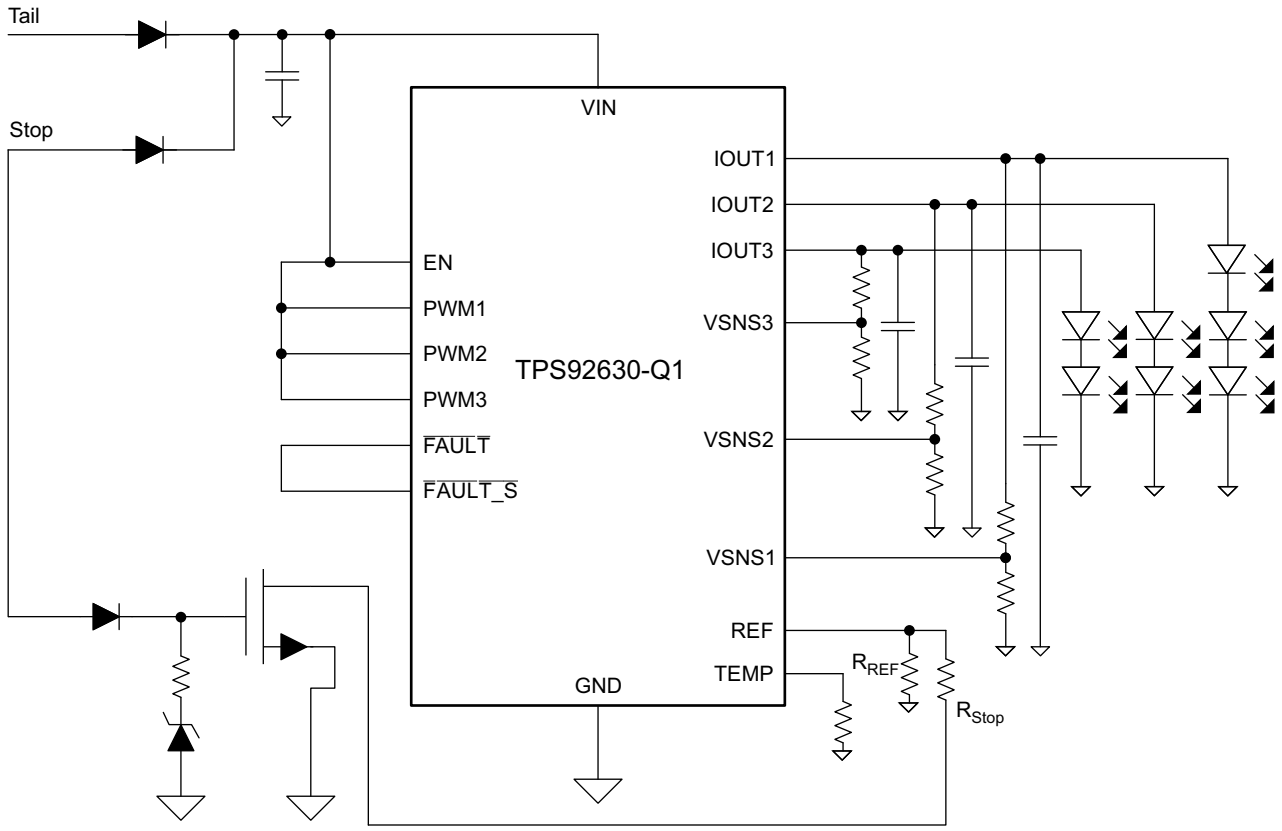


Figure 28. Two-Level Brightness Adjustment Using the TPS92630-Q1 Device With Minimum External Components

10.2.2.1 Design Requirements

For this design example, use the following as the input parameters.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
$I_{(Tail)}$	30 mA
$I_{(Stop)}$	70 mA

10.2.2.2 Detailed Design Procedure

10.2.2.2.1 Step-by-Step Design Procedure

To begin the design process, one must decide on a few parameters. The designer must know the following:

- $I_{(Tail)}$ – Taillight current
- $I_{(Stop)}$ – Stop-light current

10.2.2.2.1.1 $R_{(REF)}$

$$R_{(REF)} = V_{ref} \times K_{(I)} / I_{(tail)} = 1.222 \times 100 / 0.03 = 4.072\ k\Omega \quad (10)$$

10.2.2.2.1.2 $R_{(Stop)}$

$$R_{(Stop)} = V_{ref} \times K_{(I)} / (I_{(stop)} – I_{(tail)}) \ 1.222 \times 100 / (0.07 – 0.03) = 3.055\ k\Omega \quad (11)$$

10.2.2.2.1.3 Input and Output Capacitors

TI recommends to add capacitors at VIN and IOUTx. TI recommends an input capacitor of at least 1 µF close to the VIN pin, and output capacitors of 10 nF close to the IOUTx pins. Larger capacitors are helpful for EMC and ESD; however, it takes a longer time to charge up the capacitor and could affect PWM dimming performance.

10.2.3 Parallel Connection

This device can drive up to three strings with one to three LEDs in each string, at a total current up to 150 mA per channel. Outputs can be paralleled to provide higher current drive up to 450 mA. For example, if the load current is up to 2 times the device rating, connect the outputs of two devices in parallel as shown in Figure 29.

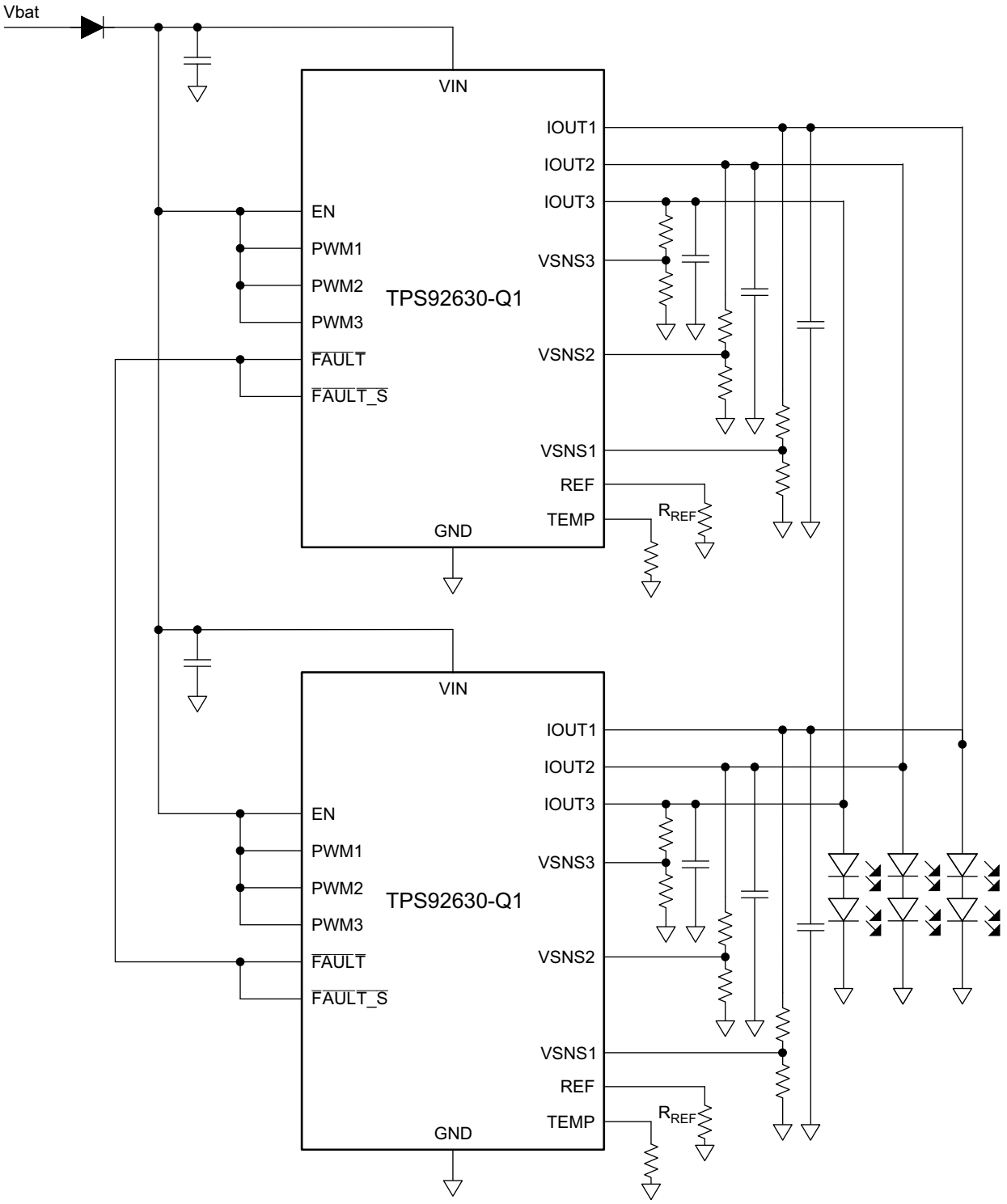


Figure 29. Two TPS92630-Q1 Devices in Parallel for Large Loads

10.2.3.1 Design Requirements

For this design example, use the following as the input parameters.

Table 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
$I_{(LED)}$ per string	200 mA

10.2.3.2 Detailed Design Procedure

10.2.3.2.1 Step-by-Step Design Procedure

To begin the design process, one must decide on a few parameters. The designer must know the following:

$I_{(LED)}$ per string

10.2.3.2.1.1 $R_{(REF)}$

$$R_{(REF)} = V_{ref} \times K_{(I)} / (I_{(LED)} / \text{Channel}) = 1.222 \times 100 / (200 / 2) = 1.222\ k\Omega \quad (12)$$

10.2.3.2.1.2 Input and Output Capacitors

TI recommends to add capacitors at VIN and IOUTx. TI recommends an input capacitor of at least 1 µF close to the VIN pin, and output capacitors of 10 nF close to the IOUTx pins. Larger capacitors are helpful for EMC and ESD; however, it takes a longer time to charge up the capacitor and could affect PWM dimming performance.

10.2.4 Alternate Parallel Connection

An alternate method of connecting two devices in parallel drives six LEDs while getting better thermal performance (see Figure 30).

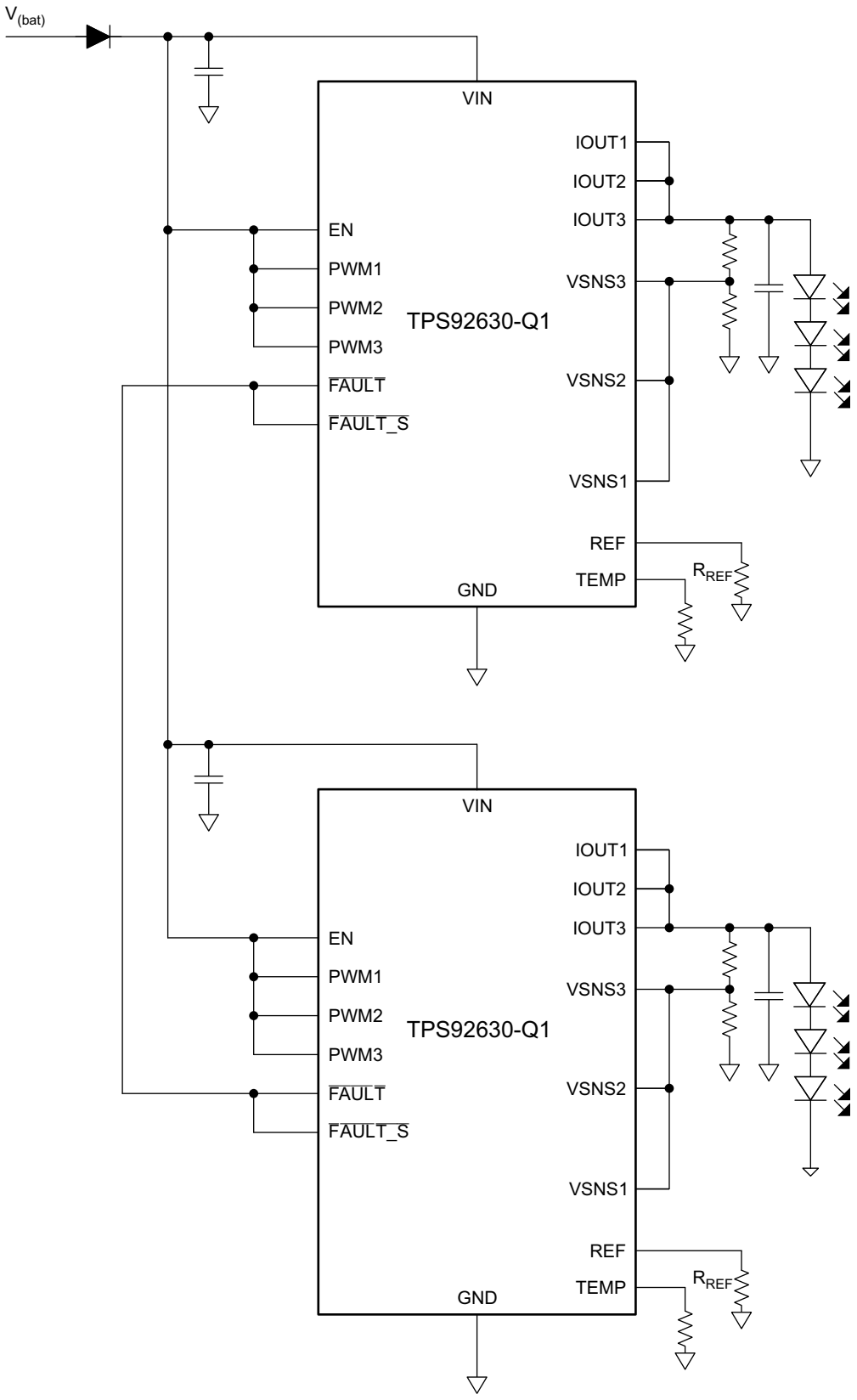


Figure 30. Two TPS92630-Q1 Devices in Parallel for Large Loads

10.2.4.1 Design Requirements

For this design example, use the following as the input parameters.

Table 5. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
$I_{(LED)}$ per string	300 mA

10.2.4.2 Detailed Design Procedure

10.2.4.2.1 Step-by-Step Design Procedure

To begin the design process, one must decide on a few parameters. The designer must know the following:

$I_{(LED)}$ per string

10.2.4.2.1.1 $R_{(REF)}$

$$R_{(REF)} = V_{ref} \times K_{(I)} / (I_{(LED)} / \text{channel}) = 1.222 \times 100 / (300 / 3) = 1.222\ k\Omega \quad (13)$$

10.2.4.2.1.2 Input and Output Capacitors

TI recommends to add capacitors at VIN and IOUTx. TI recommends an input capacitor of at least 1 µF close to the VIN pin, and output capacitors of 10 nF close to the IOUTx pins. Larger capacitors are helpful for EMC and ESD; however, it takes a longer time to charge up the capacitor and could affect PWM dimming performance.

10.2.5 High-Side PWM Dimming

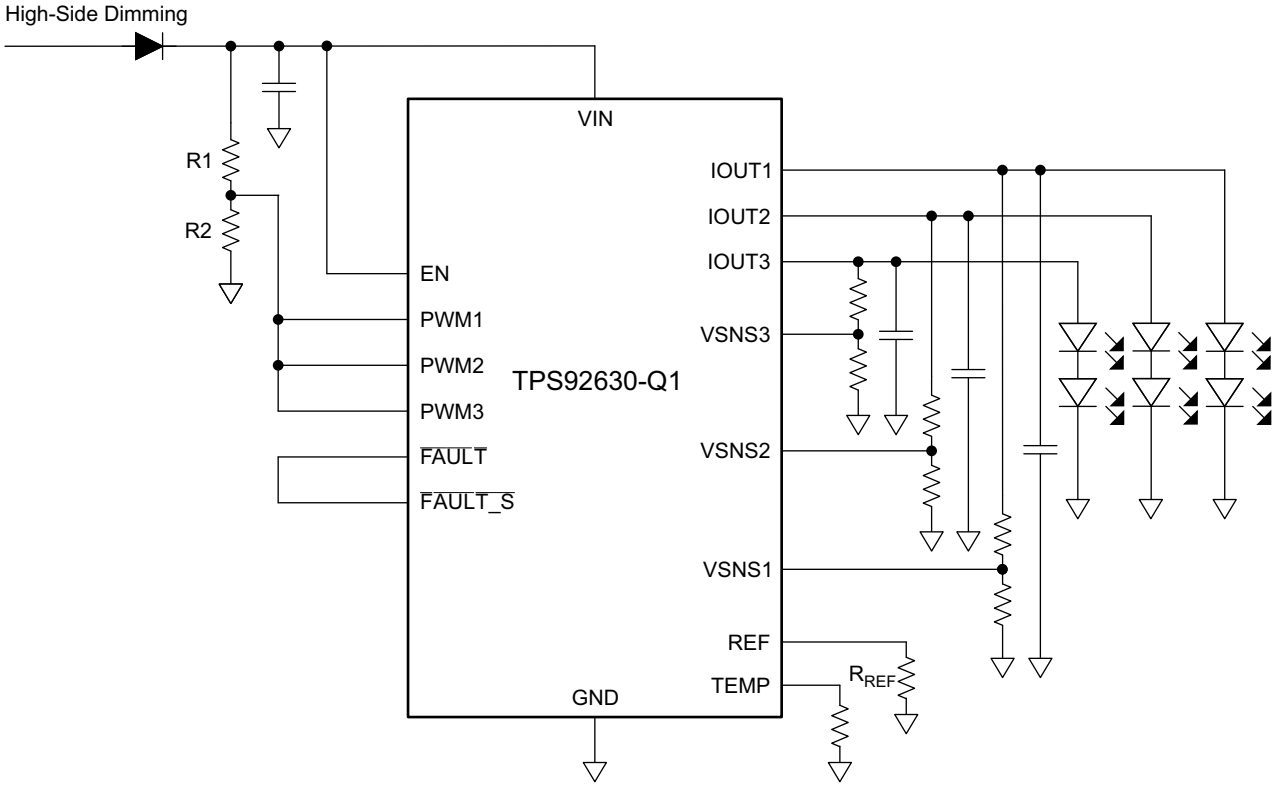


Figure 31. High-Side PWM Dimming

10.2.5.1 Design Requirements

For this design example, use the following as the input parameters.

Table 6. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
$V_{(VIN-low)}$	7 V

10.2.5.2 Detailed Design Procedure

If the system has no MCU or PWM, one can use the high-side driver to do the dimming directly. When using the high-side driver to do PWM dimming, a resistor divider must be put in the PWM pin in case of current overshoot on the PWM rising edge. The resistor divider is needed to turn off the channel before the next PWM rising edge.

10.2.5.2.1 Step-by-Step Design Procedure

To begin the design process, one must decide on a parameter. The designer must know the value for $V_{(VIN-low)}$.

10.2.5.2.1.1 Ratio of Resistors, R1 / R2

First, measure the voltage on the VIN pin when the high-side dimming voltage is at a low level. Then calculate he ratio of R1 / R2 using the formula of Equation 14.

$$\frac{R1}{R2} = \frac{V_{(VIN-low)} + 0.1}{1.178 \times 0.95} \tag{14}$$

Assuming that the measured voltage was 7 V, the R1 / R2 ratio would be 5.25.

10.2.5.2.1.2 R1 and R2 Selection

Select R1 = 105 kΩ and R2 = 20 kΩ.

10.2.5.2.1.3 Input and Output Capacitors

TI recommends to add capacitors at VIN and IOUTx. TI recommends an input capacitor of at least 1 µF close to the VIN pin, and output capacitors of 10 nF close to the IOUTx pins. Larger capacitors are helpful for EMC and ESD; however, it takes a longer time to charge up the capacitor and could affect PWM dimming performance.

11 Power Supply Recommendations

The TPS92630-Q1 device is qualified for automotive applications. The normal power supply connection is therefore to an automobile electrical system that provides a voltage within the range specified in the *Recommended Operating Conditions*.

12 Layout

12.1 Layout Guidelines

In order to prevent thermal shutdown, T_J must be less than 150°C. If the input voltage is very high, the power dissipation might be large. The devices are currently available in the TSSOP-EP package, which has good thermal impedance. However, the PCB layout is also very important. Good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

- Maximize the copper coverage on the PCB to increase the thermal conductivity of the board, because the major heat-flow path from the package to the ambient is through the copper on the PCB. Maximum copper is extremely important when the design does not include heat sinks attached to the PCB on the other side of the package.
- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- All thermal vias should be either plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85 percent.

12.2 Layout Example

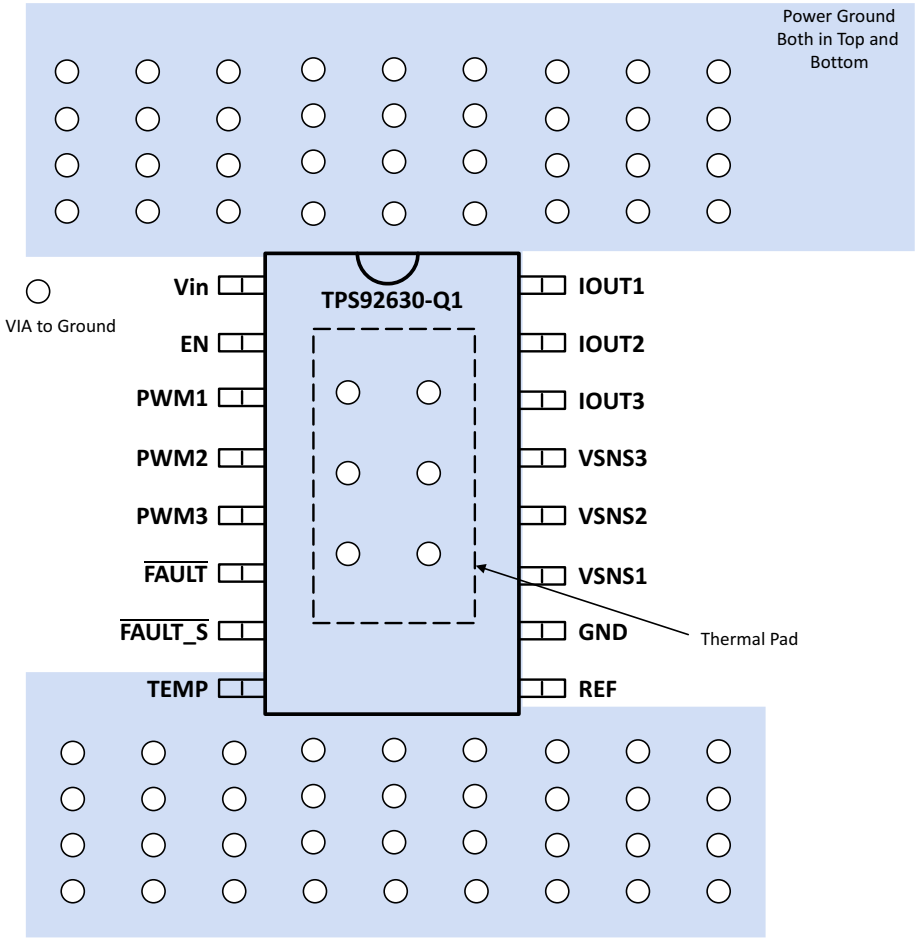


Figure 32. TPS92630-Q1 Board Layout Diagram

13 器件和文档支持

13.1 文档支持

13.1.1 相关文档

请参阅如下相关文档：

- *《如何在汽车外部照明应用中计算 TPS92630-Q1 最大输出 电流》*
- *《适用于基于降压 + 线性 LED 驱动器的系统的 CISPR25 汽车尾灯参考设计》*
- *《适用于基于升压 + 线性 LED 驱动器的系统的 CISPR25 经测试汽车尾灯参考设计》*
- *《适用于汽车照明应用的线性 LED 驱动器参考 设计》*
- *《汽车高侧调光尾灯参考设计》*
- *《汽车尾灯 EMC 参考设计》*

13.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

13.4 商标

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是适用于指定器件的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查看左侧的导航面板。

10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92630QPWPRQ1	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	92630	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

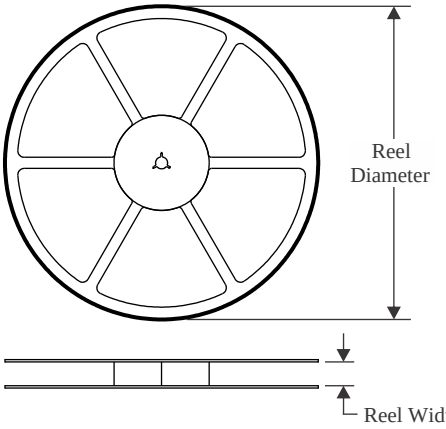
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

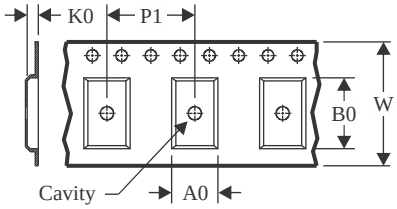
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

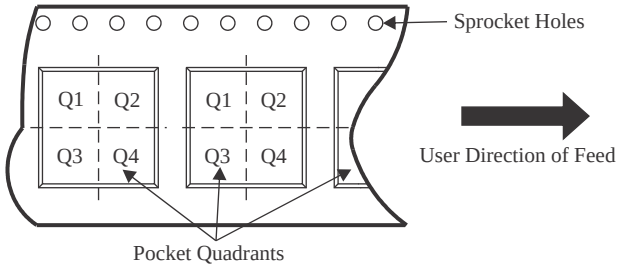


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



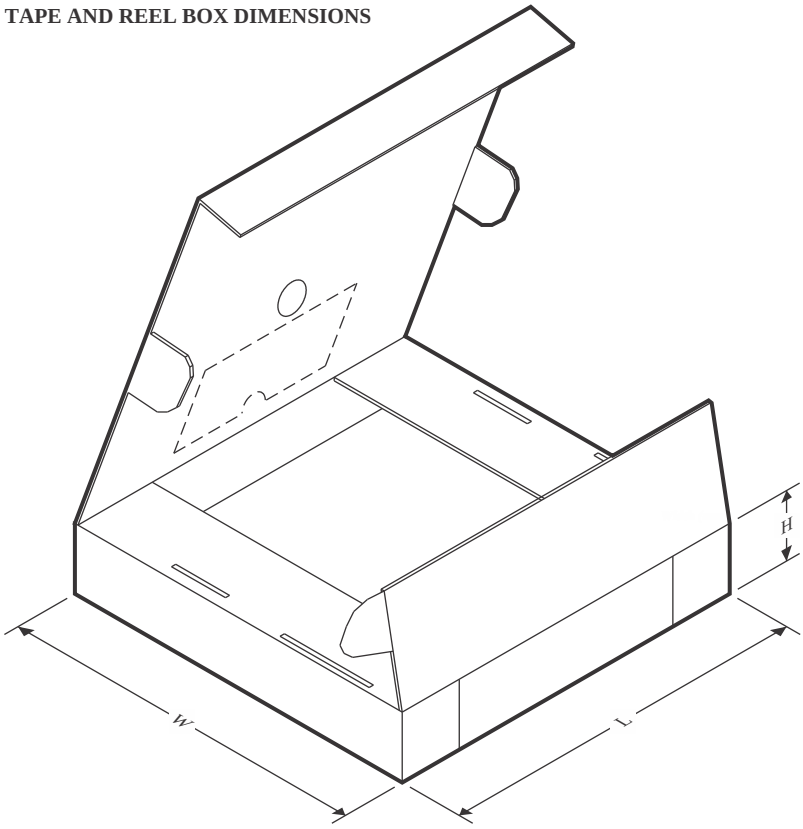
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92630QPWPRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

5-Dec-2023

TAPE AND REEL BOX DIMENSIONS



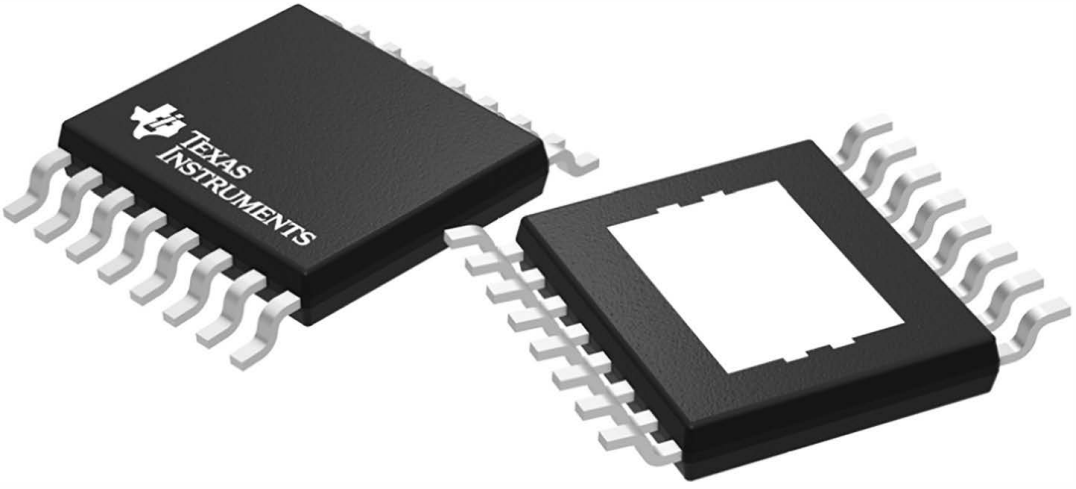
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92630QPWPRQ1	HTSSOP	PWP	16	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

PWP 16 **PowerPAD™ TSSOP - 1.2 mm max height**

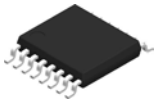
PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

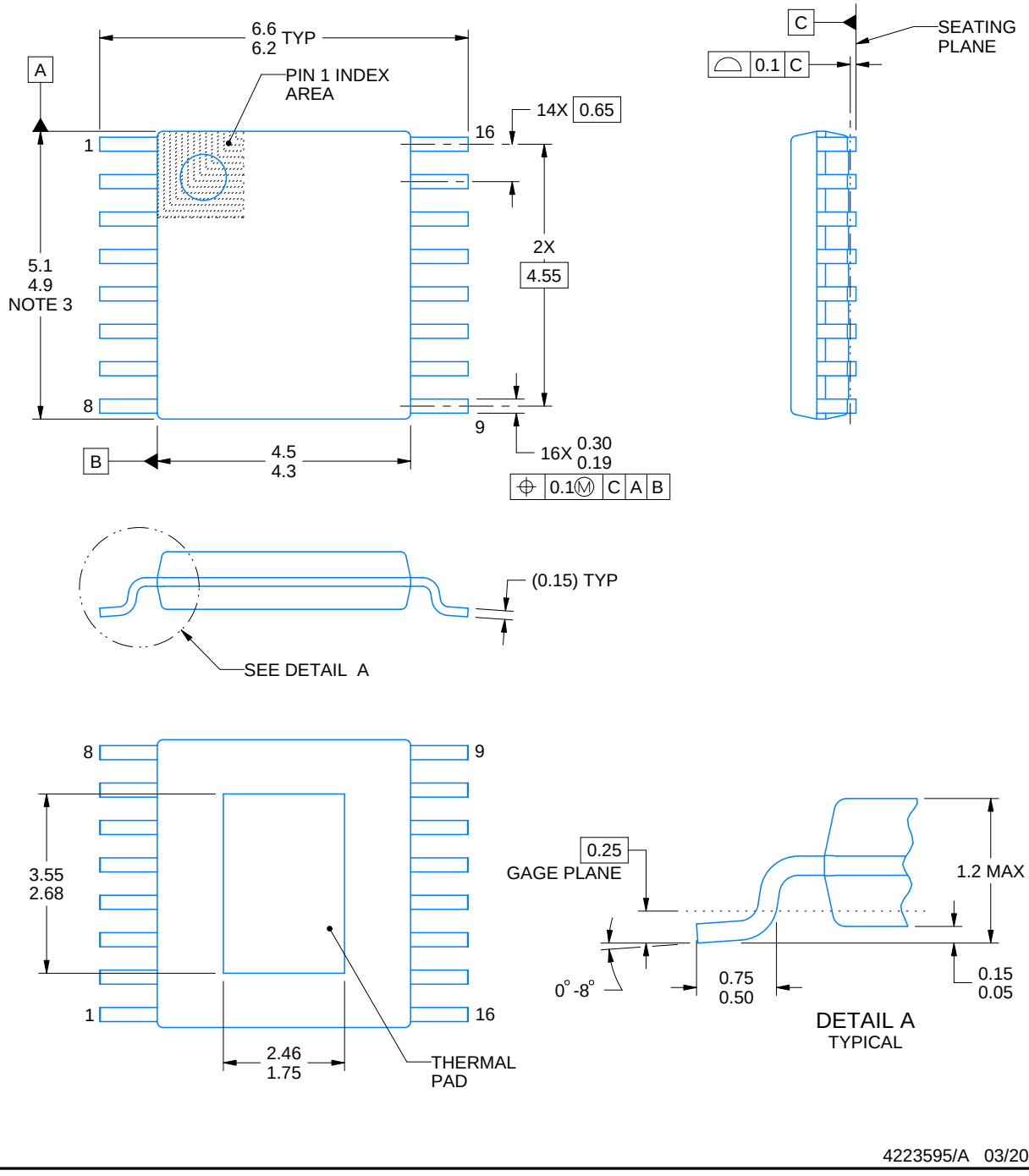
PACKAGE OUTLINE

PWP0016J



PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

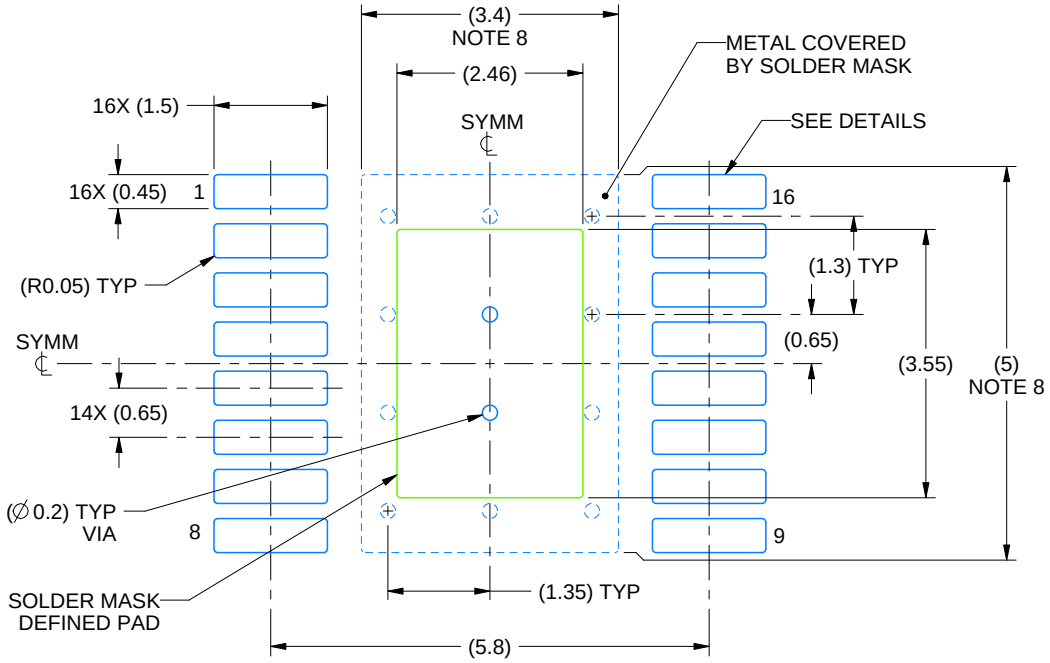
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

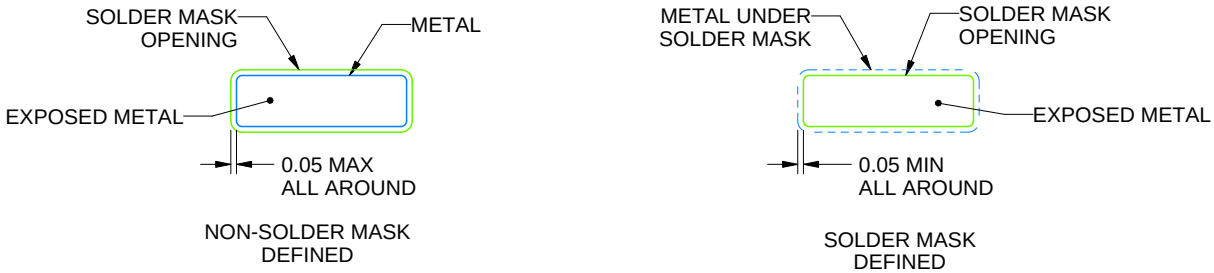
PWP0016J

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4223595/A 03/2017

NOTES: (continued)

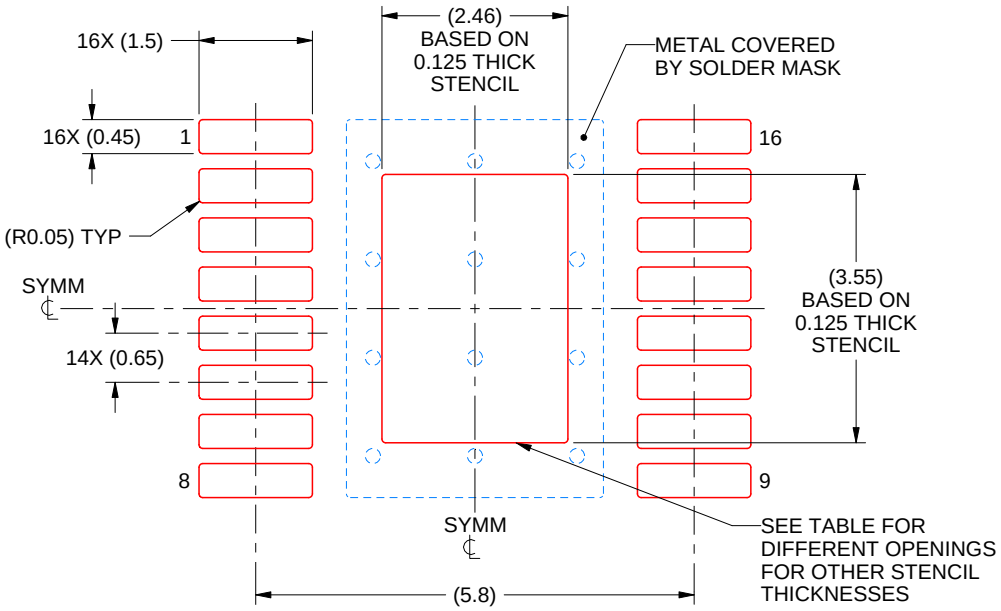
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
8. Size of metal pad may vary due to creepage requirement.
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

PWP0016J

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 3.97
0.125	2.46 X 3.55 (SHOWN)
0.15	2.25 X 3.24
0.175	2.08 X 3.00

4223595/A 03/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.