SGM42408Q
8-Channel Low-side Driver for Automotive Applications

GENERAL DESCRIPTION

The SGM42408Q consists of 8 identical low-side drivers with series protection functions. A number of protection features are provided in the device, including open-load detection, active clamp circuit, over-current protection and thermal shutdown.

The device is AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and it is suitable for automotive applications.

The SGM42408Q is available in a Green TSSOP-24 (Exposed Pad) package.

APPLICATIONS

Driving Resistive, Inductive Load

FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
  Device Temperature Grade 1
  T_A = -40℃ to +125℃
- **8-Channel Low-side Switch for Driving Resistive, Inductive Load**
- **16-Bit SPI for Diagnostics and Control (1)**
- **Output Clamp Voltage: 56V (TYP)**
- **Support SPI Mode or DIR Mode**
- **Current Limit: 1.2A/Channel (TYP)**
- **Active Clamp Energy: 90mJ at T_J = +25℃**
- **On-Resistance: 570mΩ (TYP)**
- **Protection and Features:**
  - **Open-Load Detection (OL)**
  - **Over-Current Protection (OCP)**
  - **Active Clamp Circuit**
  - **Thermal Shutdown (TSD)**
- **Available in a Green TSSOP-24 (Exposed Pad) Package**

代理商 威尔迈 www.viswie.com
联系电话 138 2526 5270

SIMPLIFIED SCHEMATIC

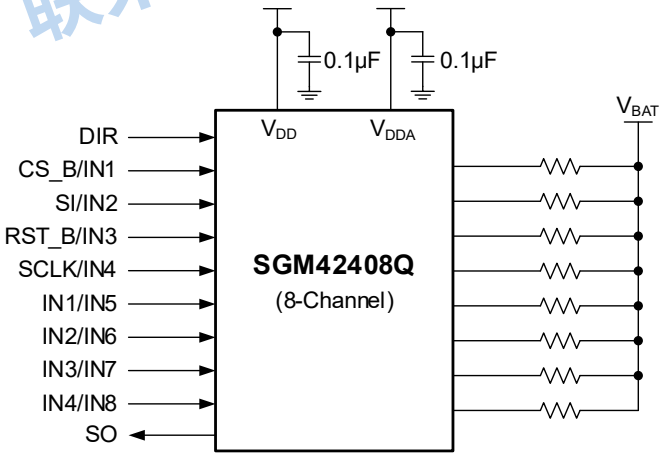


Figure 1. Simplified Schematic

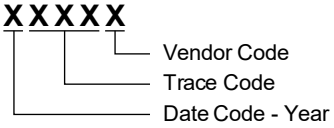
NOTE: 1. SPI control supports the use of multiple devices in parallel, but don't support serial daisy chain.

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM42408Q	TSSOP-24 (Exposed Pad)	-40℃ to +125℃	SGM42408QPTS24G/TR	112PTS24 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} ..... -0.3V to 7V
Output Voltage, V_{DSx} ..... -0.3V to 50V (Internally Limited)
Output Current, I_{Dx} ..... 0.5A (Internally Limited) (1)
Diagnostic Output Voltage, V_{SO} ..... -0.3V to 7V
Input Voltage, V_{INx}, V_{DIR} ..... -0.3V to 7V
Single Pulse Drain-to-Source Avalanche Energy, E_{AS}
$T_{J(0)}$ = +25℃ 90mJ (2)
$T_{J(0)}$ = +150℃ 85mJ (3)
Max Single Pulse Drain-to-Source Avalanche Energy, E_{AS}
$T_{J(0)}$ = +25℃ 130mJ (4)
Package Thermal Resistance
TSSOP-24 (Exposed Pad), θ_{JA} ..... 28.7℃/W
TSSOP-24 (Exposed Pad), θ_{JB} ..... 10℃/W
TSSOP-24 (Exposed Pad), $\theta_{JC\ (TOP)}$ ..... 21.7℃/W
TSSOP-24 (Exposed Pad), $\theta_{JC\ (BOT)}$ ..... 2.1℃/W
Package Thermal Characterization Parameter
TSSOP-24 (Exposed Pad), ψ_{JT} ..... 0.7℃/W
TSSOP-24 (Exposed Pad), ψ_{JB} ..... 9.5℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (5) (6)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. Operating temperature never exceeds T_{JMAX}.
2. Single pulse drain-to-source avalanche energy ($T_{J(0)}$ = +25℃), V_{DD} = 32V, V_{INx} = 5V, I_{PK} = 0.5A, L = 300mH.
3. Single pulse drain-to-source avalanche energy ($T_{J(0)}$ = +150℃), V_{DD} = 32V, V_{INx} = 5V, I_{PK} = 0.5A, L = 300mH.
4. Max single pulse drain-to-source avalanche energy ($T_{J(0)}$ = +25℃), V_{DD} = 32V, V_{INx} = 5V, I_{PK} = 0.76A, L = 300mH.
5. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
6. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Operating Voltage (1)
Digital Part, V_{DD} ..... 3V to 5.5V
Analog Part, V_{DDA} ..... 4V to 5.5V

NOTE: 1. Keep 9 input pins (INx, DIR, SCLK, RST_B, SI, CS_B) voltage level following V_{DD} supply voltage level.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

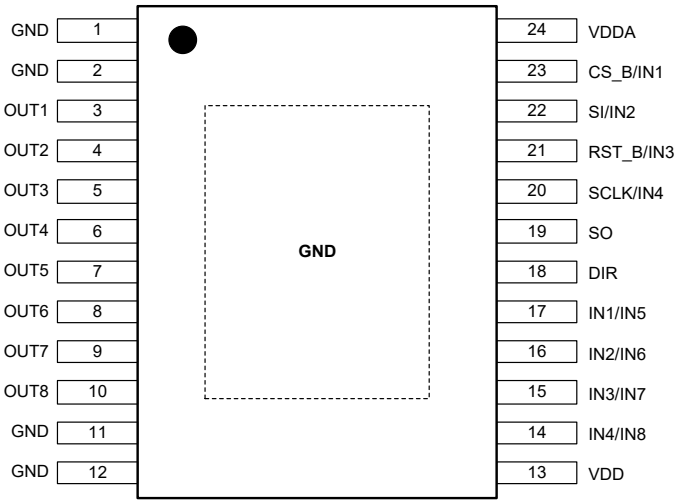
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

SGM42408Q (TOP VIEW)



TSSOP-24 (Exposed Pad)

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	GND	-	Ground.
2	GND	-	Ground.
3	OUT1	O	Output 1 of the device.
4	OUT2	O	Output 2 of the device.
5	OUT3	O	Output 3 of the device.
6	OUT4	O	Output 4 of the device.
7	OUT5	O	Output 5 of the device.
8	OUT6	O	Output 6 of the device.
9	OUT7	O	Output 7 of the device.
10	OUT8	O	Output 8 of the device.
11	GND	-	Ground.
12	GND	-	Ground.
13	VDD	-	Digital Power Supply.
14	IN4/IN8	I	Channel 4 and 8 Input (DIR = L)/Channel 8 Input (DIR = H), Internal Pull-Down.
15	IN3/IN7	I	Channel 3 and 7 Input (DIR = L)/Channel 7 Input (DIR = H), Internal Pull-Down.
16	IN2/IN6	I	Channel 2 and 6 Input (DIR = L)/Channel 6 Input (DIR = H), Internal Pull-Down.
17	IN1/IN5	I	Channel 1 and 5 Input (DIR = L)/Channel 5 Input (DIR = H), Internal Pull-Down.
18	DIR	I	DIR = L, SPI Mode. DIR = H, DIR mode.
19	SO	O	Serial Data Output.
20	SCLK/IN4	I	Serial Clock (DIR = L)/Channel 4 Input (DIR = H), Internal Pull-Down.
21	RST_B/IN3	I	Reset Pin (DIR = L)/Channel 3 Input (DIR = H), Internal Pull-Down.
22	SI/IN2	I	Serial Data Input (DIR = L)/Channel 2 Input (DIR = H), Internal Pull-Down.
23	CS_B/IN1	I	SPI Enable Input (DIR = L)/Channel 1 Input (DIR = H). Pull up at DIR = L setting, pull down at DIR = H.
24	VDDA	-	Analog Power Supply.
Exposed Pad	GND	-	Ground.

NOTE: I = input, O = output.

ELECTRICAL CHARACTERISTICS

(V_{DDA} = V_{DD} = 5V, T_J = -40℃ to +150℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supplies (VDD, VDDA)						
VDDA Standby Current	I_{DDAS}	All output on standby mode, V_{DDA} = V_{DD} = V_{CS_B} = 5V, V_{RST_B} = 0V		0	2	μA
VDD Standby Current	I_{DDS}	All output on standby mode, V_{DDA} = V_{DD} = V_{CS_B} = 5V, V_{RST_B} = 0V		0	1	μA
VDDA Operating Current	I_{DDA}	V_{DDA} = V_{DD} = 5V		1	2	mA
VDD Operating Current	I_{DD}	V_{DDA} = V_{DD} = 5V		5.6	12	μA
VDDA Power-On Reset Threshold Voltage	V_{PORA}	Rising			4	V
VDD Power-On Reset Threshold Voltage	V_{POR}	Rising			2.7	V
Input Pins						
Low-Level Input Voltage	V_{INL}		0		V_{DD} × 0.2	V
High-Level Input Voltage	V_{INH}		V_{DD} × 0.7		V_{DD}	V
Input Hysteresis	V_{HYS}			0.345		V
Low-Level Input Current 1 (RST_B, DIR, IN1 to IN4, SCLK, SI)	I_{INL1}	V_{RST_B}, V_{DIR}, V_{IN1} to V_{IN4}, V_{SCLK}, V_{SI} = 0V	-1	0	1	μA
Low-Level Input Current 2 (CS_B)	I_{INL2}	V_{CS_B} = 0V, V_{DIR} = 0V	-100	-50	-25	μA
Low-Level Input Current 3 (CS_B)	I_{INL3}	V_{CS_B} = 0V, V_{DIR} = 5V	-1	0	1	μA
High-Level Input Current 1 (RST_B, DIR, IN1 to IN4, SCLK, SI)	I_{INH1}	V_{RST_B}, V_{DIR}, V_{IN1} to V_{IN4}, V_{SCLK}, V_{SI} = 5V	25	50	100	μA
High-Level Input Current 2 (CS_B)	I_{INH2}	V_{CS_B} = 5V, V_{DIR} = 0V	-1	0	1	μA
High-Level Input Current 3 (CS_B)	I_{INH3}	V_{CS_B} = 5V, V_{DIR} = 5V	25	50	100	μA
Power MOSFET Output						
Output On-Resistance	R_{DSON}	V_{DD} = V_{DDA} = 5V, I_{Dx} (1) = 0.2A, T_J = +25℃		0.57	0.7	Ω
		V_{DD} = V_{DDA} = 5V, I_{Dx} (1) = 0.2A, T_J = +150℃		1	1.2	Ω
Output Leakage Current	I_{L_OFF}	V_{DS} = 30V, V_{DIR} = 0V, T_J = +25℃		0	1	μA
		V_{DS} = 30V, V_{DIR} = 0V, T_J = +150℃		1	4	μA
Output Leakage Current (Open-Load Detected)	I_{OL}	V_{DS} =40V, V_{DIR} = 5V	25	42	60	μA
Switching Time	t_{ON}	V_{DD} = 5V, V_{INx} (1) = 0V/5V, R_L = 60Ω, V_{BAT} = 12V, V_{DIR} = 5V		16	40	μs
	t_{OFF}	V_{DD} = 5V, V_{INx} (1) = 0V/5V, R_L = 60Ω, V_{BAT} = 12V, V_{DIR} = 5V		30	50	μs
Slew Rate On	dV/dt_{ON}	V_{DD} = 5V, V_{INx} (1) = 0V/5V, R_L = 60Ω, V_{BAT} = 12V, V_{DIR} = 5V, 80% to 20% of V_{BAT}	0.3	1	2	V/μs
Slew Rate Off	$-dV/dt_{OFF}$	V_{DD} = 5V, V_{INx} (1) = 0V/5V, R_L = 60Ω, V_{BAT} = 12V, V_{DIR} = 5V, 20% to 80% of V_{BAT}	0.3	1	2	V/μs
PWM Output Range	f_{PWM}	V_{DD} = 5V, V_{INx} (1) = 0V/5V, R_L = 60Ω, V_{DIR} = 5V, V_{BAT} = 12V			5	kHz
Output Clamp Voltage	V_{CL}	I_{Dx} (1) = 1mA (output off-state)	49	56	63	V
Serial Output (SO)						
Low-Level Output Voltage	V_{SOL}	I_{SO} = 1mA		0.25	0.6	V
High-Level Output Voltage	V_{SOH}	I_{SO} = -1mA	V_{DD} - 0.6	V_{DD} - 0.3		V
Serial Out Output Leak Current	I_{SO_OFF}		-1	0	1	μA
Protection						
Over-Current Detection Current	I_{OCP_ON}		0.5	1.2	2	A
Over-Current Detection Time	t_{OCP}		400	1000	2000	μs
Open-Load Release Voltage	V_{OLD_OFF}		1.6	2.6	3.6	V
Open-Load Detection Voltage	V_{OLD_ON}	V_{INx} (1) = 0V, V_{DIR} = 5V	1.1	2.1	3.1	V
Open-Load Detection Time	t_{OLD}		50	150	300	μs
TSD Detection Temperature (2)	T_{JD}			175		℃

NOTES:

1. “x” shows the channel number.

2. Not 100% tested.

DEFINITION

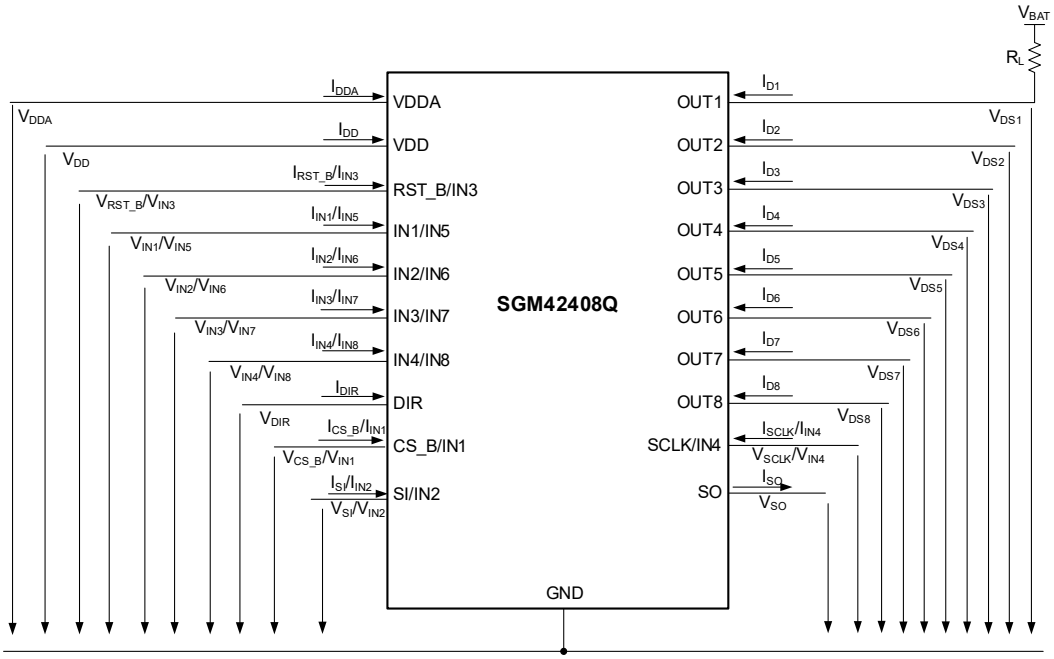


Figure 2. Definition

TEST CIRCUITS

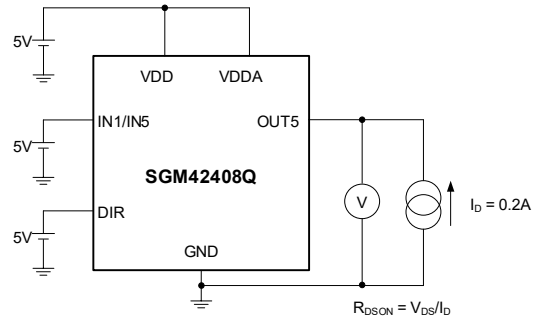


Figure 3. Output On-Resistance

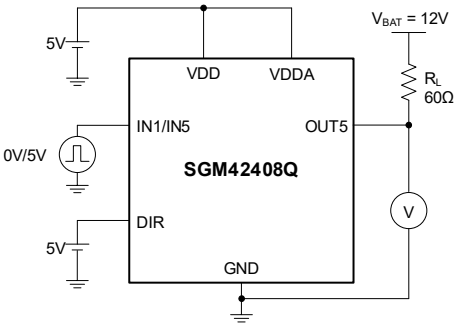


Figure 4. Switching Time

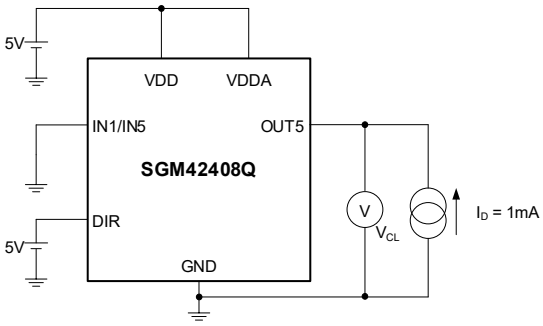


Figure 5. Output Clamp Voltage

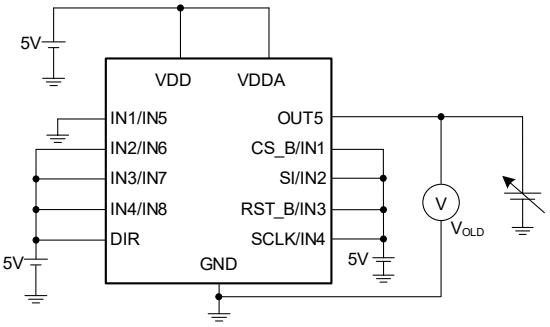


Figure 6. Open Detection

SWITCHING CHARACTERISTICS

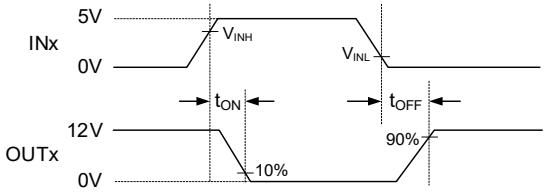


Figure 7. Switching Time

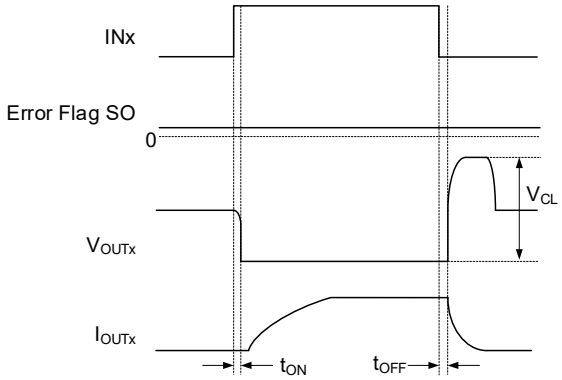


Figure 8. Timing Chart with Inductive Load

POWER SOURCE ON/OFF SEQUENCE

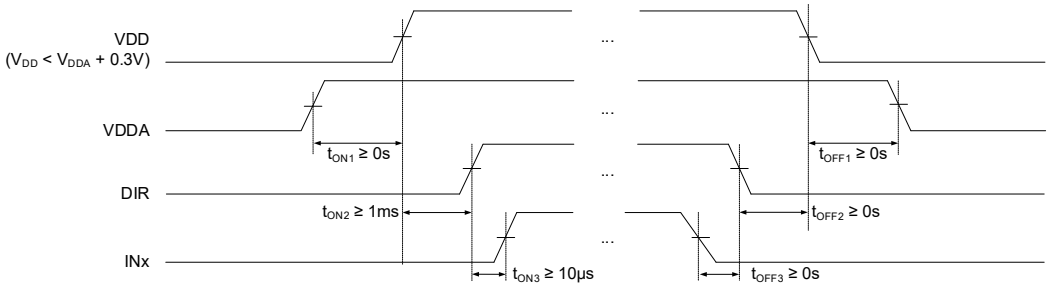


Figure 9. Power Source On/Off Sequence (DIR Mode)

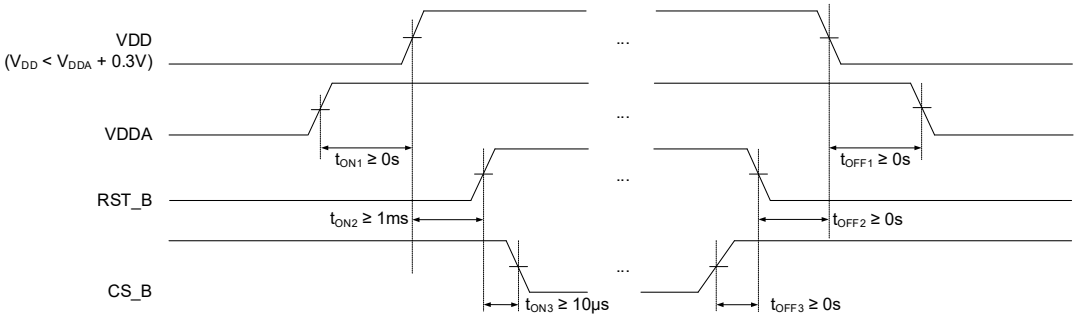


Figure 10. Power Source On/Off Sequence (SPI Mode)

TRUTH TABLE

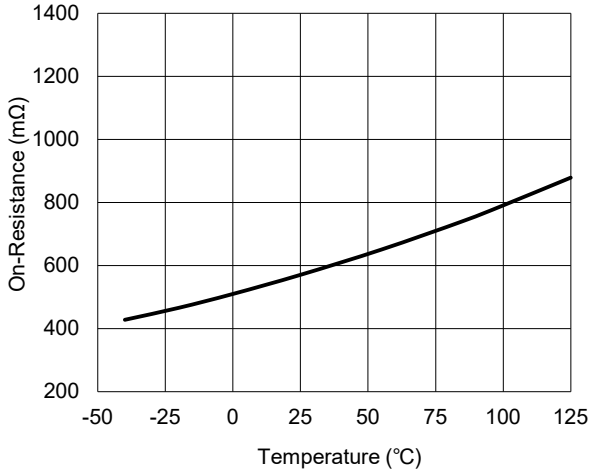
Table 1. DIR (Direct) Mode Diagnostic Output Truth Table

INx	Mode	T_{SD}	Output		V_{SO}	Output State
			V_{OUTx}	I_{OUTx}		
H	Normal	Off	-	I_{Dx} < 0.5A (MIN)	L	On
	Over-Current Detection			I_{Dx} ≥ 0.5A (MIN) to 2A	H	Off
	Thermal Shutdown	On	-	-	H	Off
L	Normal	-	V_{DSx} > 3V	-	L	Off
	Open-Load Detection		V_{DSx} ≤ 1V to 3V	-	H	Off

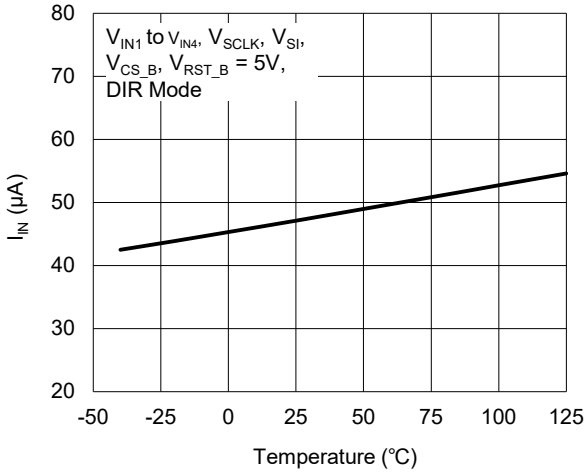
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, unless otherwise noted.

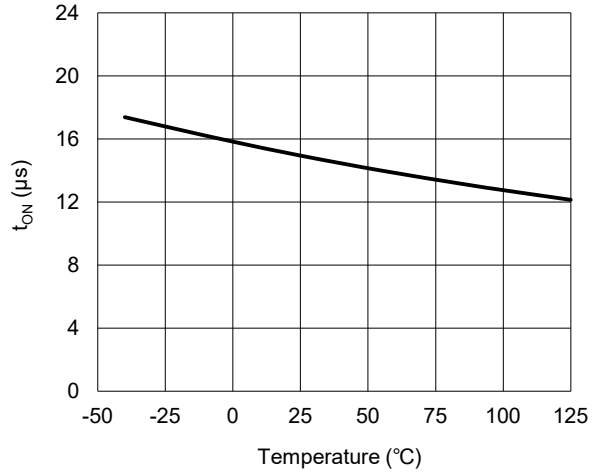
On-Resistance vs. Temperature



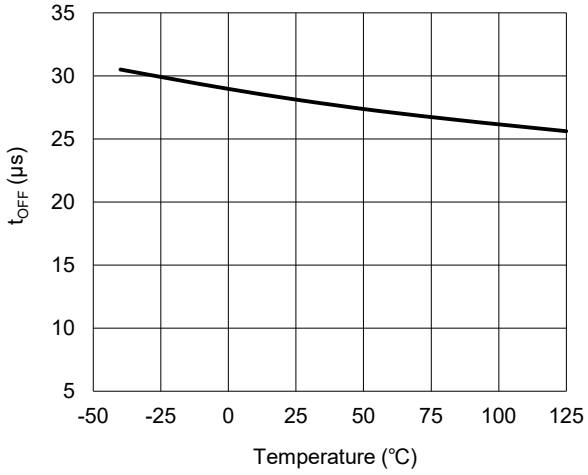
I_{IN} vs. Temperature



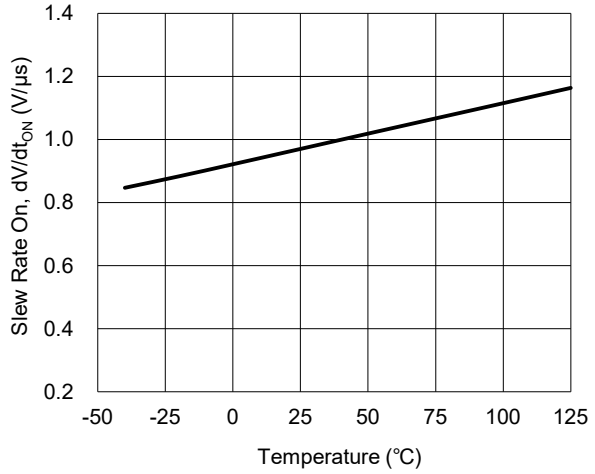
t_{ON} vs. Temperature



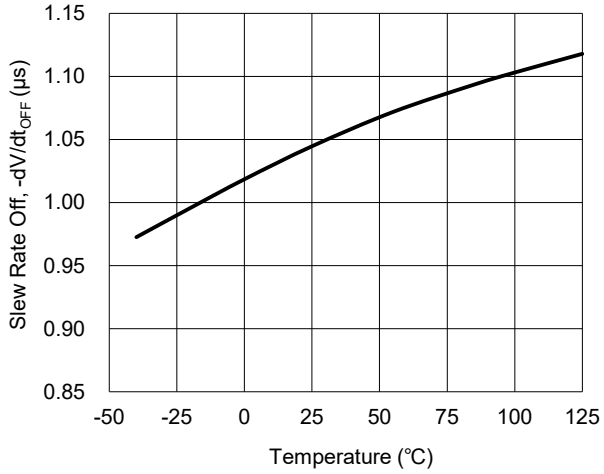
t_{OFF} vs. Temperature



Slew Rate On vs. Temperature



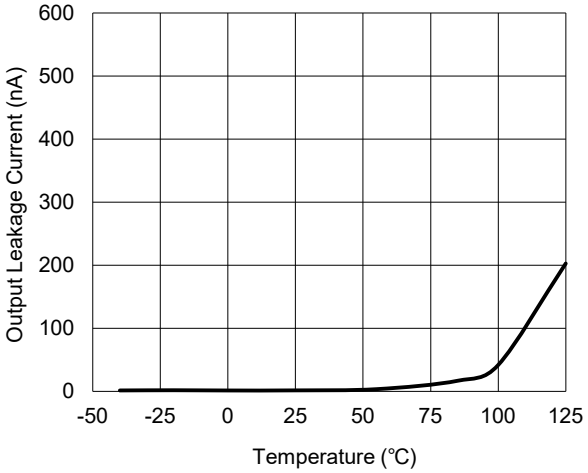
Slew Rate Off vs. Temperature



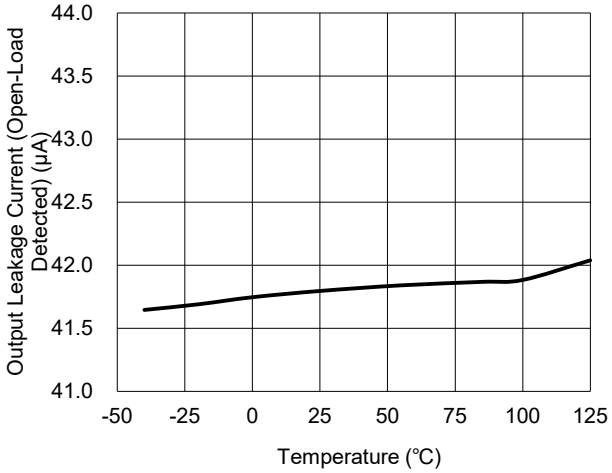
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

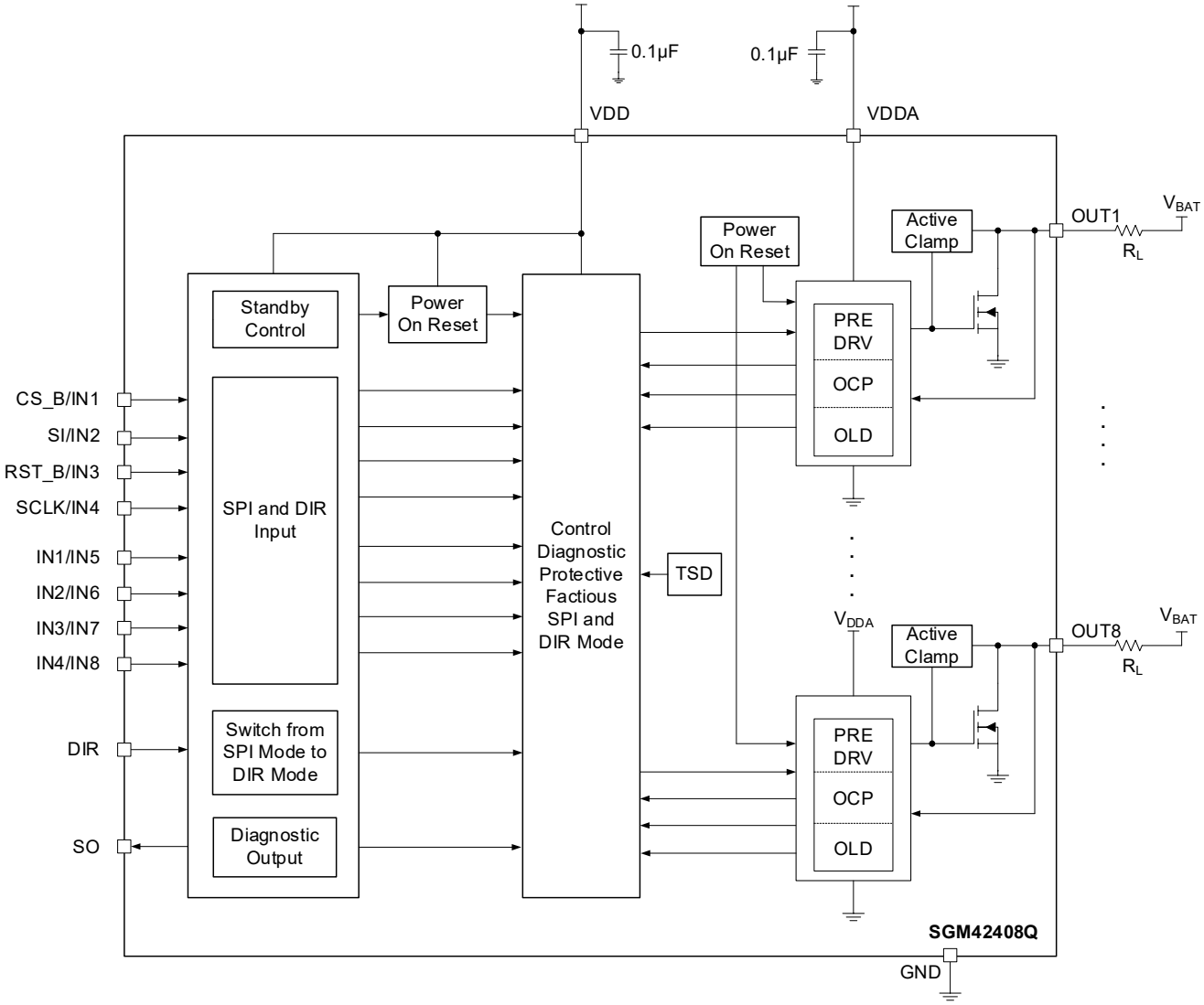
Output Leakage Current vs. Temperature



Output Leakage Current (Open-Load Detected) vs. Temperature



FUNCTIONAL BLOCK DIAGRAM



NOTE: Keep 9 input pins (INx, DIR, SCLK, RST_B, SI, CS_B) voltage level following V_{DD} supply voltage level.

SPI MODE

If DIR is low and RST_B is high, the device is under SPI mode. When CS_B is high, SO terminal output state is Hi-Z. If CS_B is turned to low, diagnostics and protections state (OLD, OCP, TSD) are latched at falling edge of CS_B, and SO terminal output state is latched at rising edge of SCLK. SI terminal is written in register at falling edge of SCLK. Output corresponding to the input of each channel is controlled at rising edge of CS_B.

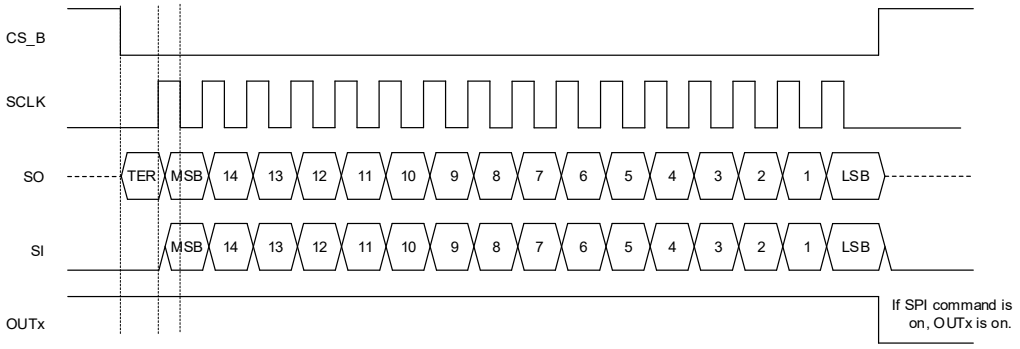


Figure 11. SPI Mode

SI Signals

Initial State: 0000h

Bit[15:14]	Bit[13:12]	Bit[11:10]	Bit[9:8]	Bit[7:6]	Bit[5:4]	Bit[3:2]	Bit[1:0]
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1

Bits	CHx	Output and Protection Circuit Status			
		Output	OCP	TSD	OLD
[15:14], [13:12], [11:10], [9:8], [7:6], [5:4], [3:2], [1:0]	00	Off	Disable	Disable	Disable
	01	On/Off (1)	Enable/Disable	Enable/Disable	Disable/Enable
	10	On	Enable	Enable	Disable
	11	Off	Disable	Disable	Enable

NOTE: 1. When CHx = 01, CHx output enable is controlled by IN1/IN5, IN2/IN6, IN3/IN7 and IN4/IN8.

Table 2. Output Controlled by Each Input

Input	Controlled Output
IN1/IN5	OUT1
IN2/IN6	OUT2
IN3/IN7	OUT3
IN4/IN8	OUT4
IN1/IN5	OUT5
IN2/IN6	OUT6
IN3/IN7	OUT7
IN4/IN8	OUT8

SPI MODE (continued)

SO Signals

CS_B = high, SO terminal state output is Hi-Z.
CS_B = low, the following table corresponds to the different state bits.

Bit[16]	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
TER	OL8	D8	OL7	D7	OL6	D6	OL5	D5	OL4	D4	OL3	D3	OL2	D2	OL1	D1
	OUT8		OUT7		OUT6		OUT5		OUT4		OUT3		OUT2		OUT1	

Field	Bits	Data	State
TER	[16] (1)	0	Correspondence just after reset and normal operation.
		1	Correspondence error of last time.
OLx (x = 8 to1)	[15], [13], [11], [9], [7], [5], [3], [1]	0	Normal operation.
		1	Load open.
Dx (x = 8 to1)	[14], [12], [10], [8], [6], [4], [2], [0]	0	Normal operation.
		1	OCD or TSD.

NOTE: 1. The signal output logic for the TER bit is as follows.

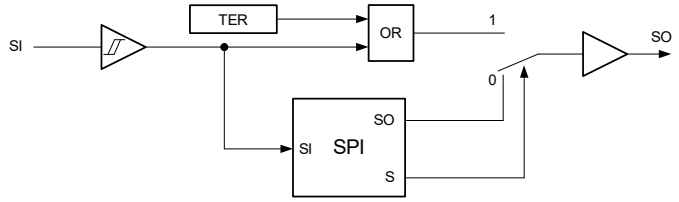


Figure 12. Block Diagram

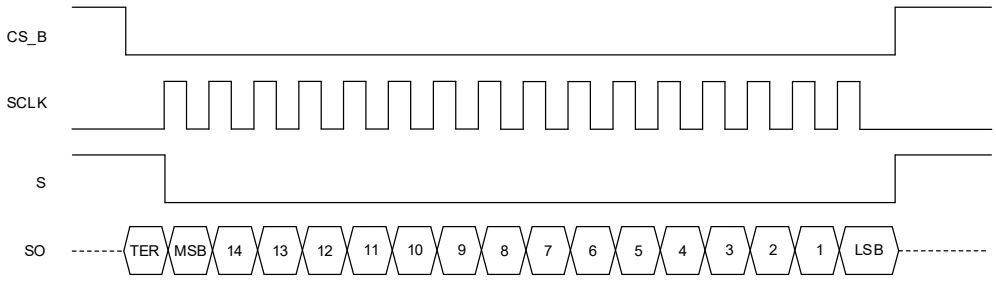


Figure 13. SO Timing

Generate an "S" signal within the device. And switch the output to choose whether the output TER signal or the output SPI data output (OLx, Dx) signals.

SPI MODE (continued)

Parallel Connection

Support the use of multiple devices in parallel, as shown in Figure 14. The SI/SO/SCLK signals are connected in parallel to the common signal. The CS_Bx signal for each device needs to be supplied independently.

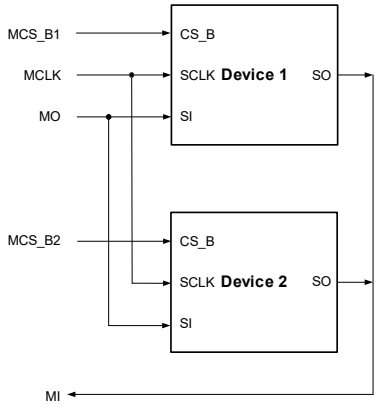


Figure 14. Parallel Connection

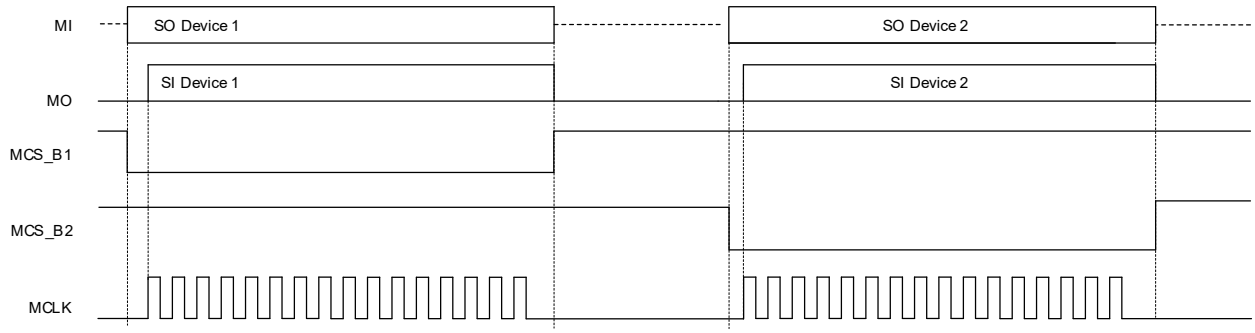


Figure 15. Timing Chart when 2 Devices are Connected

SPI RST_B Releasing Sequence

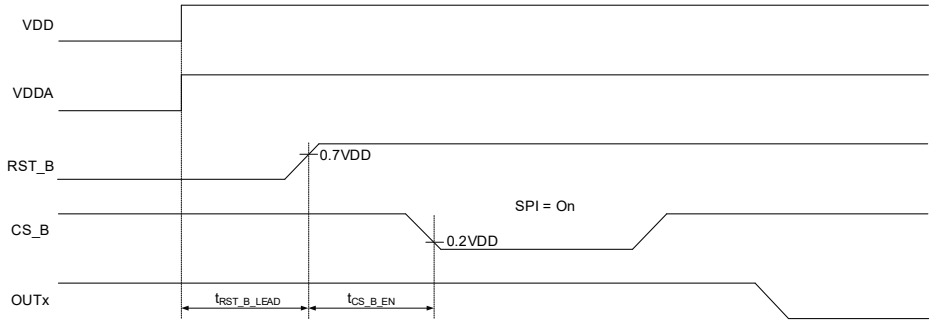


Figure 16. RST_B Releasing Sequence

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
RST_B Lead Time (1) (2)	$t_{RST_B_LEAD}$	1			ms
CS_B Enable Time (1)	$t_{CS_B_EN}$	10			μs

NOTES:
1. Not 100% tested.
2. Low time and high time of the RST_B must be over 10μs.

SPI MODE (continued)

SPI Timing Chart

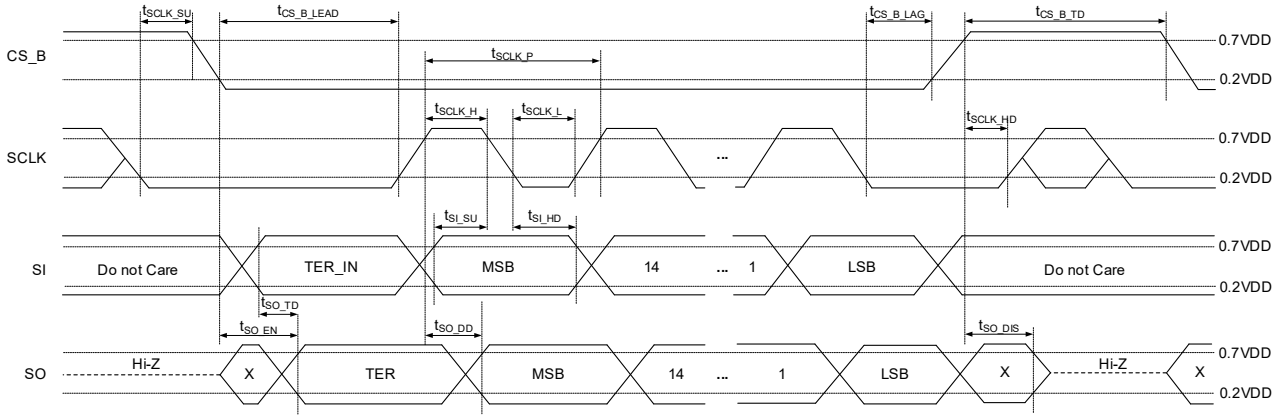


Figure 17. SPI Timing Chart

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SCLK Frequency	f_{SCLK}	0		5	MHz
SCLK Cycle Length	t_{SCLK_P}	200			ns
SCLK High Time	t_{SCLK_H}	50			ns
SCLK Low Time	t_{SCLK_L}	50			ns
SCLK Setup Time	t_{SCLK_SU}	50			ns
SCLK Hold Time	t_{SCLK_HD}	50			ns
CS_B Lead Time	$t_{CS_B_LEAD}$	250			ns
CS_B Lag Time	$t_{CS_B_LAG}$	250			ns
Transfer Delay Time	$t_{CS_B_TD}$	250			ns
Data Setup Time	t_{SI_SU}	20			ns
Data Hold Time	t_{SI_HD}	45			ns
SPI Output Enable Time (1)	t_{SO_EN}			200	ns
SPI Output Disable Time (1)	t_{SO_DIS}			250	ns
SPI Output Data Delay Time (1) (2)	t_{SO_DD}			100	ns
ERR Output Through Delay Time (1)	t_{SO_TD}			200	ns

NOTES:
1. Not 100% tested.
2. C_{SO} = 10pF, 3.0V ≤ V_{DD} ≤ 5.5V.

DIR MODE

DIR (Direct) Mode

If DIR is high, DIR mode is selected, as shown in the table below for input/output control correspondence. In DIR mode, the SPI signal and the RST_B signal are invalid.

Input Pin	Controlled Output
CS_B/IN1	OUT1
SI/IN2	OUT2
RST_B/IN3	OUT3
SCLK/IN4	OUT4
IN1/IN5	OUT5
IN2/IN6	OUT6
IN3/IN7	OUT7
IN4/IN8	OUT8

DIR (Direct) Mode Timing Chart

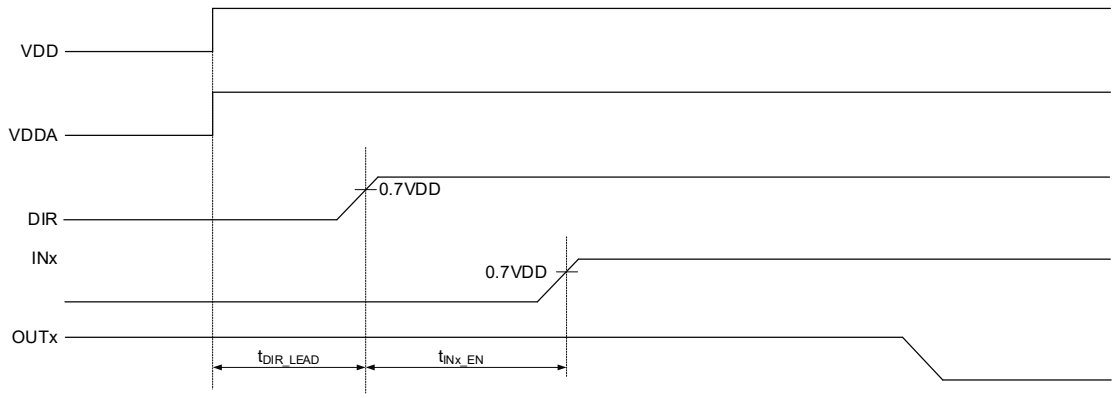


Figure 18. DIR Mode Timing (a)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
DIR Lead Time (1)	t_{DIR_LEAD}	1			ms
INx Enable Time (1)	t_{INx_EN}	10			μs

NOTE: 1. Not 100% tested.

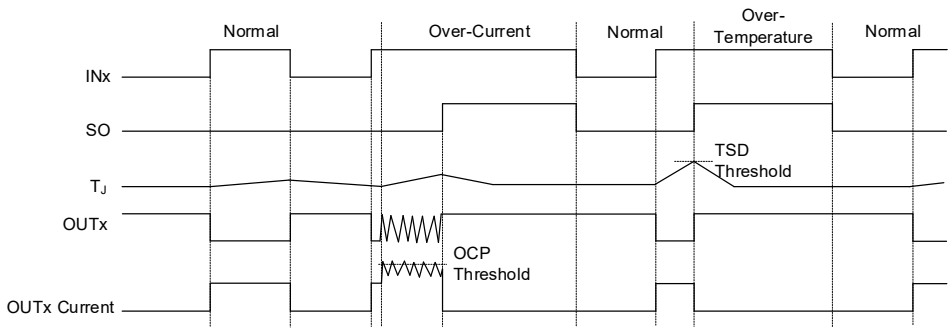


Figure 19. DIR Mode Timing (b)

DIR MODE (continued)

The transition of the operating current I_{DDA} + I_{DD} in direct mode is shown in Figure 20.

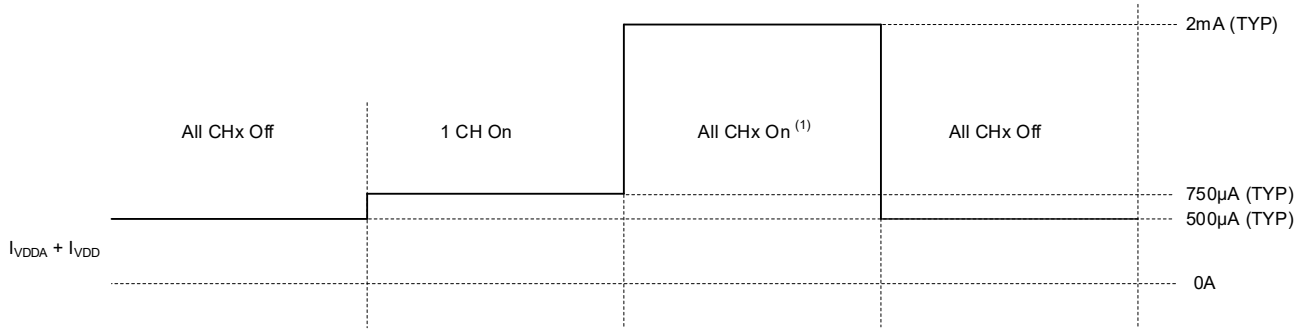


Figure 20. Operation Current State Transition Diagram

NOTE: 1. Sum of VDDA and VDD operation current (when all outputs are on).

DETAILED DESCRIPTION

Over-Current Protection

When I_{OUTx} exceeds 1.2A (TYP) and maintains 1000μs, the error state is output through the SO terminal, and the SO terminal error flag is released only when the OUTENx (1) changes from high to low (2).

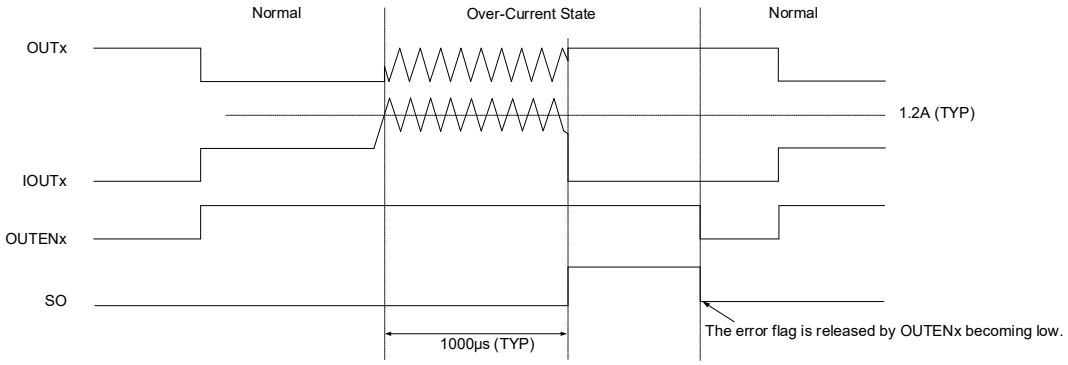


Figure 21. Over-Current Protection Timing

NOTES:

1. OUTENx shows the on/off enable signal of the OUTx terminals.
2. When the OUTENx becomes low before the over-current detection time (TYP: 1000μs, MAX: 2000μs), the SO terminal does not output an error flag, and the over-current detection latch timer is cleared.

Overheat Protection

When the temperature of any channel reaches or exceeds +175℃ and lasts 30μs, the corresponding channel output is turned off, and the error signal is output by the SO terminal, and the error flag is released only when OUTENx (3) becomes low (4).

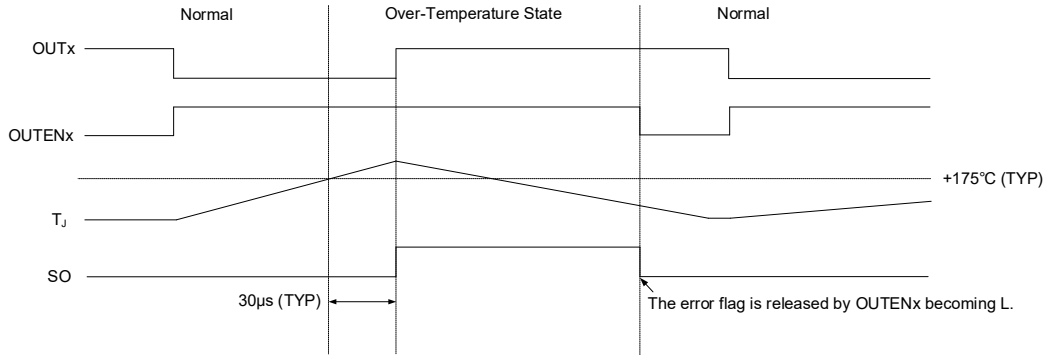


Figure 22. Overheat Protection Timing

NOTES:

3. OUTENx shows the on/off enable signal of the OUTx terminals.
4. When the OUTENx becomes low before the overheat detection time (TYP: 30μs, MAX: 65μs), the SO terminal does not output an error flag, and the overheat detection latch timer is cleared.

DETAILED DESCRIPTION (continued)

Open Detection

Under the condition of enabling open-load detection (1), when the voltage of any channel drops below 1.5V (TYP), the SO terminal outputs an error flag.

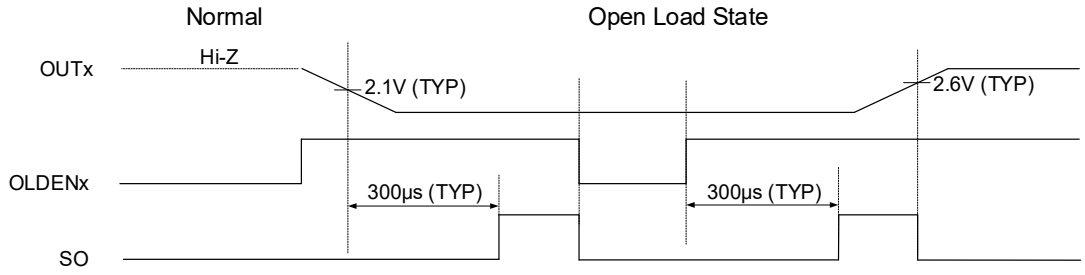


Figure 23. Open Detection Protection Timing

NOTE: 1. In DIR mode, the open-load detection function is enabled when the channel is in the off-state (OUTENx = low). In SPI mode, please refer to the previous table.

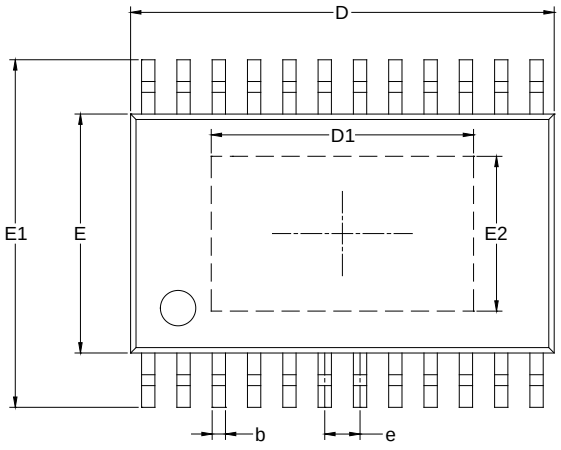
REVISION HISTORY

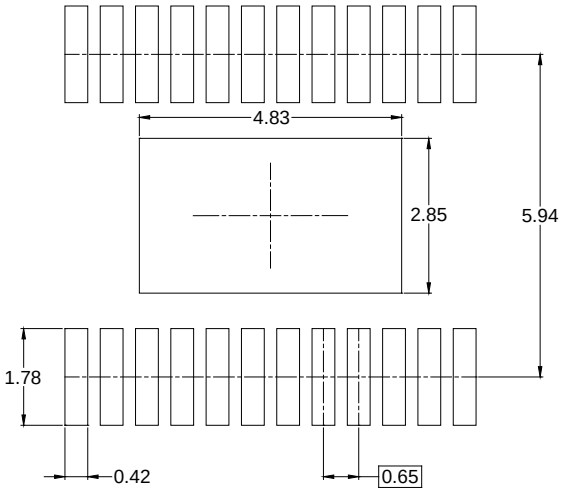
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (DECEMBER 2025)	Page
Changed from product preview to production data	All

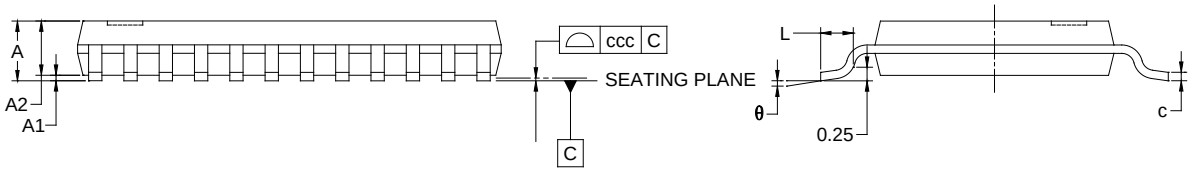
PACKAGE OUTLINE DIMENSIONS

TSSOP-24 (Exposed Pad)





RECOMMENDED LAND PATTERN (Unit: mm)

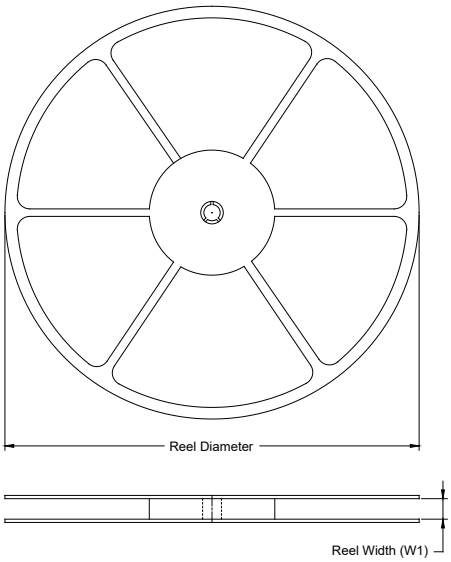


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	1.000 REF		
b	0.190	-	0.300
c	0.090	-	0.200
D	7.700	-	7.900
D1	4.630	-	5.030
E	4.300	-	4.500
E1	6.200	-	6.600
E2	2.650	-	3.050
e	0.650 BSC		
L	0.450	-	0.750
θ	0°	-	8°
ccc	0.100		

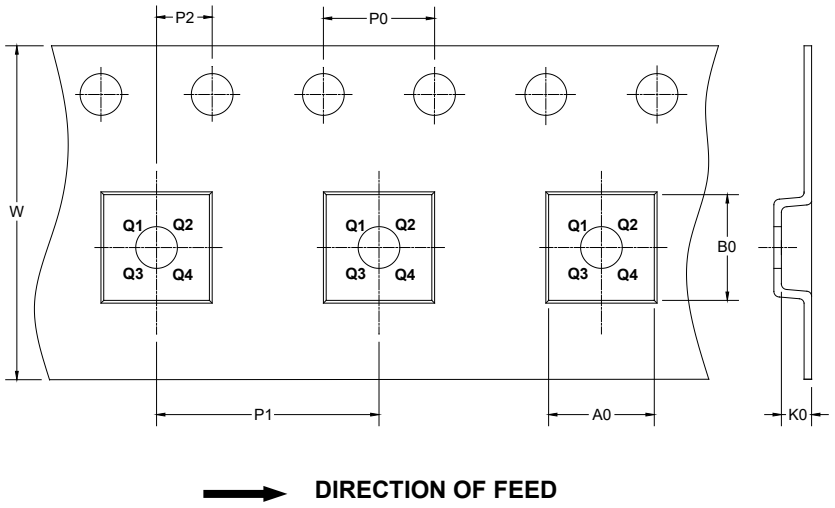
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



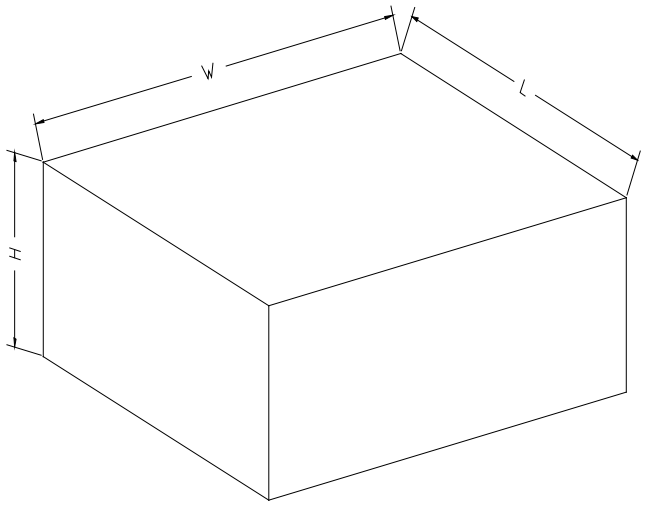
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-24 (Exposed Pad)	13"	16.4	6.80	8.30	1.60	4.0	8.0	2.0	16.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002