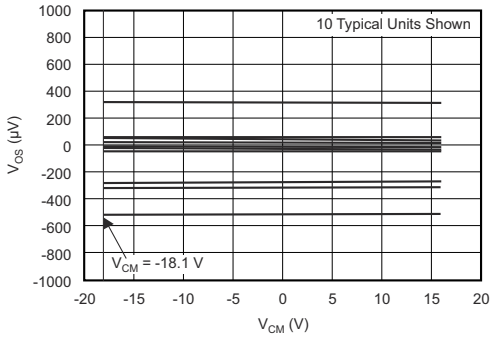
OPAx171-Q1 36-V, Single-Supply, General-Purpose Operational Amplifier

1 Features

- Qualified for automotive applications
- AEC-Q100 test guidance with the following results:
  - Temperature grade 1: –40°C to +125°C ambient operating temperature
  - Device HBM ESD classification level:
    - Level 3A for OPA171-Q1
    - Level 2 for OPA4171-Q1
  - Device CDM ESD classification level
    - Level C4A for OPA171-Q1 TLV171-Q1
    - Level C6 for OPA2171-Q1
    - Level C6 for OPA4171-Q1
- Supply range:
  - Single-supply: 2.7 V to 36 V
  - Dual-supply ±1.35 V to ±18 V
- Low noise: 14 nV/√Hz at 1 kHz
- Low offset drift: ±0.3 µV/°C (typical)
- Input range includes negative supply
- Input range operates to positive supply with reduced performance
- Rail-to-rail output
- Gain bandwidth: 3 MHz
- Low quiescent current: 475 µA per amplifier
- High Common-mode rejection: 120 dB (typical)
- Low input bias current: 10 pA
- Industry-Standard Package:
  - 5-Pin Small-Outline Transistor SOT-23 (DBV) Package



Offset Voltage vs Common-Mode Voltage: V_{SUPPLY} = ±18 V

2 Applications

- Tracking amplifier in power modules
- Merchant power supplies
- Transducer amplifiers
- Bridge amplifiers
- Temperature measurements
- Strain gauge amplifiers
- Precision integrators
- Battery-powered instruments
- Test equipment

3 Description

The OPA171-Q1 family of devices is a 36-V, single-supply, low-noise operational amplifier (op amp) with the ability to operate on supplies ranging from 2.7 V (±1.35 V) to 36 V (±18 V). This series is available in multiple packages and offers low offset, drift, and low quiescent current. The single, dual, and quad versions all have identical specifications for maximum design flexibility.

Unlike most op amps, which are specified at only one supply voltage, the OPAx171-Q1 family of devices is specified from 2.7 V to 36 V. Input signals beyond the supply rails do not cause phase reversal.
The OPAx171-Q1 family of devices is stable with capacitive loads up to 300 pF. The input can operate 100 mV below the negative rail and within 2 V of the top rail during normal operation. The device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail.

The OPAx171-Q1 op amp family is specified from –40°C to +125°C.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
OPA171-Q1	SOT-23 (5)	2.90 mm × 1.60 mm
OPA2171-Q1	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm
OPA4171-Q1	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (December 2015) to Revision D (August 2020)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed OPA2171-Q1 V+ pinout table value to correctly reflect pinout image	3
• Rewrote *Electrical Overstress* section to match with TLV171 commercial data sheet	19

Changes from Revision B (December 2014) to Revision C (December 2015)	Page
• Changed the ESD classification levels for HBM and CDM in the *Features* list	1
• Added the 8-pin VSSOP (DGK) package option for the OPA2171-Q1 device	1
• Clarified the ESD values for each device in the *ESD Ratings* table	5

Changes from Revision A (September 2012) to Revision B (December 2014)	Page
• Added the *Handling Ratings* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Added the OPA2171-Q1 and OPA4171-Q1 devices to the data sheet	1

Changes from Revision * (June, 2011) to Revision A (September, 2012)	Page
• Added second bullet to Features: AEC-Q100 Test Guidance With the Following Results: –Device Temperature Grade1: -40°C to 125°C Ambient Operating Temperature Range –Device HBM ESD Classification Level H2 –Device CDM ESD Classification Level C3A	1
• Added classification levels to ESD ratings in Absolute Maximum Ratings table	5
• Added row to Absolute Maximum Ratings table: Latch-up per JESD78D with Class 1 value	5

5 Pin Configuration and Functions

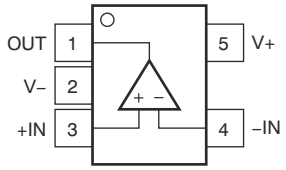


Figure 5-1. OPA171-Q1 DBV Package
5-Pin SOT-23
Top View

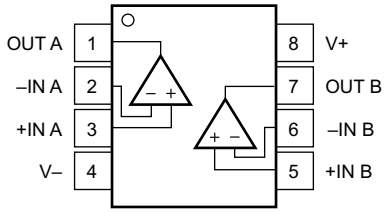


Figure 5-2. OPA2171-Q1 D or DGK Package
8-Pin SOIC and VSSOP
Top View

Pin Functions : OPA171-Q1 and OPA2171-Q1

PIN			I/O	DESCRIPTION
NAME	OPA171-Q1 SOT-23	OPA2171-Q1 SOIC AND VSSOP		
+IN	3	—	I	Noninverting input
+IN A	—	3	I	Noninverting input, channel A
+IN B	—	5	I	Noninverting input, channel B
–IN	4	—	I	Inverting input
–IN A	—	2	I	Inverting input, channel A
–IN B	—	6	I	Inverting input, channel B
OUT	1	—	O	Output
OUT A	—	1	O	Output, channel A
OUT B	—	7	O	Output, channel B
V+	5	8	—	Positive (highest) power supply
V–	2	4	—	Negative (lowest) power supply

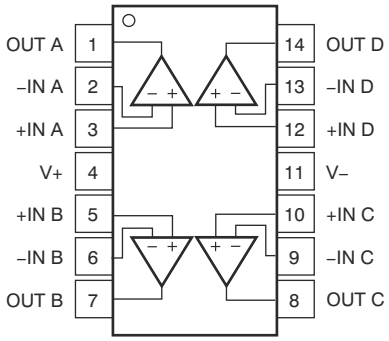


Figure 5-3. OPA4171-Q1 D and PW Packages
14-Pin SOIC and TSSOP
Top View

Pin Functions : OPA4171-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
+IN C	10	I	Noninverting input, channel C
+IN D	12	I	Noninverting input, channel D
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
–IN C	9	I	Inverting input, channel C
–IN D	13	I	Inverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V+	4	—	Positive (highest) power supply
V–	11	—	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage, V_S			40	V
Signal input terminals	Voltage	(V–) – 0.5	(V+) + 0.5	V
	Current		±10	mA
Output short circuit[2]		Continuous		
Junction temperature, T_J			150	°C
Latch-up per JESD78D		Class 1		
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
OPA171-Q1				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	±4000	V
		Charged device model (CDM), per AEC Q100-011	±500	
OPA2171-Q1				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	±4000	V
		Charged device model (CDM), per AEC Q100-011	±1000	
OPA4171-Q1				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage (V+ – V–)	4.5 (±2.25)		36 (±18)	V
Specified operating temperature	–40		125	°C

6.4 Thermal Information — OPA171-Q1 and OPA2171-Q1

THERMAL METRIC[1]		OPA171-Q1	OPA2171-Q1		UNIT
		DBV (SOT-23)	D (SOIC)	DGK (VSSOP)	
		5 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	277.3	116.1	186.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	193.3	69.8	78	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	121.2	56.6	107.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	51.8	22.5	15.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	109.5	56.1	106.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Thermal Information — OPA4171-Q1

THERMAL METRIC[1]		OPA4171-Q1		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.2	106.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	51.8	24.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.4	59.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.5	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.2	54.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics

at T_A = 25°C, V_S = 2.7 V to 36 V, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			0.25	±1.8	mV
	Input offset voltage over temperature	T_A = –40°C to 125°C		0.3	±2	mV
dV_{OS}/dT	Input offset voltage drift (over temperature)	T_A = –40°C to 125°C		0.3	±2 (2)	µV/°C
PSRR	Input offset voltage over temperature vs power supply	V_S = 4.5 V to 36 V		120	±3	µV/V
	Channel separation, DC			5		µV/V
INPUT BIAS CURRENT						
I_B	Input bias current			±8	±15	pA
	Input bias current over temperature				±3.5	nA
I_{OS}	Input offset current			±4		pA
	Input offset current over temperature				±3.5	nA
NOISE						
	Input voltage noise	f = 0.1 Hz to 10 Hz		3		μV_{PP}
e_n	Input voltage noise density	f = 100 Hz		25		$nV/\sqrt{Hz}$
		f = 1 kHz		14		$nV/\sqrt{Hz}$
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range(1)		(V–) – 0.1		(V+) – 2	V
CMRR	Common-mode rejection ratio (over temperature)	V_S = ±2.25 V (V–) – 0.1 V < V_{CM} < (V+) – 2 V	90	104		dB
		V_S = ±18 V (V–) – 0.1 V < V_{CM} < (V+) – 2 V	104	120		dB
INPUT IMPEDANCE						
	Differential			100 || 3		MΩ || pF
	Common-mode			6 || 3		10^{12}Ω || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain (over temperature)	V_S = 4.5 V to 36 V (V–) + 0.35 V < V_O < (V+) – 0.35 V	110	130		dB
FREQUENCY RESPONSE						
GBP	Gain bandwidth product			3		MHz
SR	Slew rate	G = 1		1.5		V/µs
t_S	Settling time	To 0.1%, V_S = ±18 V G = 1, 10-V step		6		µs
		To 0.01% (12 bit), V_S = ±18 V G = 1, 10-V step		10		µs
	Overload recovery time	$V_{±IN}$ × Gain > V_S		2		µs
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz V_O = 3 V_{RMS}		0.0002%		
OUTPUT						
V_O	Voltage output swing from rail (over temperature)	R_L = 10 kΩ A_{OL} ≥ 110 dB	(V–) + 0.35		(V+) – 0.35	V
I_{SC}	Short-circuit current	Sourcing		25		mA
		Sinking		–37		
C_{LOAD}	Capacitive load drive			See *Section 6.7*		pF
R_O	Open-loop output resistance	f = 1 MHz, I_O = 0 A		150		Ω
POWER SUPPLY						
V_S	Specified voltage range	T_A = –40°C to 125°C	4.5		36	V

at T_A = 25°C, V_S = 2.7 V to 36 V, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_Q	Quiescent current per amplifier	I_O = 0 A, T_A = –40°C to 125°C		475	595	µA

(1) The input range can be extended beyond (V+) – 2 V up to V+ at reduced performance. See *Section 6.7* and *Section 7* for additional information.

(2) Not production tested.

6.7 Typical Characteristics

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

Table 6-1. Characteristic Performance Measurements

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 6-1
Offset Voltage Drift Distribution	Figure 6-2
Offset Voltage vs Temperature	Figure 6-3
Offset Voltage vs Common-Mode Voltage	Figure 6-4
Offset Voltage vs Common-Mode Voltage (Upper Stage)	Figure 6-5
Offset Voltage vs Power Supply	Figure 6-6
I_B and I_{OS} vs Common-Mode Voltage	Figure 6-7
Input Bias Current vs Temperature	Figure 6-8
Output Voltage Swing vs Output Current (Maximum Supply)	Figure 6-9
CMRR and PSRR vs Frequency (Referred-to Input)	Figure 6-10
CMRR vs Temperature	Figure 6-11
PSRR vs Temperature	Figure 6-12
0.1Hz to 10Hz Noise	Figure 6-13
Input Voltage Noise Spectral Density vs Frequency	Figure 6-14
THD+N Ratio vs Frequency	Figure 6-15
THD+N vs Output Amplitude	Figure 6-16
Quiescent Current vs Temperature	Figure 6-17
Quiescent Current vs Supply Voltage	Figure 6-18
Open-Loop Gain and Phase vs Frequency	Figure 6-19
Closed-Loop Gain vs Frequency	Figure 6-20
Open-Loop Gain vs Temperature	Figure 6-21
Open-Loop Output Impedance vs Frequency	Figure 6-22
Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)	Figure 6-23, Figure 6-24
No Phase Reversal	Figure 6-25
Positive Overload Recovery	Figure 6-26
Negative Overload Recovery	Figure 6-27
Small-Signal Step Response (100 mV)	Figure 6-28, Figure 6-29
Large-Signal Step Response	Figure 6-30, Figure 6-31
Large-Signal Settling Time (10-V Positive Step)	Figure 6-32
Large-Signal Settling Time (10-V Negative Step)	Figure 6-33
Short-Circuit Current vs Temperature	Figure 6-34
Maximum Output Voltage vs Frequency	Figure 6-35
Channel Separation vs Frequency	Figure 6-36

6.7.1 Typical Characteristics

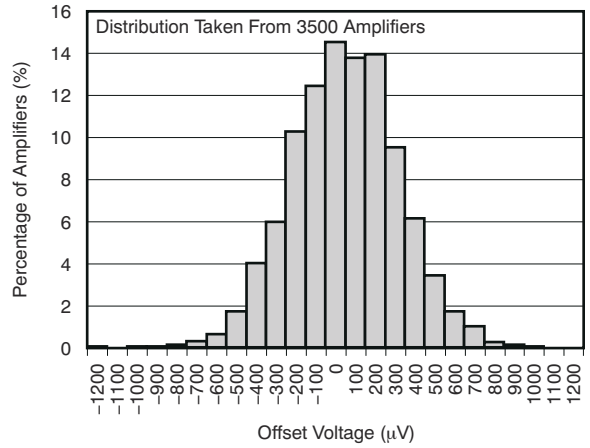


Figure 6-1. Offset Voltage Production Distribution

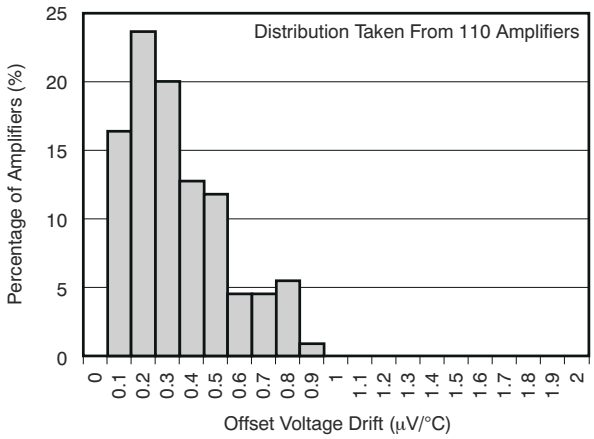


Figure 6-2. Offset Voltage Drift Distribution

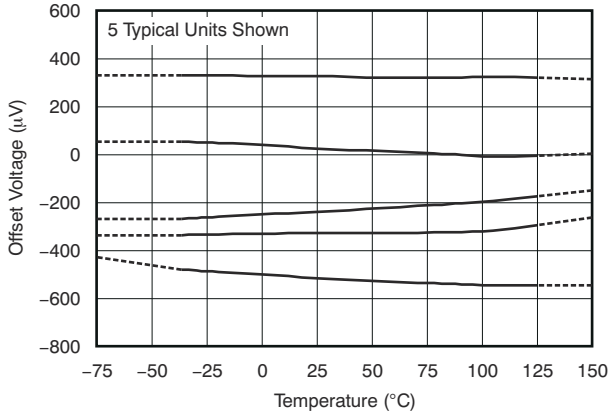


Figure 6-3. Offset Voltage vs Temperature

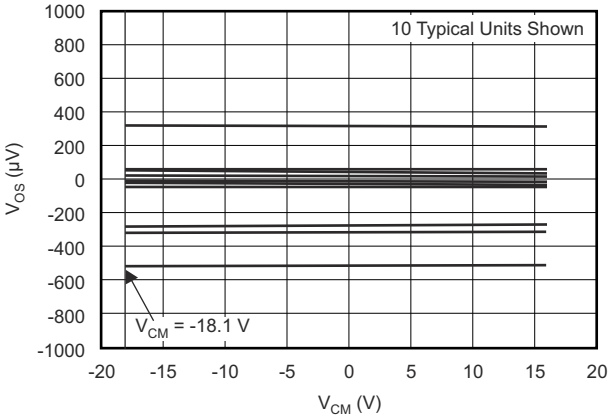


Figure 6-4. Offset Voltage vs Common-Mode Voltage: V_{SUPPLY} (V) = ±18 V

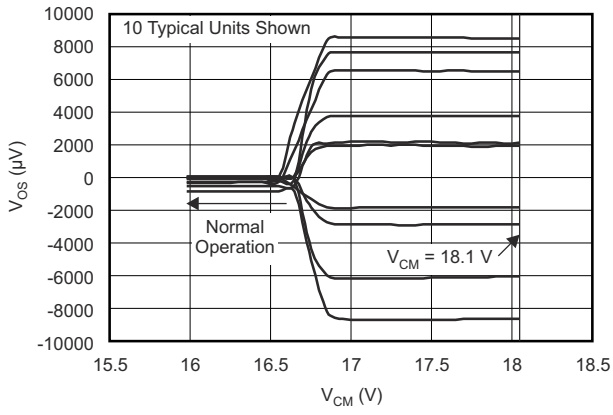


Figure 6-5. Offset Voltage vs Common-Mode Voltage: V_{SUPPLY} (V) = ±18 V (Upper Stage)

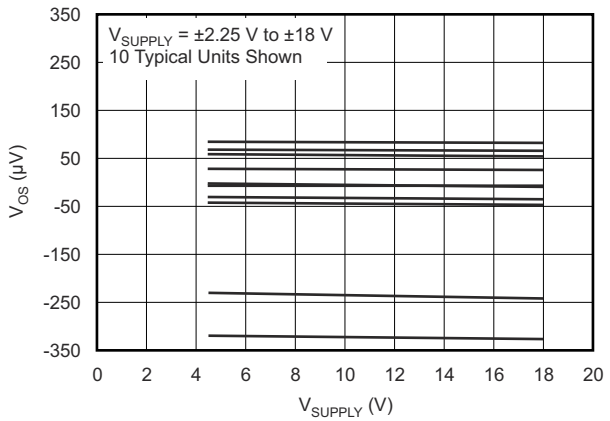


Figure 6-6. Offset Voltage vs Power Supply

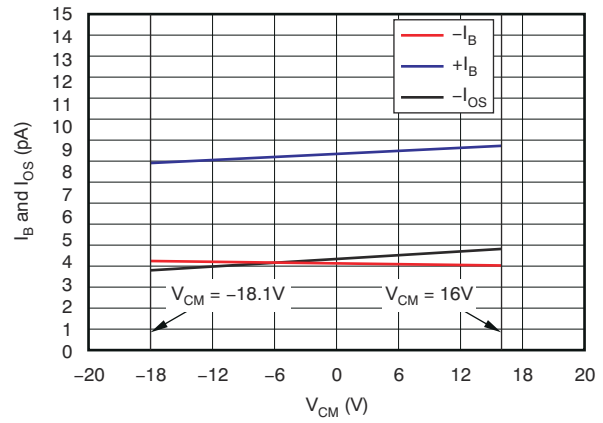


Figure 6-7. I_B and I_{OS}vs Common-Mode Voltage

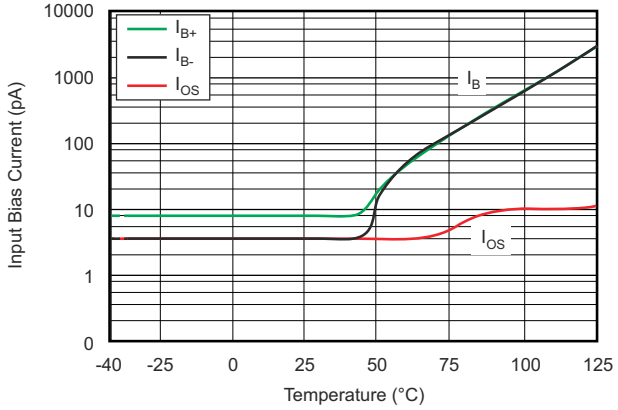


Figure 6-8. Input Bias Current vs Temperature

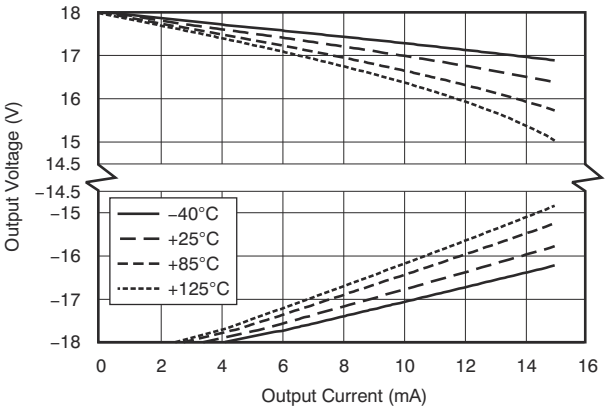


Figure 6-9. Output Voltage Swing vs Output Current (Maximum Supply)

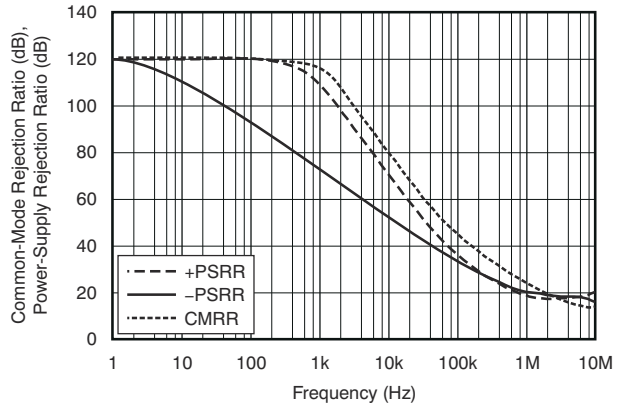


Figure 6-10. CMRR and PSRR vs Frequency (Referred-to Input)

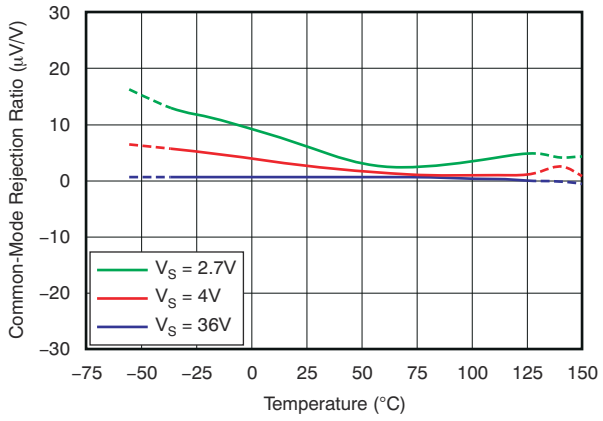


Figure 6-11. CMRR vs Temperature

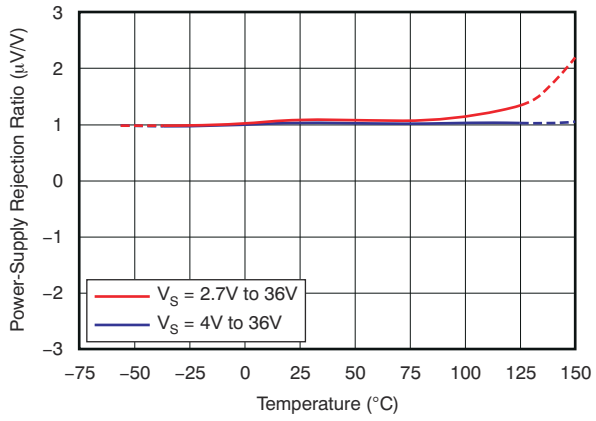


Figure 6-12. PSRR vs Temperature

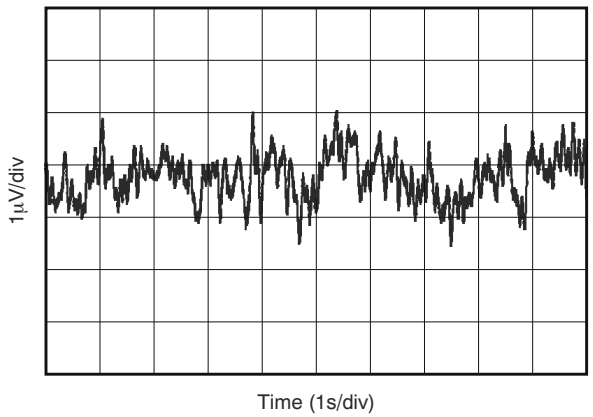


Figure 6-13. 0.1- to 10-Hz Noise

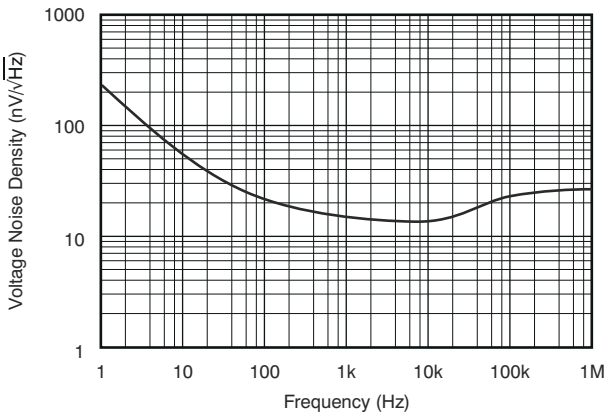


Figure 6-14. Input Voltage Noise Spectral Density vs Frequency

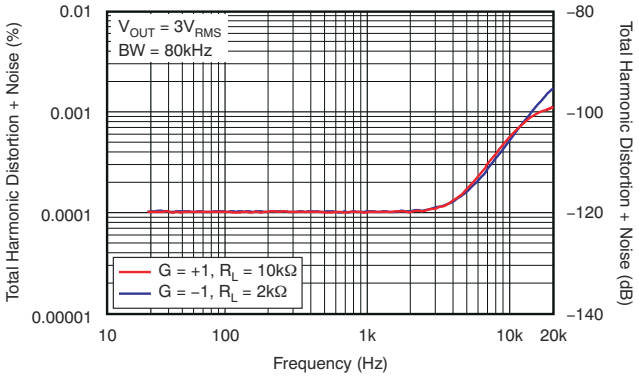


Figure 6-15. THD+N Ratio vs Frequency

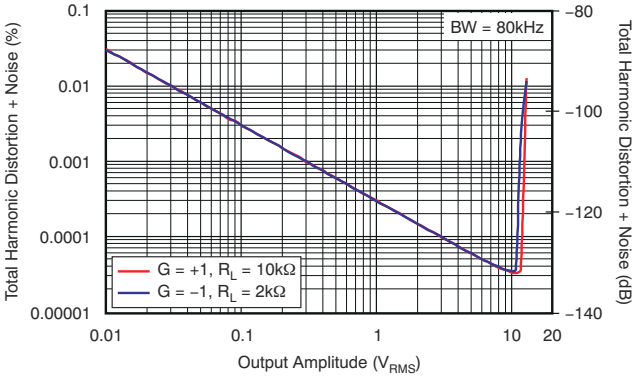


Figure 6-16. THD+N vs Output Amplitude

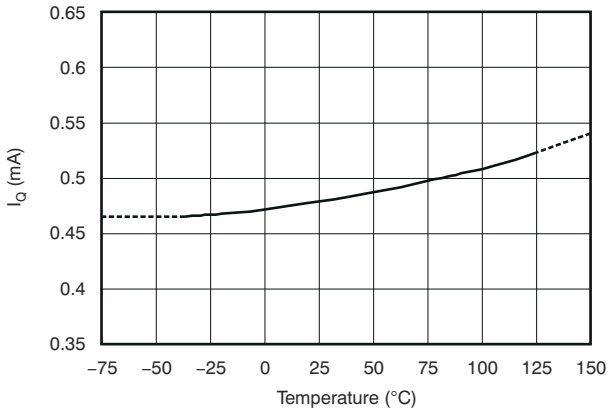


Figure 6-17. Quiescent Current vs Temperature

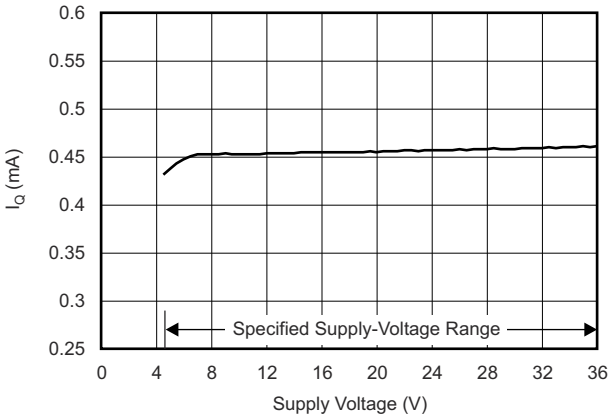


Figure 6-18. Quiescent Current vs Supply Voltage

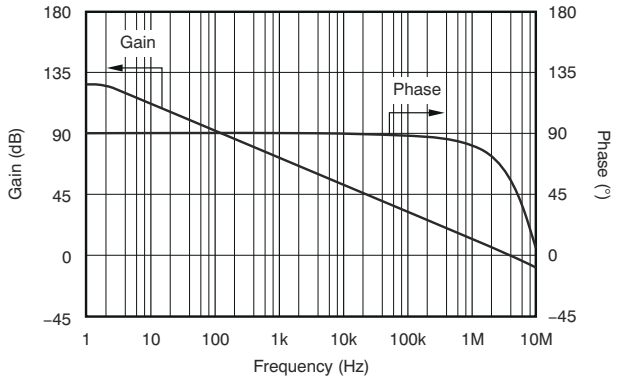


Figure 6-19. Open-Loop Gain and Phase vs Frequency

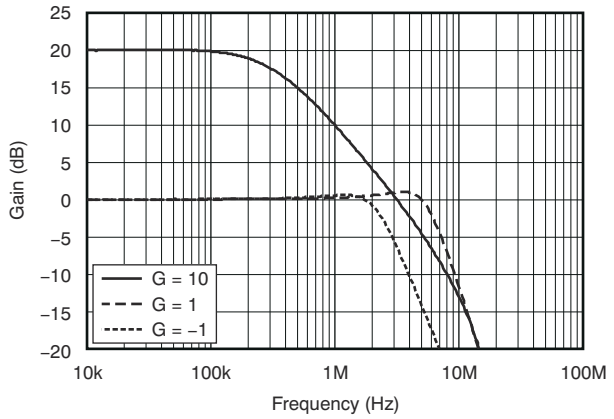


Figure 6-20. Closed-Loop Gain vs Frequency

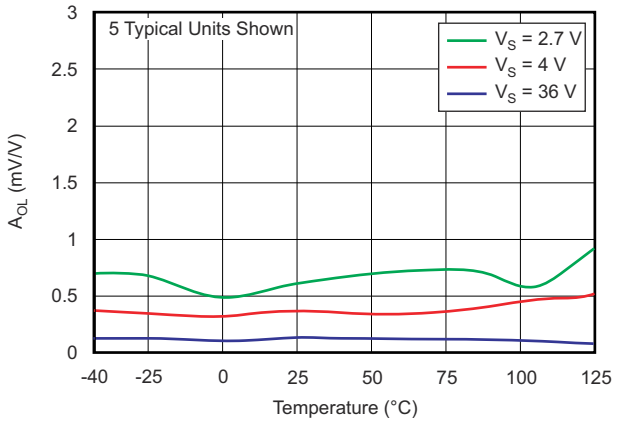


Figure 6-21. Open-Loop Gain vs Temperature

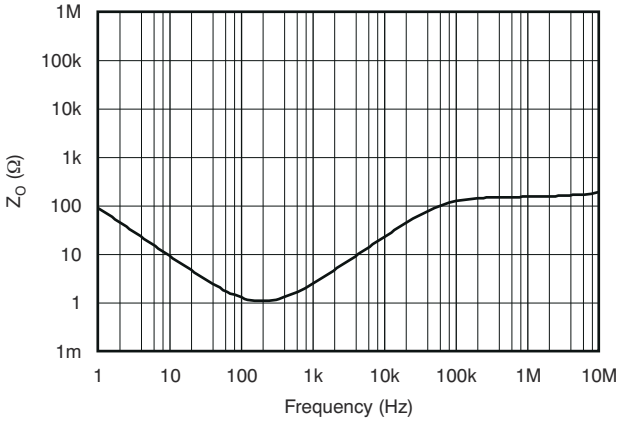


Figure 6-22. Open-Loop Output Impedance vs Frequency

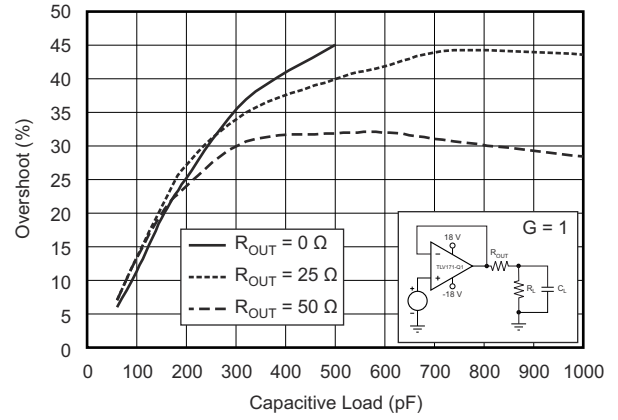


Figure 6-23. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

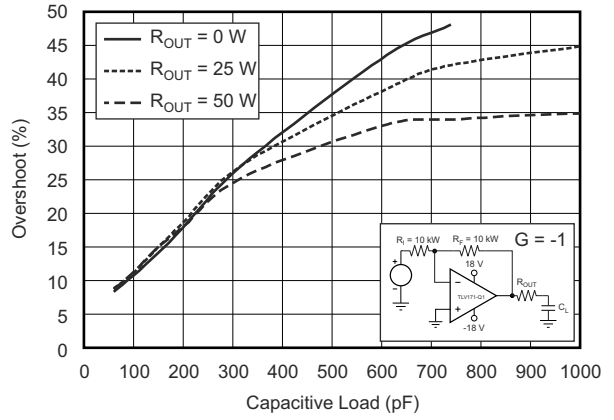


Figure 6-24. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

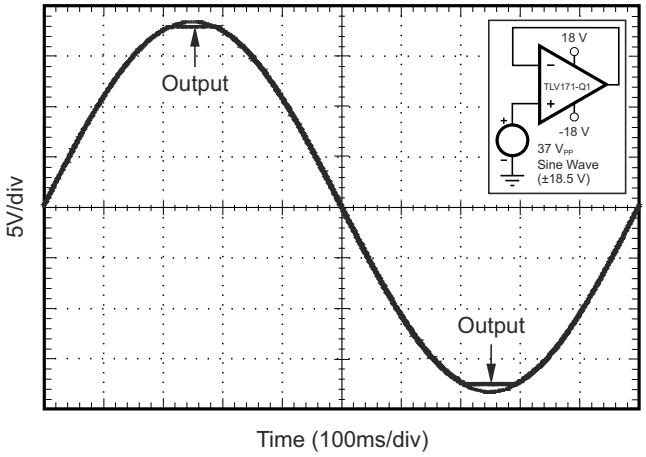


Figure 6-25. No Phase Reversal

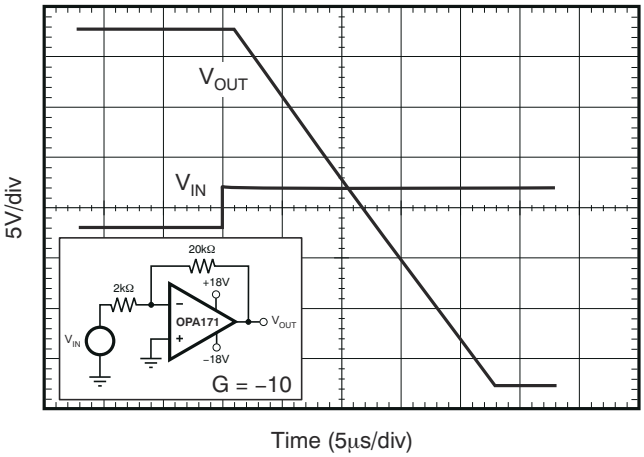


Figure 6-26. Positive Overload Recovery

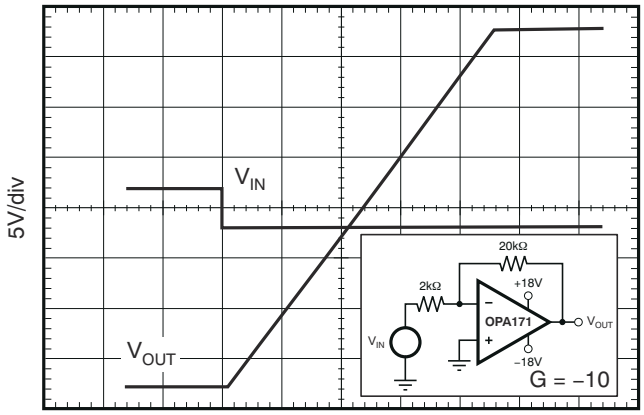


Figure 6-27. Negative Overload Recovery

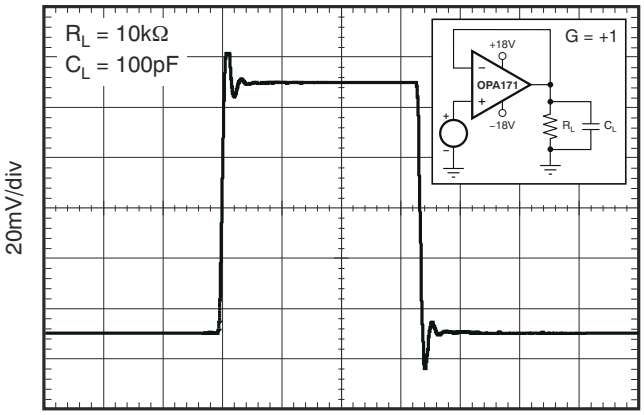


Figure 6-28. Small-Signal Step Response (100 mV)

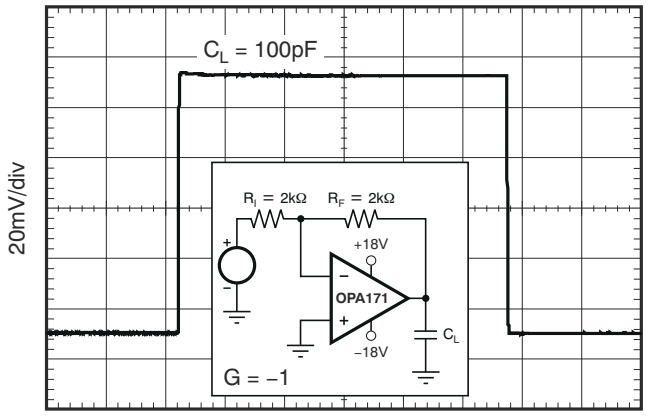


Figure 6-29. Small-Signal Step Response (100 mV)

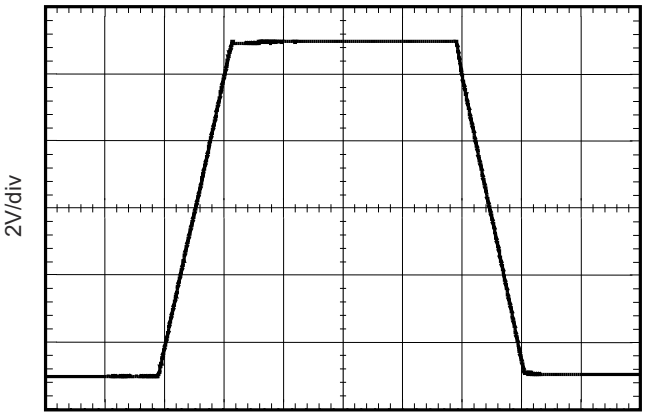
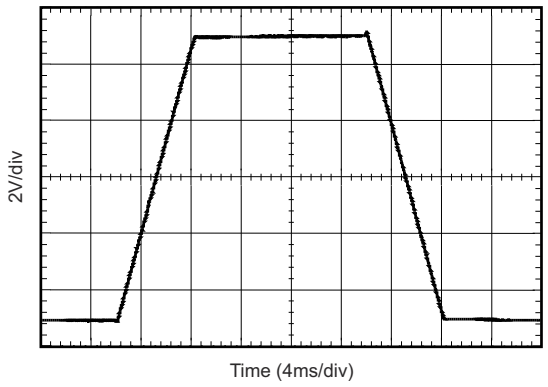
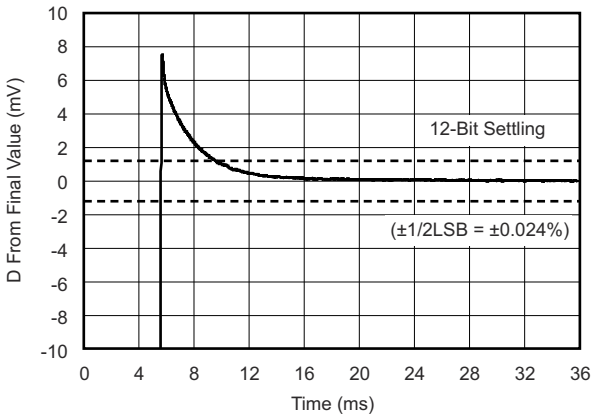


Figure 6-30. Large-Signal Step Response



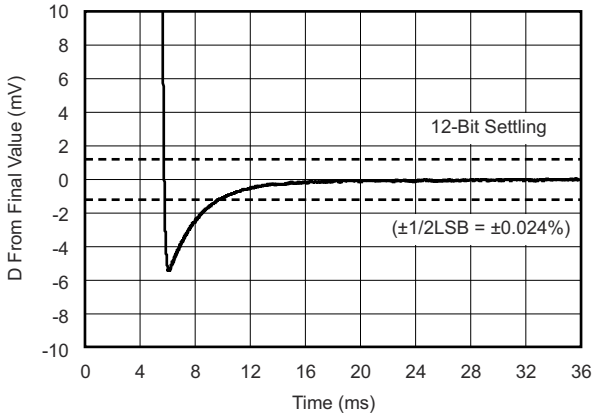
G = –1 R_L = 10 kΩ C_L = 100 pF

Figure 6-31. Large-Signal Step Response



G = –1

Figure 6-32. Large-Signal Settling Time (10-V Positive Step)



G = –1

Figure 6-33. Large-Signal Settling Time (10-V Negative Step)

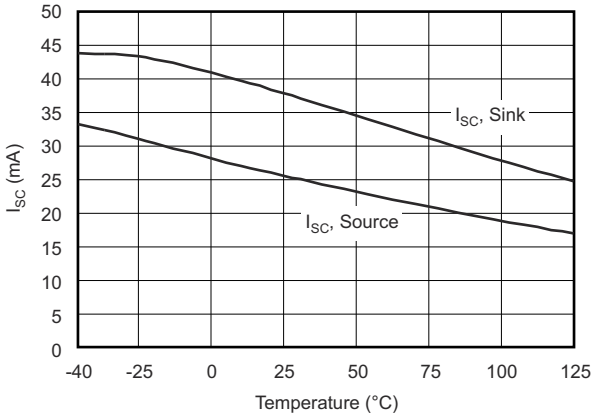


Figure 6-34. Short-Circuit Current vs Temperature

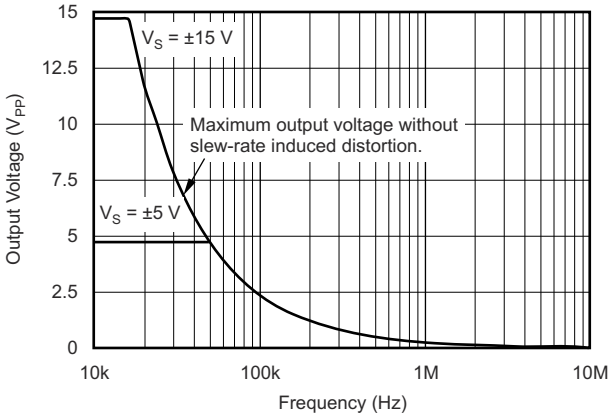


Figure 6-35. Maximum Output Voltage vs Frequency

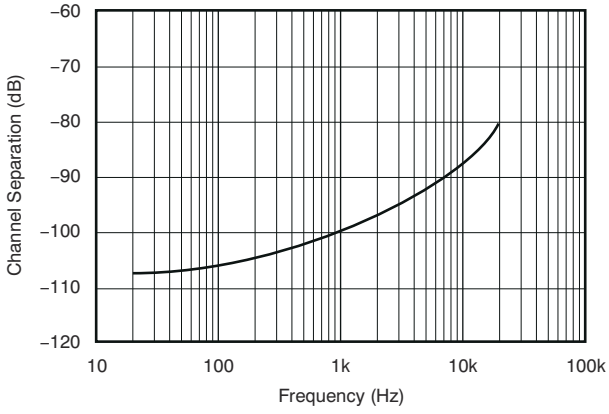


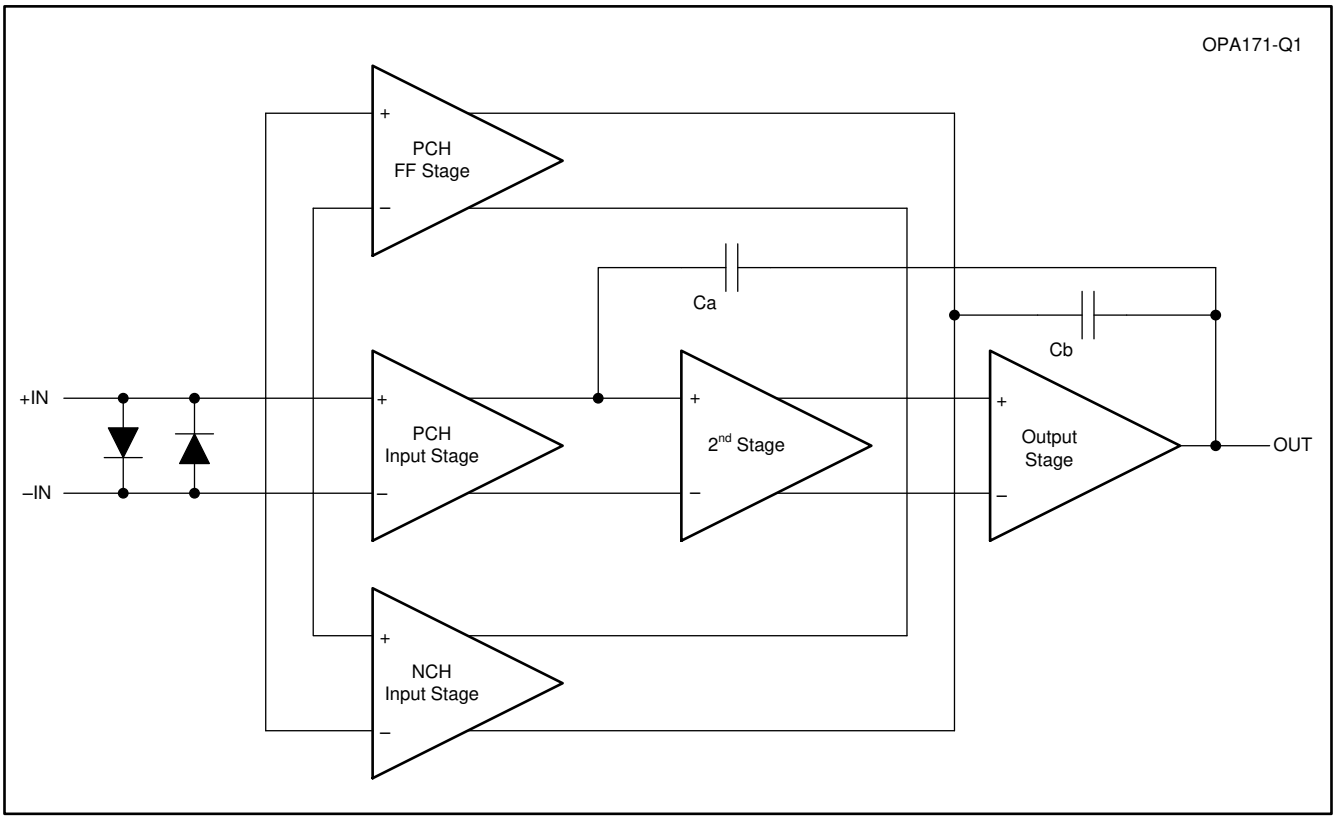
Figure 6-36. Channel Separation vs Frequency

7 Detailed Description

7.1 Overview

The OPAx171-Q1 family of operational amplifiers provides high overall performance, making them ideal for many general-purpose applications. The excellent offset drift of only 1.5 µV/°C (maximum) provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, AOL, and superior THD.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Characteristics

The OPAx171-Q1 family of devices is specified for operation from 2.7 V to 36 V (±1.35 V to ±18 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are shown in *Section 6.7*.

7.3.2 Phase-Reversal Protection

The OPAx171-Q1 family of devices has an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPAx171-Q1 family of devices prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. Figure 7-1 shows this performance.

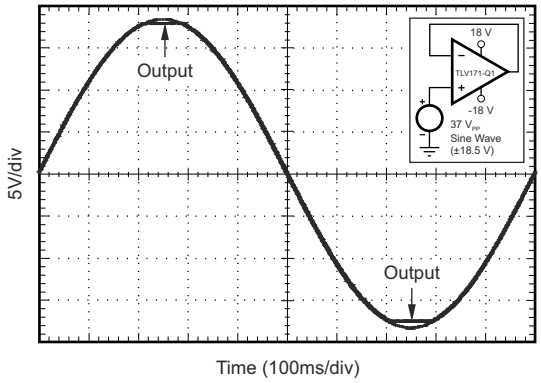


Figure 7-1. No Phase Reversal

7.3.3 Capacitive Load and Stability

The dynamic characteristics of the OPAx171-Q1 family of devices are optimized for commonly encountered operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50 Ω) in series with the output. Figure 7-2 and Figure 7-3 shows small-signal overshoot versus capacitive load for several values of R_{OUT}. For details of analysis techniques and application circuits, see *Applications Bulletin AB-028*, available for download from TI.com.

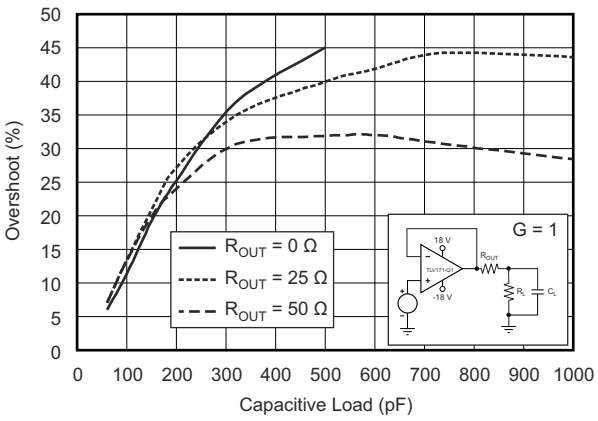


Figure 7-2. Small-Signal Overshoot versus Capacitive Load (100-mV Output Step)

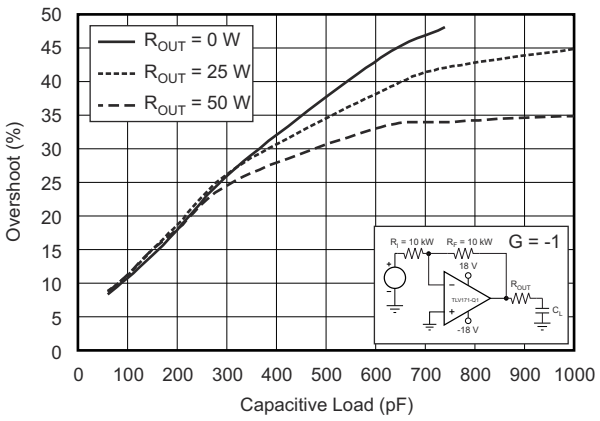


Figure 7-3. Small-Signal Overshoot versus Capacitive Load (100-mV Output Step)

7.4 Device Functional Modes

7.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the OPAx171-Q1 family of devices extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. The typical performance in this range is listed in Table 7-1.

Table 7-1. Typical Performance Range

PARAMETER	MIN	TYP	MAX	UNIT
Input common-mode voltage	(V+) – 2		(V+) + 0.1	V
Offset voltage		7		mV
Offset voltage vs temperature		12		µV/°C
Common-mode rejection		65		dB
Open-loop gain		60		dB
GBW		0.7		MHz
Slew rate		0.7		V/µs
Noise at f = 1kHz		30		nV/$\sqrt{\text{Hz}}$

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPAx171-Q1 operational amplifier family provides high overall performance, making the device ideal for many general-purpose applications. The excellent offset drift of only 2 µV/°C provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

8.1.1 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits for protection from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. illustrates the ESD circuits contained in the (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

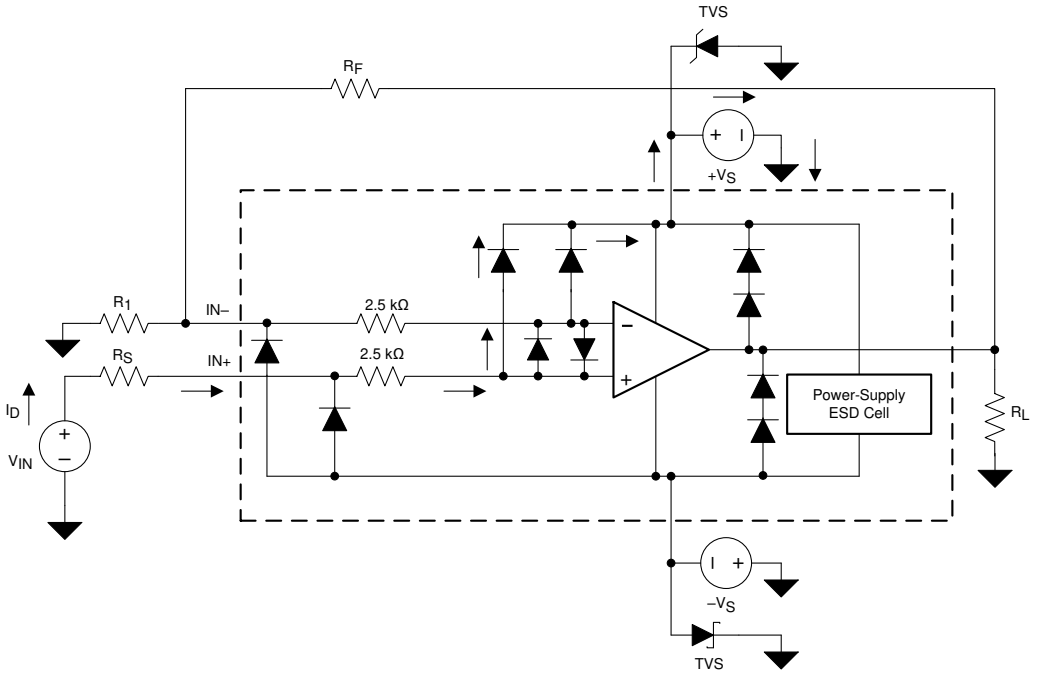


Figure 8-1. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to

provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPAx171-Q1 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (as shown in), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage (V+) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If V+ can sink the current, one of the upper input steering diodes conducts and directs current to V+. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies (V+ or V–) are at 0 V. Again, this question depends on the supply characteristic when at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply pins; see . Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe-operating, supply-voltage level.

The OPAx171-Q1 input pins are protected from excessive differential voltage with back-to-back diodes; see . In most circuit applications, the input protection circuitry has no effect. However, in low-gain or G = 1 circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, limit the input signal current to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the input signal current. This input series resistor degrades the low-noise performance of the OPAx171-Q1. illustrates an example configuration that implements a current-limiting feedback resistor.

8.2 Typical Application

8.2.1 Capacitive Load Drive Solution Using an Isolation Resistor

The OPAx171-Q1 device can be used capacitive loads such as cable shields, reference buffers, MOSFET gates, and diodes. The circuit uses an isolation resistor (R_{ISO}) to stabilize the output of an op amp. R_{ISO} modifies the open loop gain of the system to ensure the circuit has sufficient phase margin.

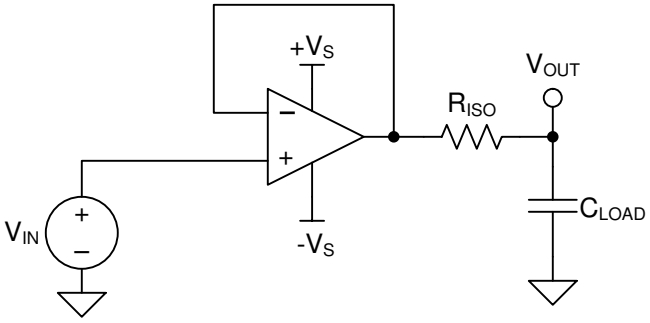


Figure 8-2. Unity-Gain Buffer with R_{ISO} Stability Compensation

8.2.1.1 Design Requirements

The design requirements are:

- Supply voltage: 30 V (±15 V)
- Capacitive loads: 100 pF, 1000 pF, 0.01 µF, 0.1 µF, and 1 µF
- Phase margin: 45° and 60°

8.2.1.2 Detailed Design Procedure

Figure 8-3 shows a unity-gain buffer driving a capacitive load. Equation 1 shows the transfer function for the circuit in Figure 8-3. Not shown in Figure 8-3 is the open-loop output resistance of the op amp, R_o.

$$T(s) = \frac{1 + C_{LOAD} \times R_{ISO} \times s}{1 + (R_o + R_{ISO}) \times C_{LOAD} \times s} \quad (1)$$

The transfer function in Equation 1 has a pole and a zero. The frequency of the pole (f_p) is determined by (R_o + R_{ISO}) and C_{LOAD}. Components R_{ISO} and C_{LOAD} determine the frequency of the zero (f_z). A stable system is obtained by selecting R_{ISO} such that the rate of closure (ROC) between the open-loop gain (A_{OL}) and 1/β is 20 dB/decade. Figure 8-3 shows the concept. The 1/β curve for a unity-gain buffer is 0 dB.

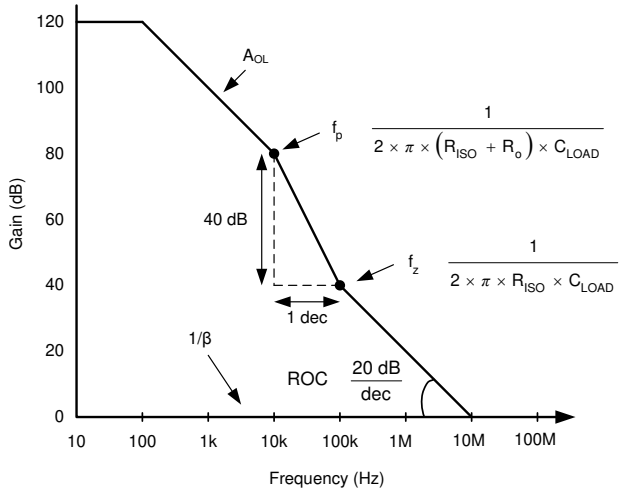


Figure 8-3. Unity-Gain Amplifier with R_{ISO} Compensation

ROC stability analysis is typically simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of R_o. In addition to simulating the ROC, a robust stability analysis includes a measurement of overshoot percentage and AC gain peaking of the circuit using a function generator, oscilloscope, and gain and phase analyzer. Phase margin is then calculated from these measurements. Table 8-1 lists the overshoot percentage and AC gain peaking that correspond to phase margins of 45° and 60°. For more details on this design and other alternative devices that can be used in place of the OPA171-Q1 , see *Capacitive Load Drive Solution using an Isolation Resistor*.

Table 8-1. Phase Margin versus Overshoot and AC Gain Peaking

PHASE MARGIN	OVERSHOOT	AC GAIN PEAKING
45°	23.3%	2.35 dB
60°	8.8%	0.28 dB

8.2.1.3 Application Curve

The OPAx171-Q1 series meets the supply voltage requirements of 30 V. The OPAx171-Q1 device was tested for various capacitive loads and R_{ISO} was adjusted to achieve an overshoot corresponding to Table 8-1. Figure 8-4 shows the test results.

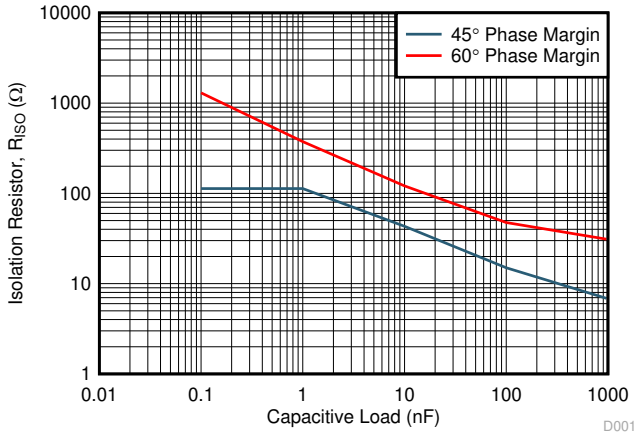


Figure 8-4. R_{ISO} vs C_{LOAD}

9 Power Supply Recommendations

The OPAx171-Q1 family of devices is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Section 6.7*.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the *Section 6.1* table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For detailed information on bypass capacitor placement, see *Section 10*.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 10-1, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

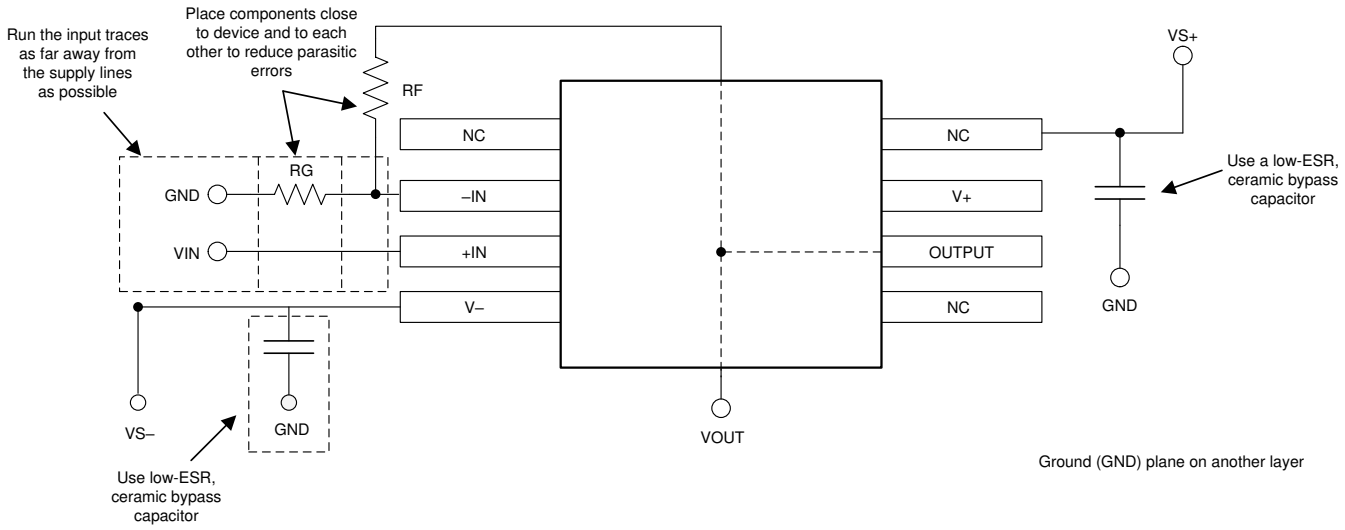


Figure 10-1. Operational Amplifier Board Layout for Noninverting Configuration

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Applications Bulletin AB-028*
- *Capacitive Load Drive Solution Using an Isolation Resistor*

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 11-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA171-Q1	Click here	Click here	Click here	Click here	Click here
OPA2171-Q1	Click here	Click here	Click here	Click here	Click here
OPA4171-Q1	Click here	Click here	Click here	Click here	Click here

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.5 Trademarks

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11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA171AQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OULQ	Samples
OPA2171AQDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2171	Samples
OPA2171AQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	2171AQ	Samples
OPA4171AQDRQ1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4171Q1	Samples
OPA4171AQPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	O4171Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

10-Dec-2020

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA171-Q1, OPA2171-Q1, OPA4171-Q1 :

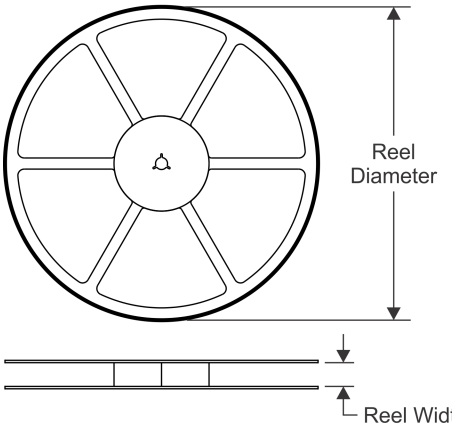
- Catalog: OPA171, OPA2171, OPA4171
- Enhanced Product: OPA2171-EP

NOTE: Qualified Version Definitions:

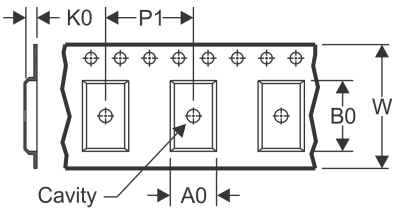
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

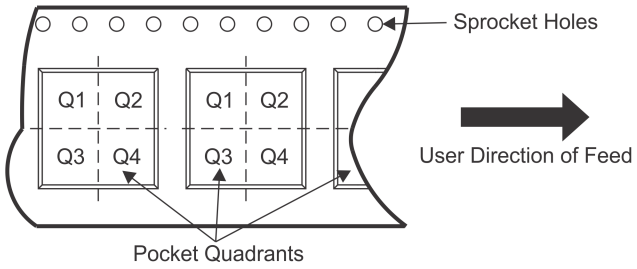


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

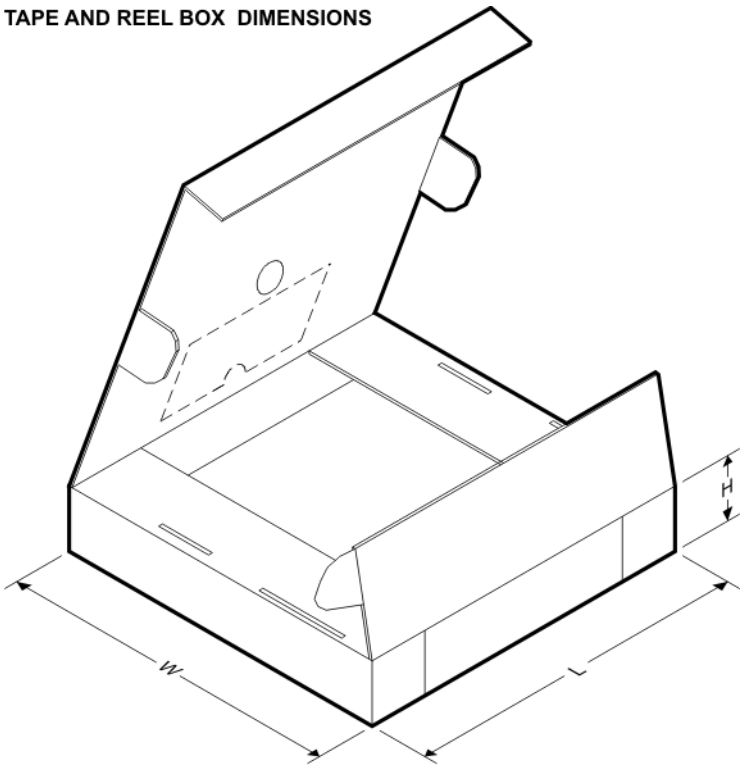
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA171AQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA2171AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2171AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4171AQDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4171AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

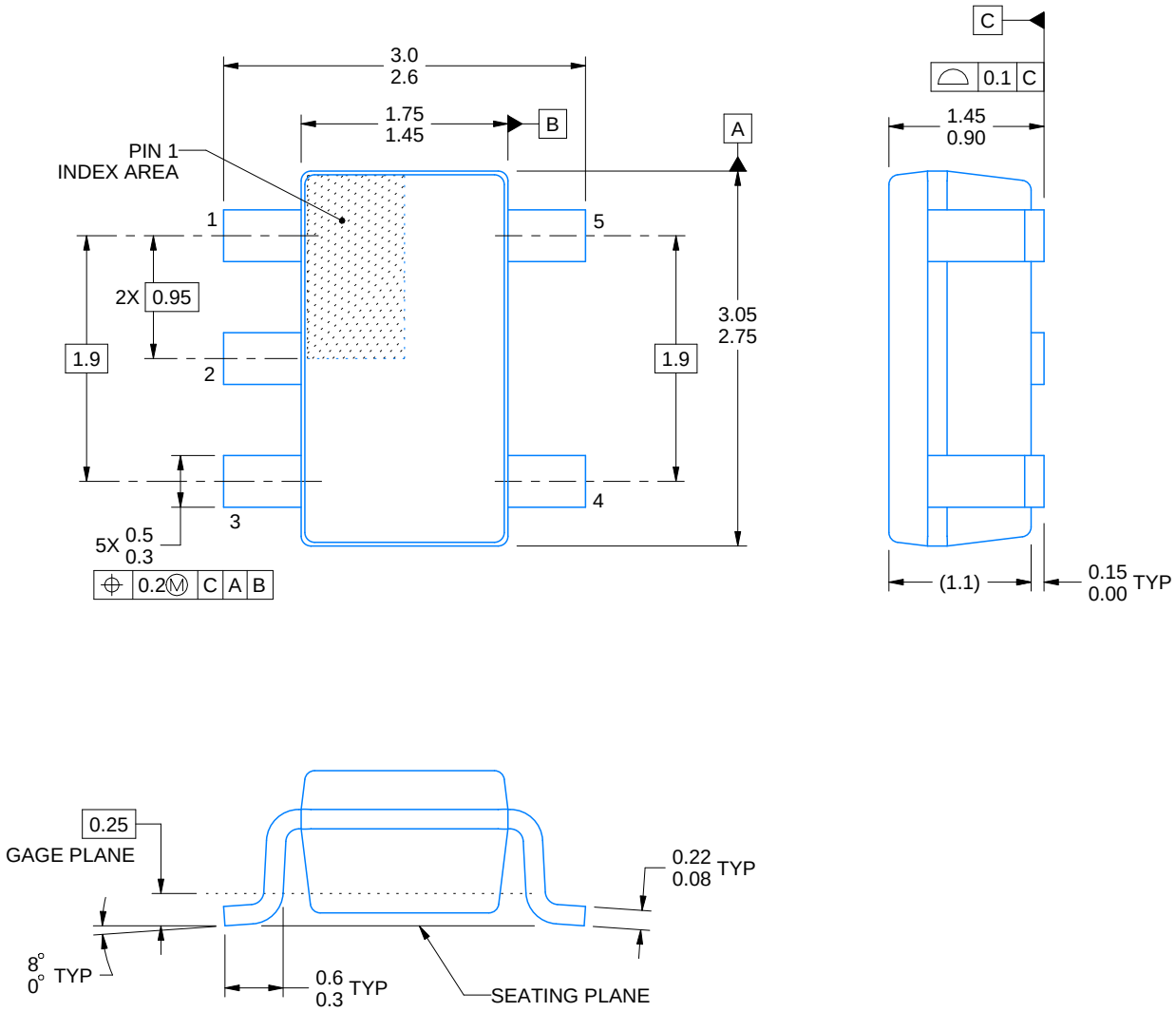
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA171AQDBVRQ1	SOT-23	DBV	5	3000	202.0	201.0	28.0
OPA2171AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2171AQDRQ1	SOIC	D	8	2500	853.0	449.0	35.0
OPA4171AQDRQ1	SOIC	D	14	2500	853.0	449.0	35.0
OPA4171AQPWRQ1	TSSOP	PW	14	2000	853.0	449.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/F 06/2021

NOTES:

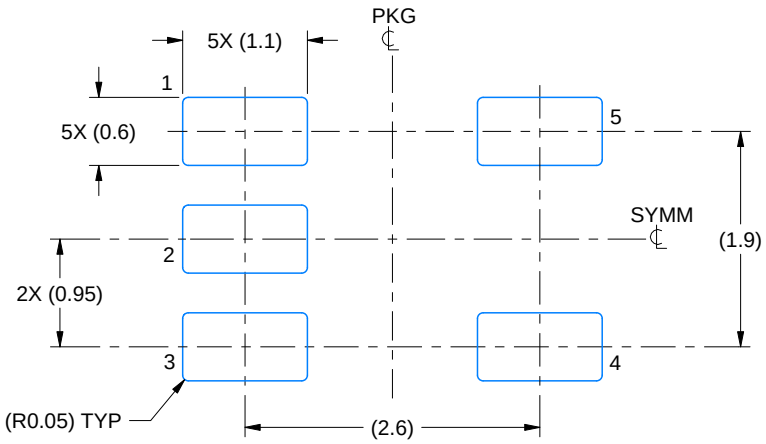
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.

EXAMPLE BOARD LAYOUT

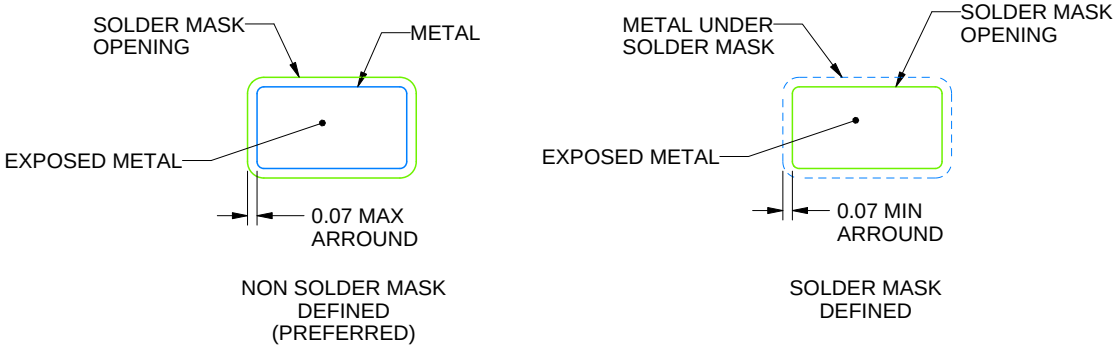
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

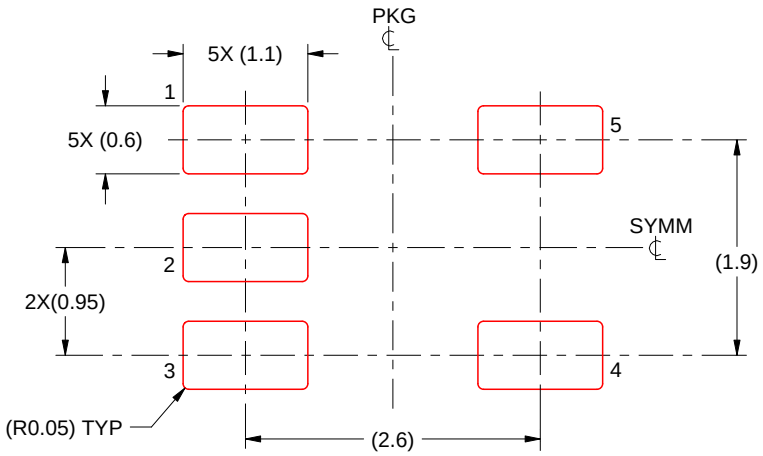
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



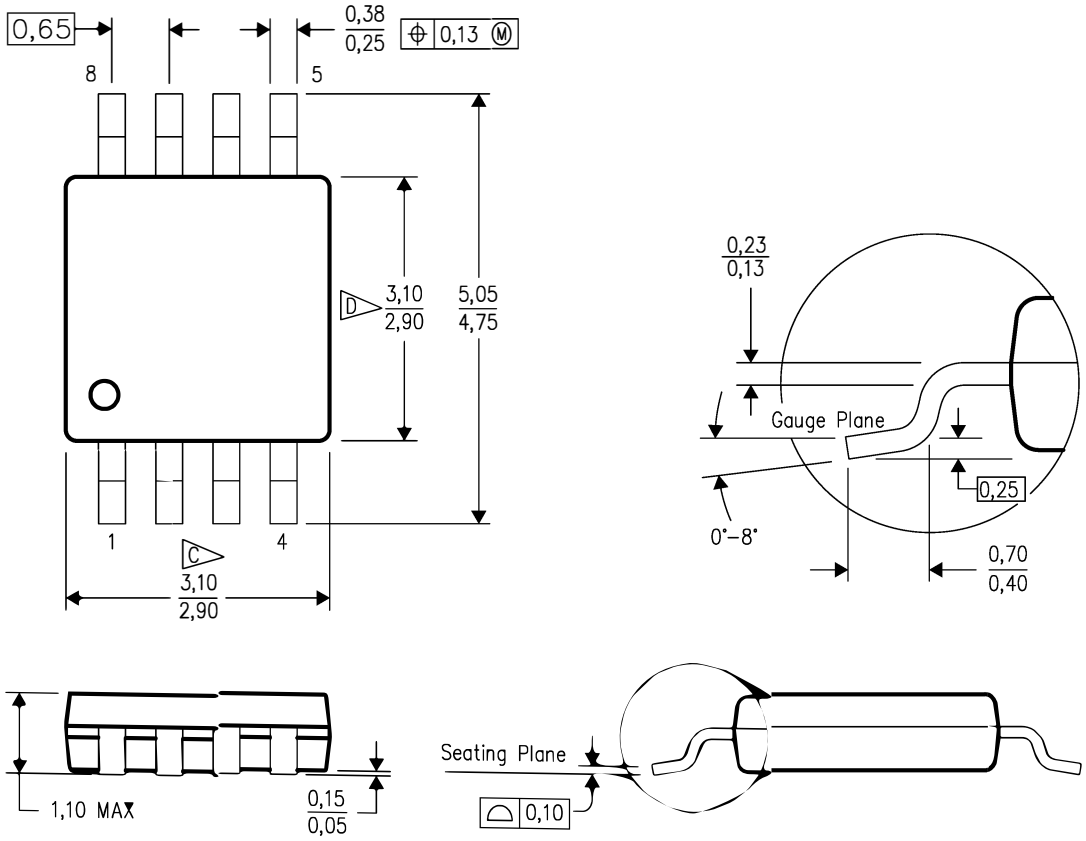
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

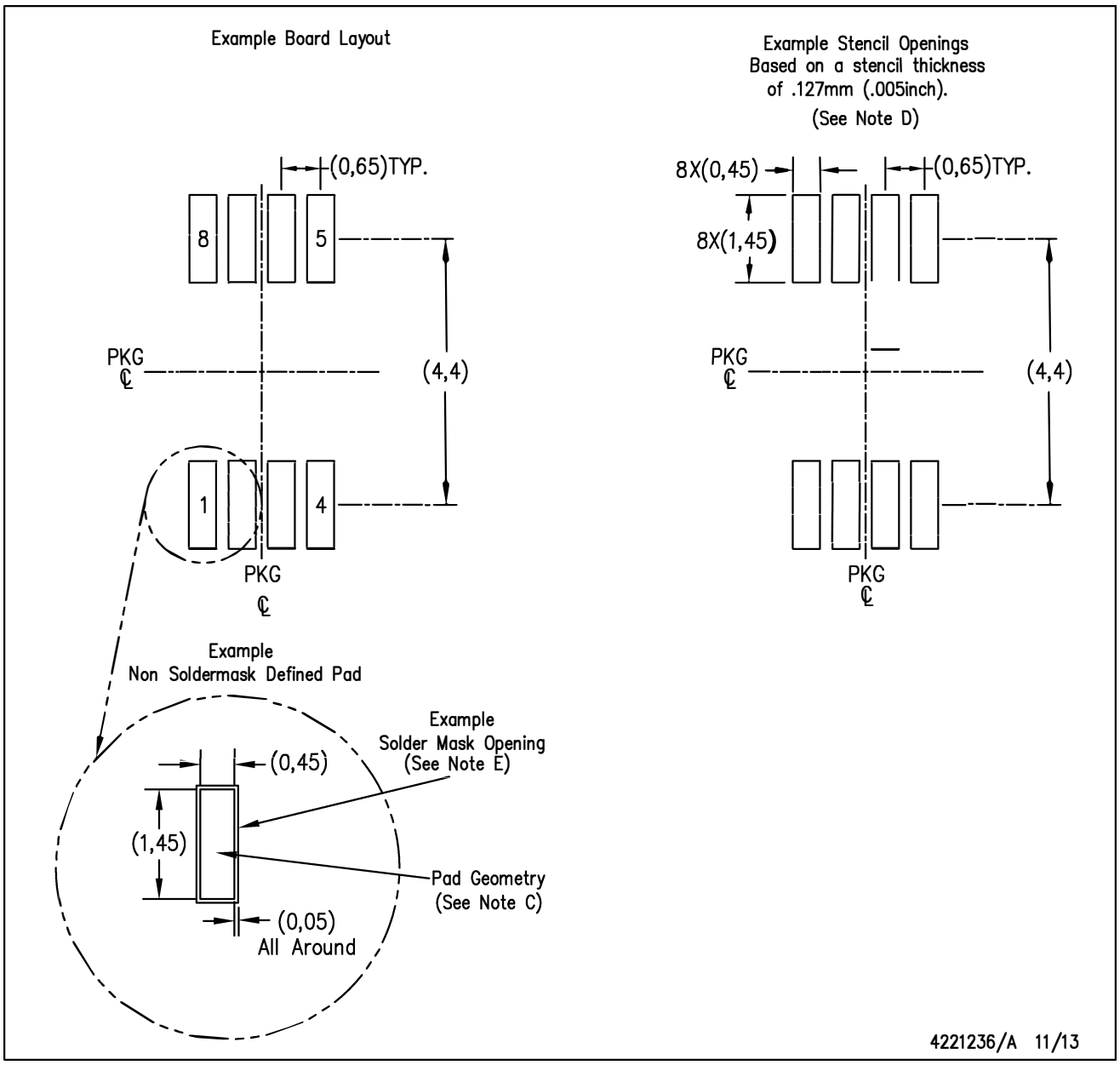
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

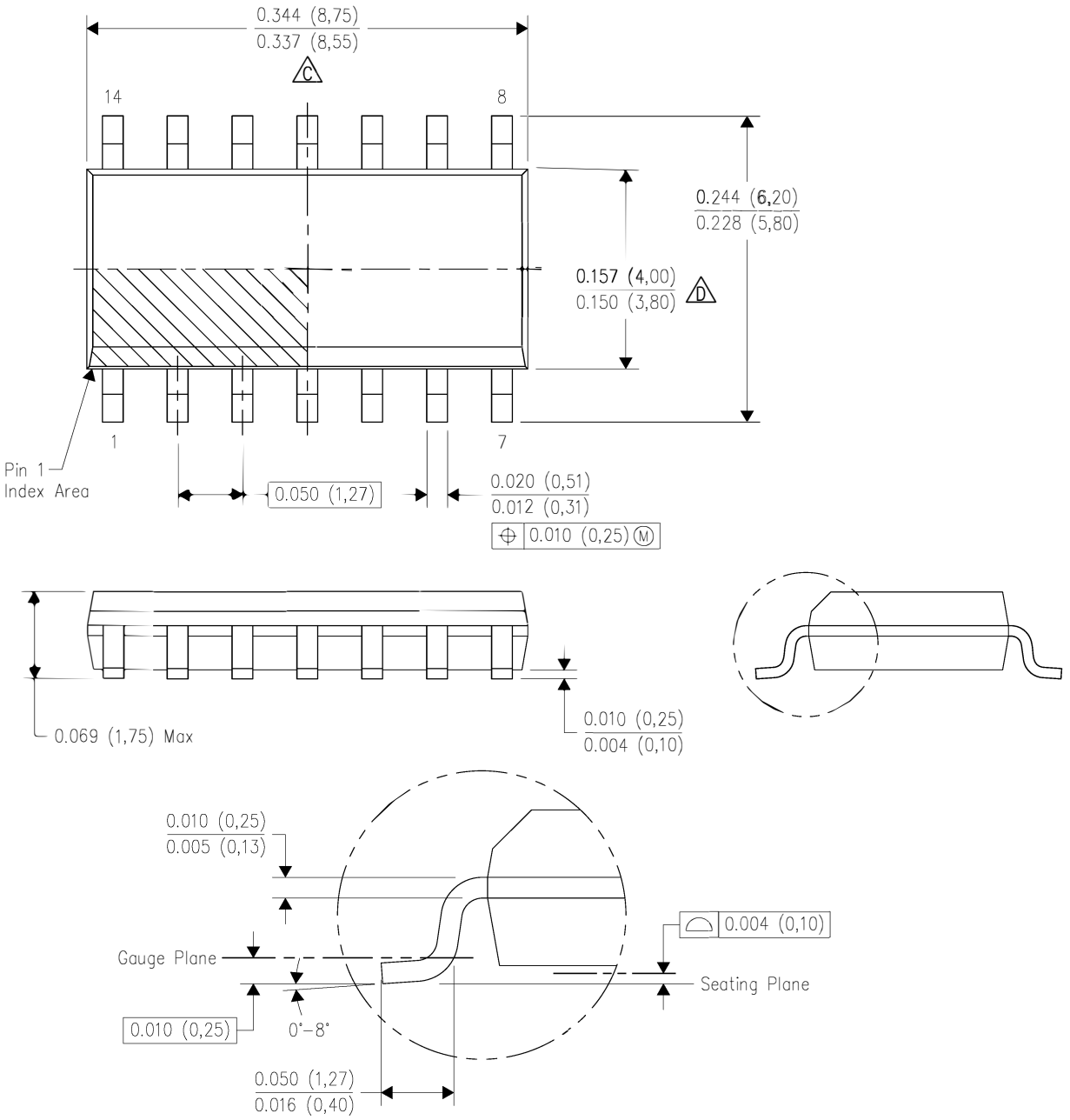
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



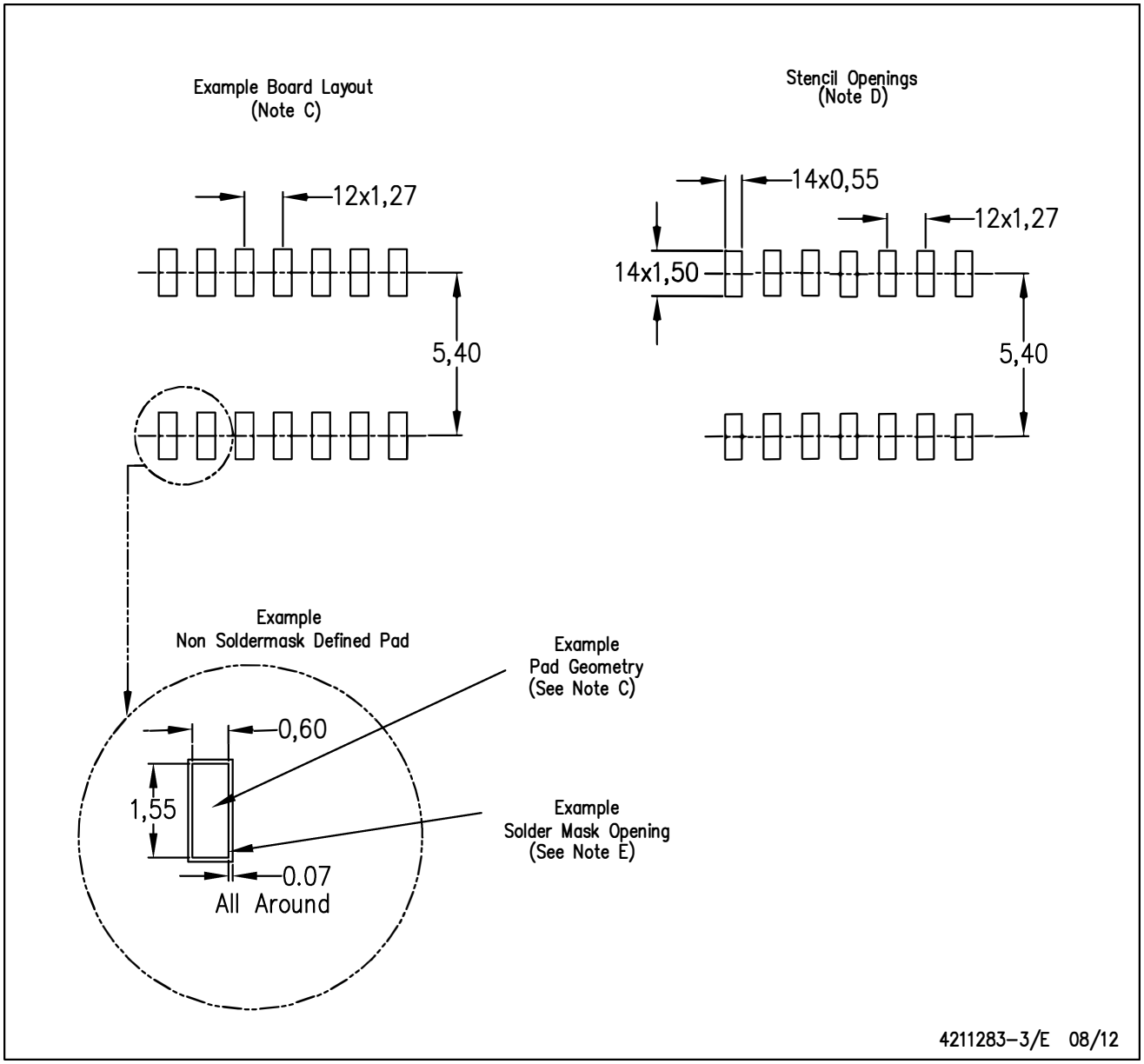
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



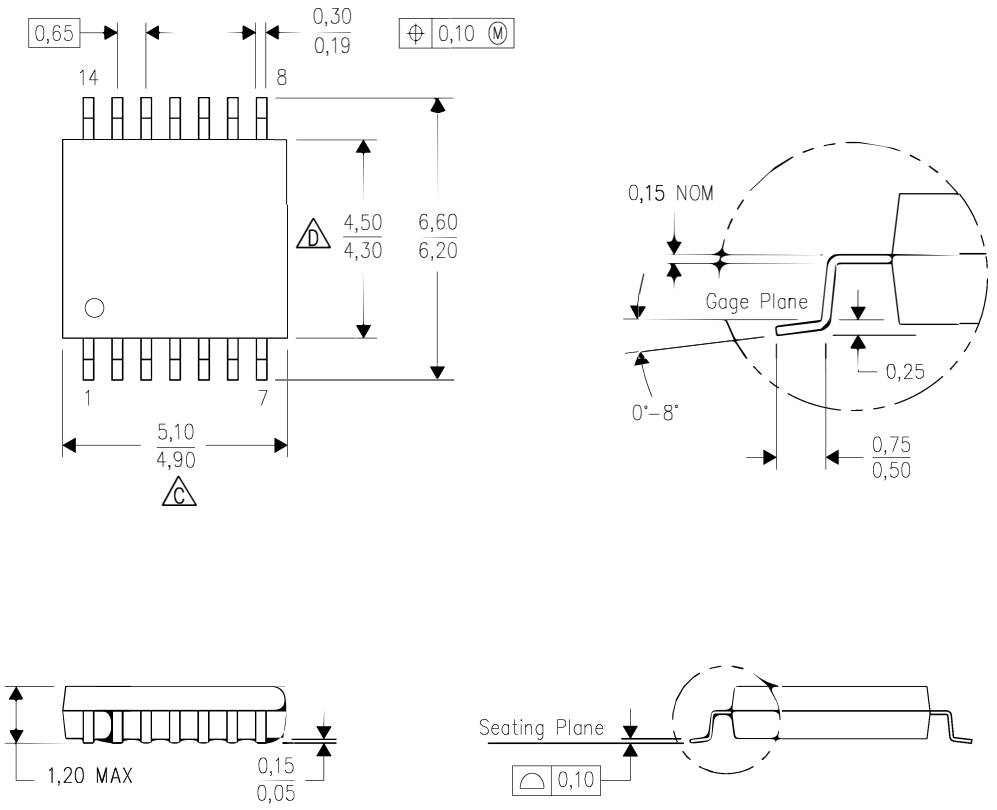
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

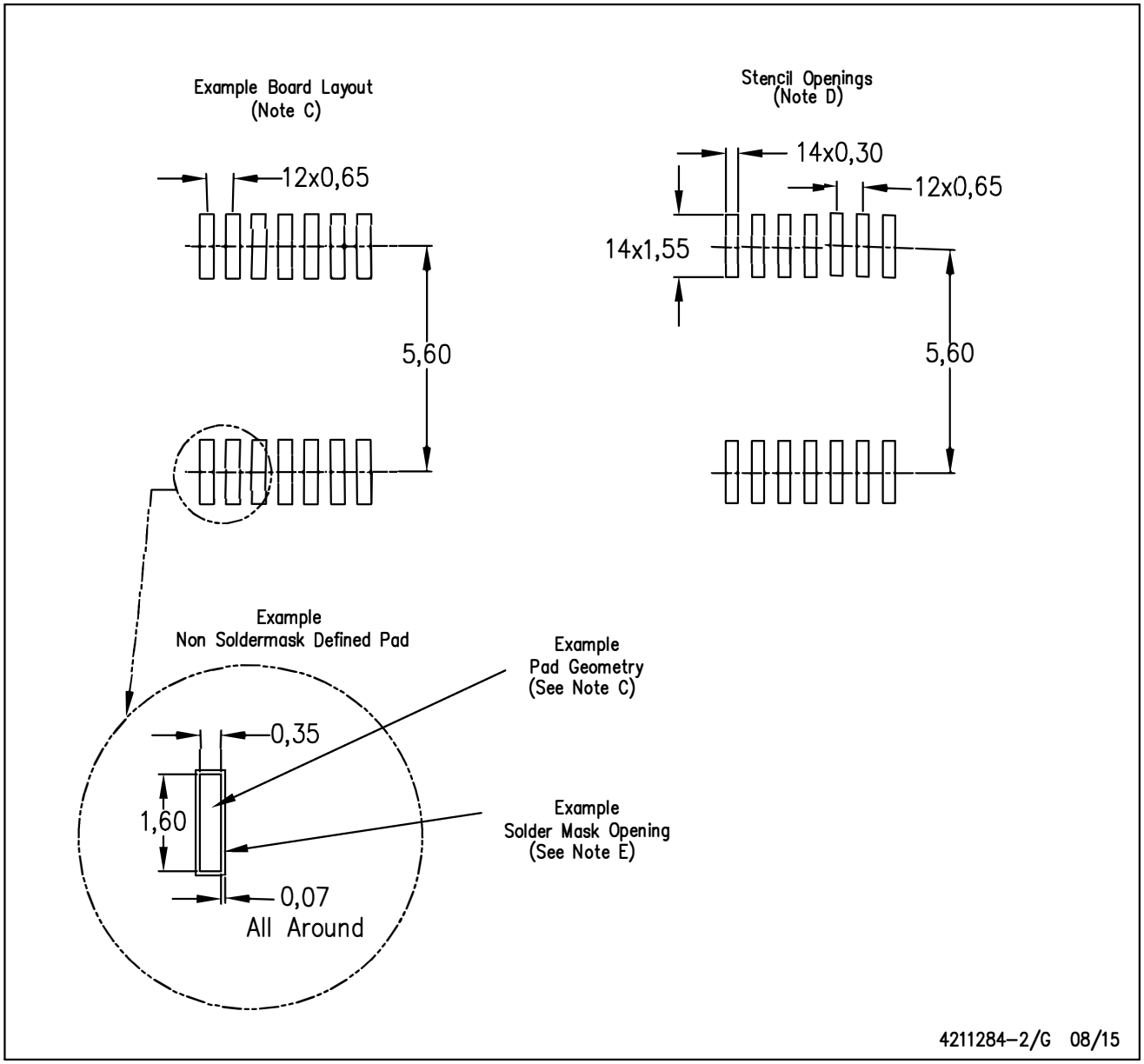
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



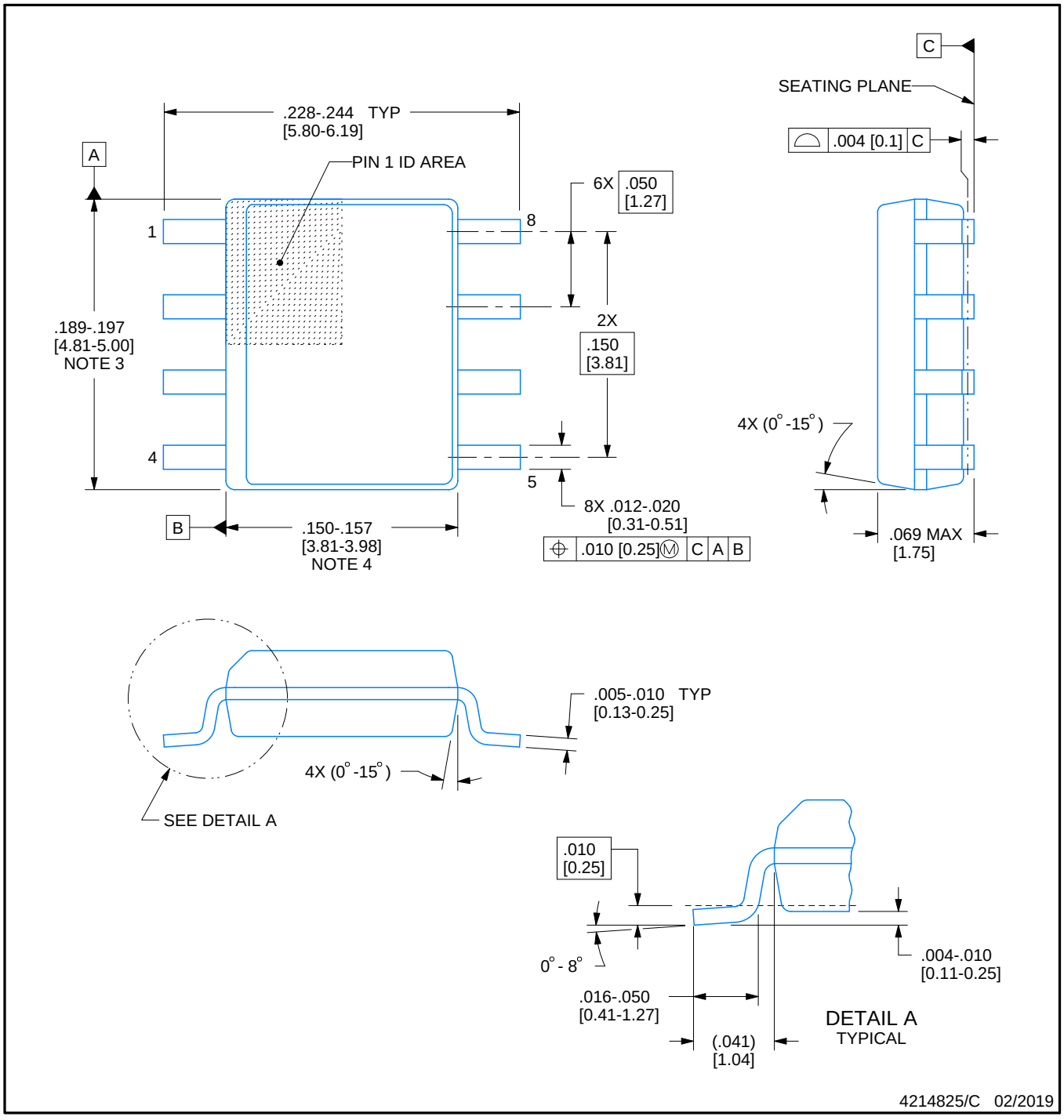
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

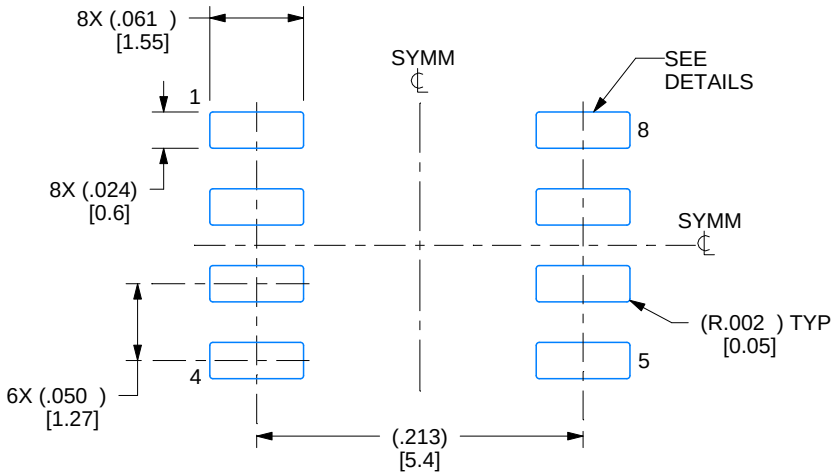
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

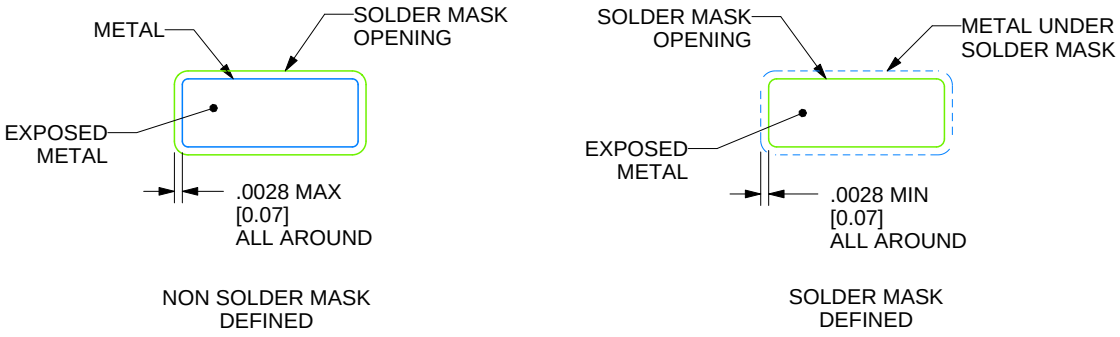
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

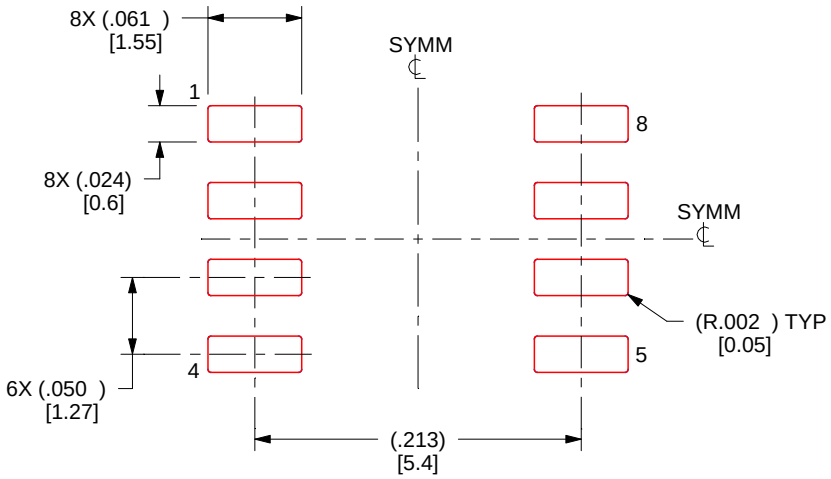
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.