SGM61606-ADJQ
Automotive 4V to 60V Input, 600mA Output Non-Synchronous Buck Converter

GENERAL DESCRIPTION

The SGM61606-ADJQ is a non-synchronous Buck converter with a wide input range from 4V to 60V and 600mA output current capability. This device can be easily used in various automotive applications powered from unregulated sources.

The SGM61606-ADJQ features 2.1MHz operating frequency, which is suitable for small solution size. It operates in pulse frequency modulation (PFM) mode at light load to boost light load efficiency. Moreover, the low 33μA (TYP) quiescent current and low shutdown current of only 1.2μA (TYP) make it a suitable choice for battery-powered applications.

The internal soft-start and loop compensation simplify the external components design and save users time and cost. Protection features include cycle-by-cycle current limit, thermal shutdown with auto recovery and output over-voltage protection.

The device is AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and it is suitable for automotive applications.

The SGM61606-ADJQ is available in a Green TSOT-23-6 package.

FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
  Device Temperature Grade 1
  T_A = -40℃ to +125℃
- **Wide 4V to 60V Input Voltage Range**
- **Up to 600mA Output Current**
- **Ultra-Low Quiescent Current: 33μA (TYP)**
- **Low Shutdown Current: 1.2μA (TYP)**
- **97% Maximum Duty Cycle**
- **2.1MHz Fixed Switching Frequency**
- **Internal Compensation**
- **Precision Enable**
- **Cycle-by-Cycle Current Limit Protection**
- **Thermal Shutdown with Auto Recovery**
- **Output Over-Voltage Protection**
- **Available in a Green TSOT-23-6 Package**

APPLICATIONS

Automotive Distributed Power Systems
Body Electronics and Lighting
Infotainment and Cluster
Advanced Driver Assistance Systems (ADAS)

代理商 威尔逊 www.visvie.com 联系电话 138 2526 5270

SIMPLIFIED SCHEMATIC

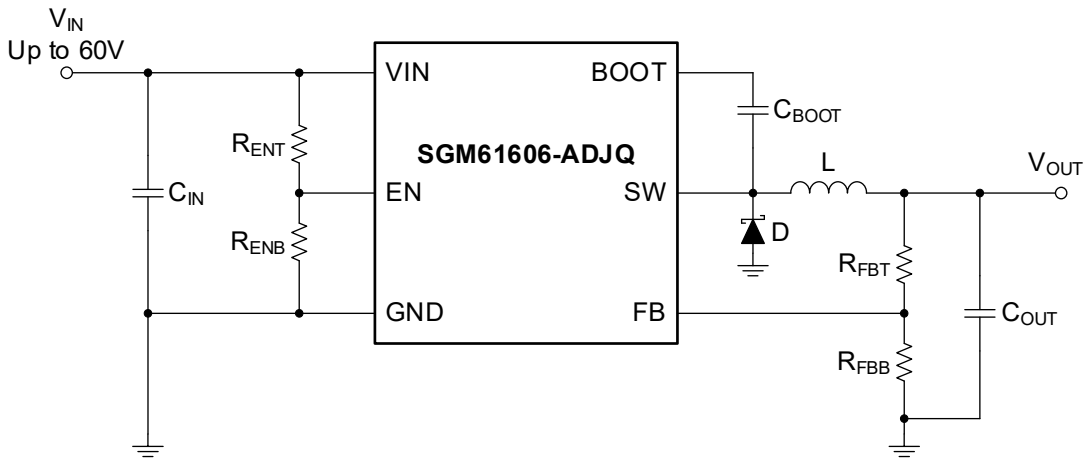


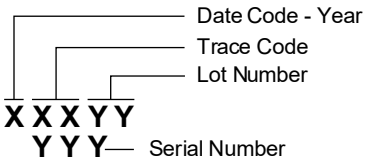
Figure 1. Simplified Schematic

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61606-ADJQ	TSOT-23-6	-40℃ to +125℃	SGM61606-ADJQTN6G/TR	XXXYY 20N	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXX = Date Code, Trace Code. YY = Lot Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltages
- VIN to GND ..... -0.3V to 65V
- EN to GND ..... -0.3V to 65V
- FB to GND ..... -0.3V to 6V
- BOOT to SW ..... -0.3V to 6V

Output Voltages
- SW to GND ..... -3V to 65V

Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1500V

NOTES:

1. For human body model (HBM), all pins comply with AEC-Q100-002 specification.

2. For charged device model (CDM), all pins comply with AEC-Q100-011 specification.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

RECOMMENDED OPERATING CONDITIONS

Buck Converter
- VIN to GND ..... 4V to 60V
- BOOT to SW ..... -0.3V to 6V
- SW to GND ..... -1V to 60V
- FB to GND ..... 0V to 5.5V

Control
- EN to GND ..... 0V to 60V

Operating Junction Temperature Range ..... -40℃ to +125℃

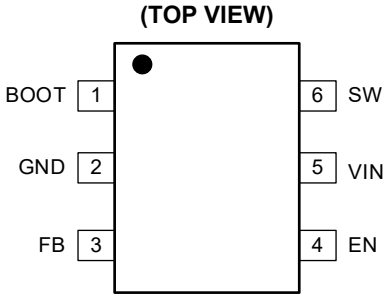
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	BOOT	P	Bootstrap Pin. Bootstrap supply for high-side driver. Connect a 0.1μF ceramic capacitor between BOOT and SW pins.
2	GND	G	Ground.
3	FB	I	Feedback Pin for Setting the Output Voltage. Tap an output feedback resistor divider to this pin. VOUT should be equal to $V_{FB} \times (1 + (R_{FBT}/R_{FBB}))$.
4	EN	I	Active High Enable Input. Float the EN pin to enable the device. Input UVLO level can be programmed using a resistor divider from VIN pin.
5	VIN	P	Supply Input. Connect VIN to a power source with 4V to 60V voltage range. Decouple VIN to GND as close as possible with a high frequency, low ESR ceramic capacitor (X5R or higher grade is recommended).
6	SW	P	Switching Node. Connection point of the internal upper power MOSFET and refresh MOSFET. Connect this pin to the output inductor, the bootstrap capacitor and the Schottky diode.

NOTE: I = input, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VIN (Input Power Supply)						
Input Voltage Range	V_{IN}		4		60	V
Under-Voltage Lockout Thresholds	V_{UV_H}	Rising threshold		3.7	4	V
	V_{UV_L}	Falling threshold	3	3.3		
Supply Current						
Shutdown Supply Current	I_{SD}	V_{IN} current, V_{EN} = 0V		1.2	6	μA
Operating Quiescent Current (Non-Switching)	I_Q	V_{IN} current, V_{EN} = 2V, V_{FB} = 1V		33		μA
EN						
EN Threshold Voltage	V_{EN_H}	Rising threshold	1.1	1.2	1.3	V
	V_{EN_L}	Falling threshold	1.05	1.15	1.25	
EN Pin Current	I_{EN_H}	V_{EN} = V_{EN_H} + 0.05V		4.3		μA
	I_{EN_L}	V_{EN} = V_{EN_L} - 0.05V		0.9		
EN Current Hysteresis	I_{EN_HYS}			3.4		μA
MOSFET						
High-side Switch On-Resistance	R_{DSON}	V_{IN} = 12V, BOOT to SW = 4.5V		950		mΩ
Reference Voltage						
Reference Voltage	V_{REF}		0.746	0.764	0.782	V
FB Leakage Current	I_{FB}	V_{FB} = 1V		20		nA
Current Limit						
Peak Current Limit	I_{LIMIT}	V_{IN} = 12V, T_J = +25℃	910	1100	1270	mA
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD} (1)			170		℃
Hysteresis	T_{HYS} (1)			20		℃
SW (SW Pin)						
Switching Frequency	f_{SW}		1.7	2.1	2.5	MHz
Minimum Turn-On Time	t_{ON_MIN} (1)	f_{SW} = 2.1MHz		80		ns
Maximum Duty Cycle	D_{MAX} (1)			97		%

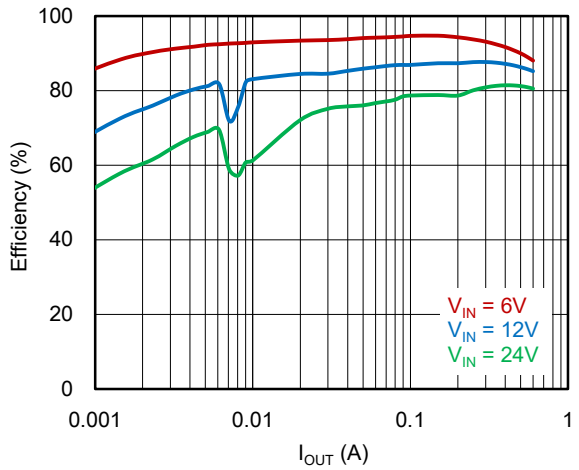
NOTE:

1. Guaranteed by design, not tested in production.

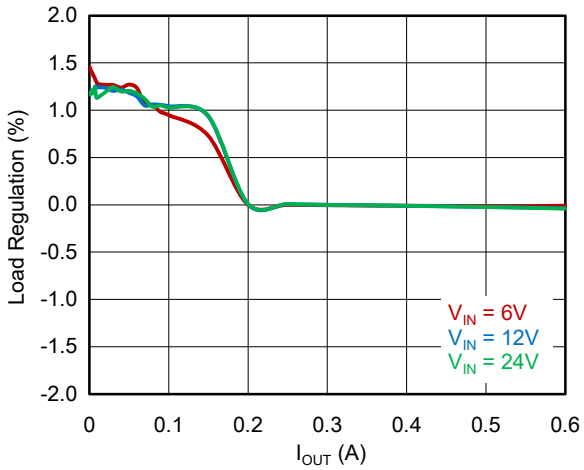
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, L = 10μH (DCR = 35.4mΩ) and C_{OUT} = 10μF, unless otherwise noted.

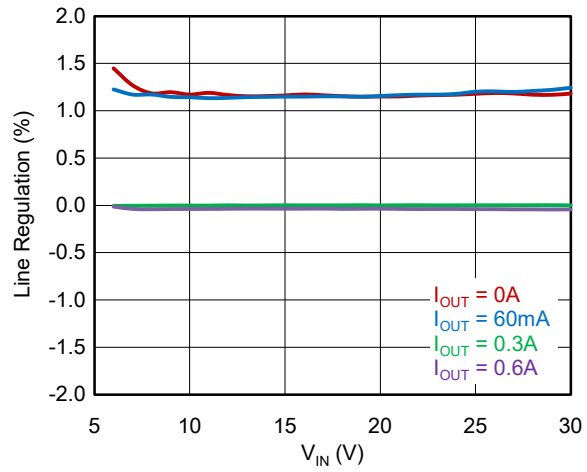
Efficiency vs. I_{OUT}



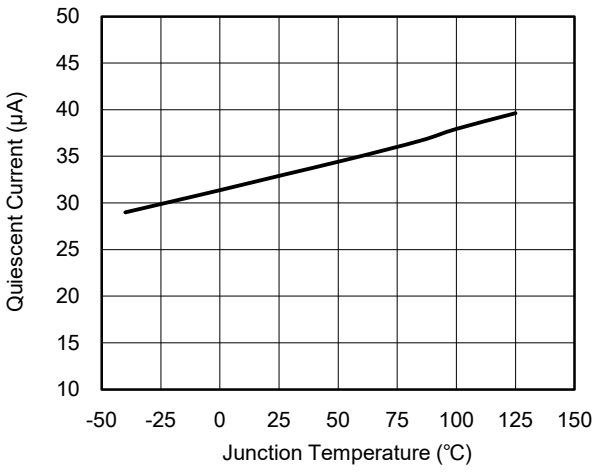
Load Regulation



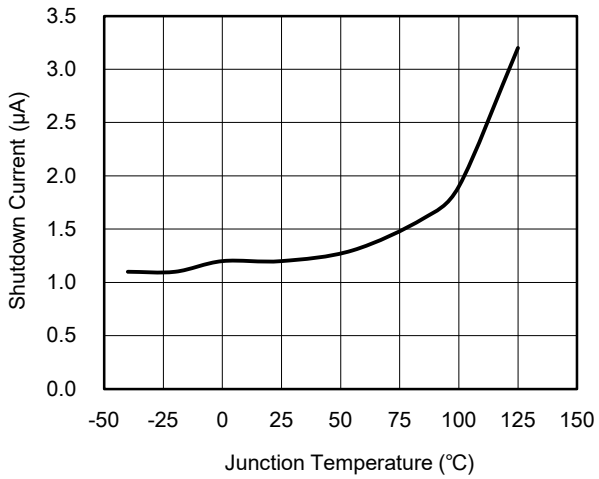
Line Regulation



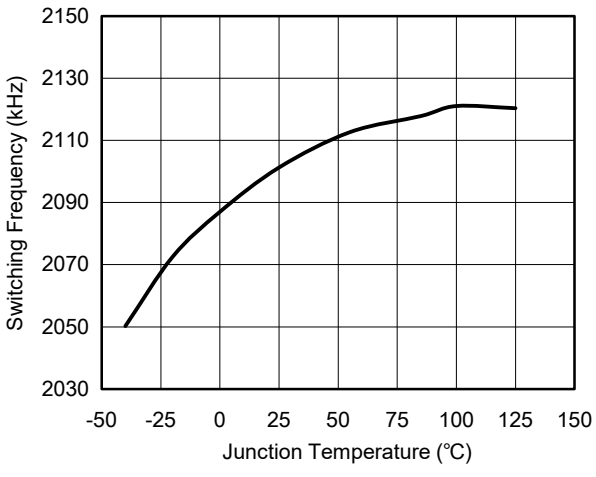
Quiescent Current vs. Junction Temperature



Shutdown Current vs. Junction Temperature



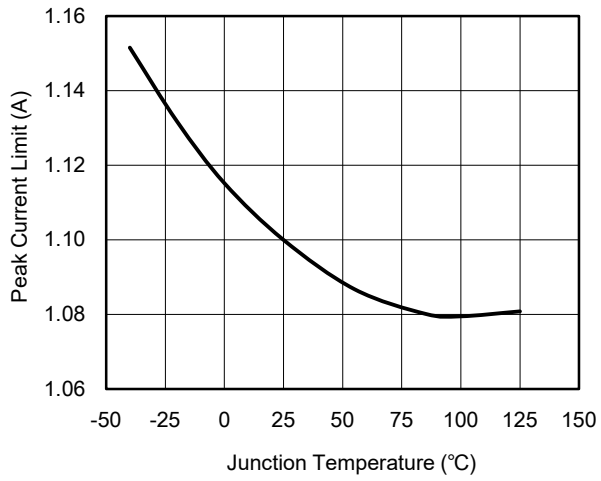
Switching Frequency vs. Junction Temperature



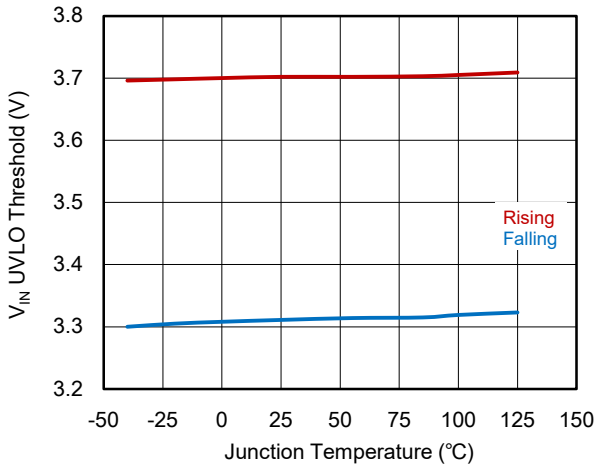
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, L = 10μH (DCR = 35.4mΩ) and C_{OUT} = 10μF, unless otherwise noted.

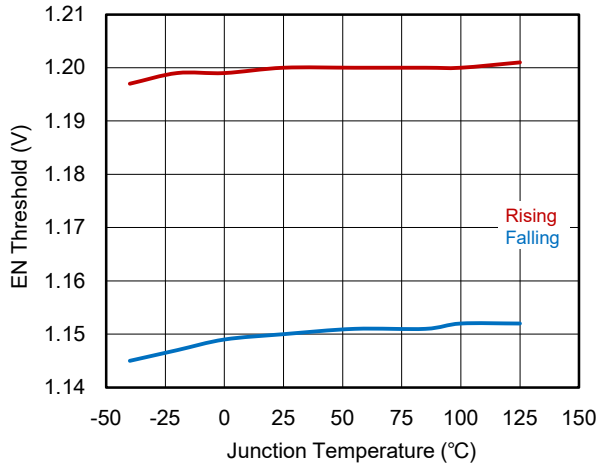
Peak Current Limit vs. Junction Temperature



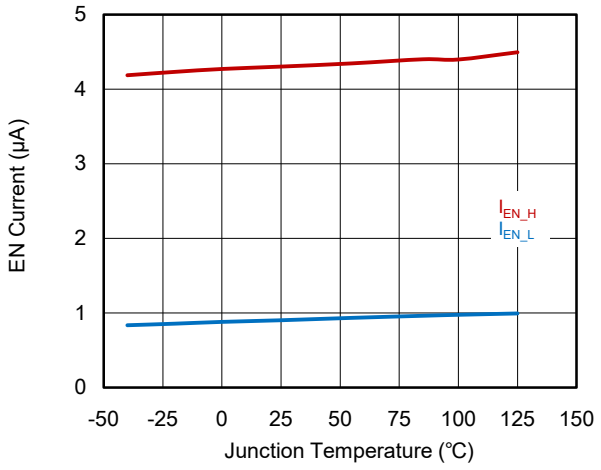
V_{IN} UVLO Threshold vs. Junction Temperature



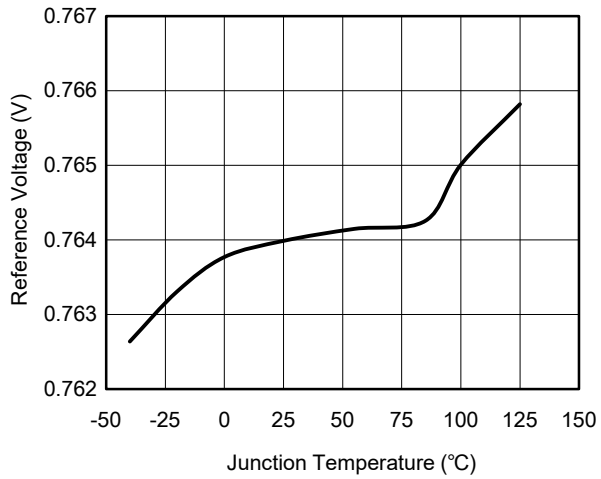
EN Threshold vs. Junction Temperature



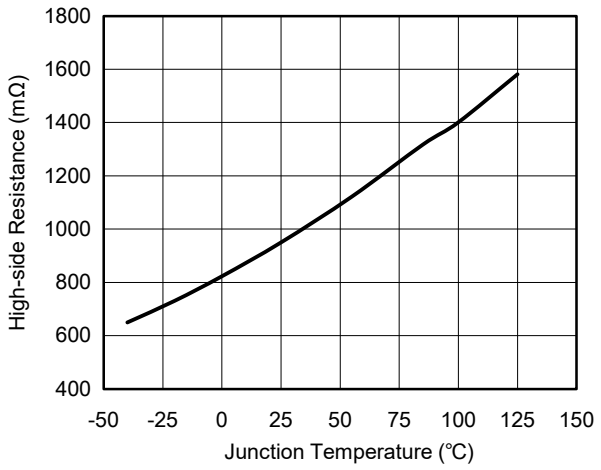
EN Current vs. Junction Temperature



Reference Voltage vs. Junction Temperature



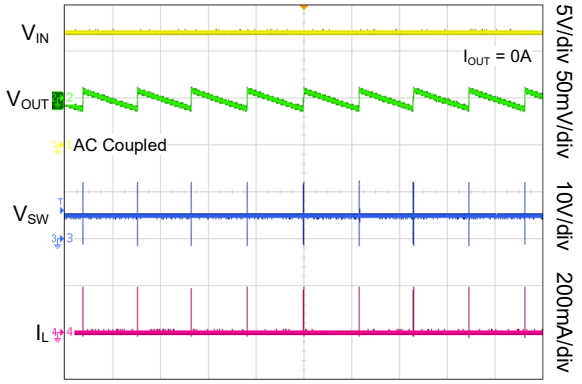
High-side Resistance vs. Junction Temperature



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

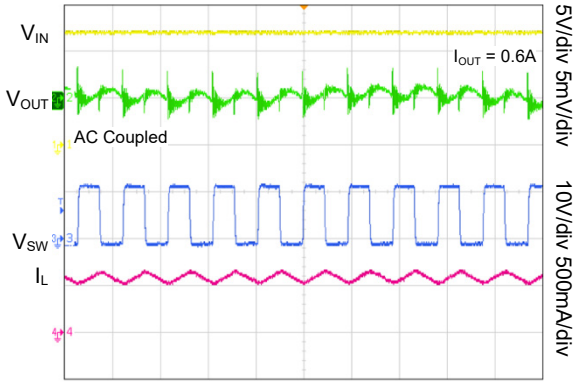
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, L = 10μH (DCR = 35.4mΩ) and C_{OUT} = 10μF, unless otherwise noted.

Output Voltage Ripple



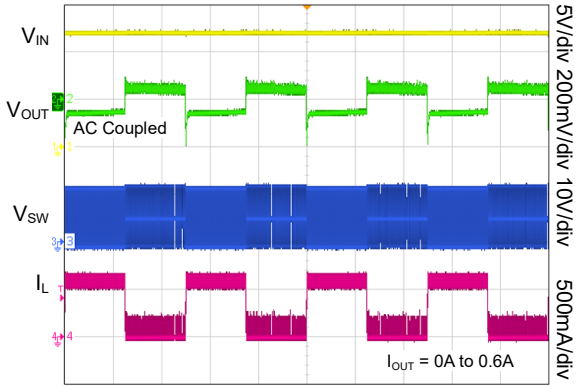
Time (2ms/div)

Output Voltage Ripple



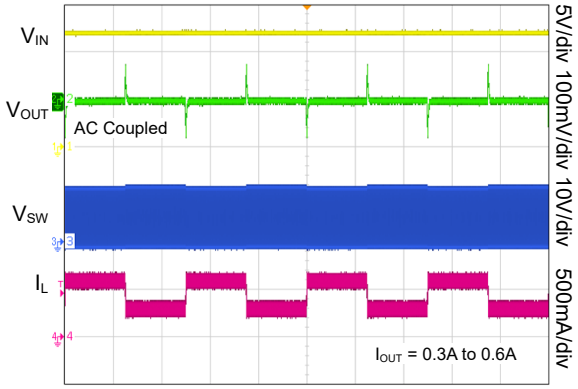
Time (500ns/div)

Load Transient



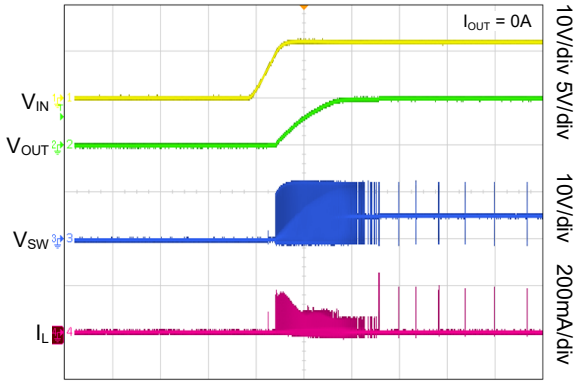
Time (2ms/div)

Load Transient



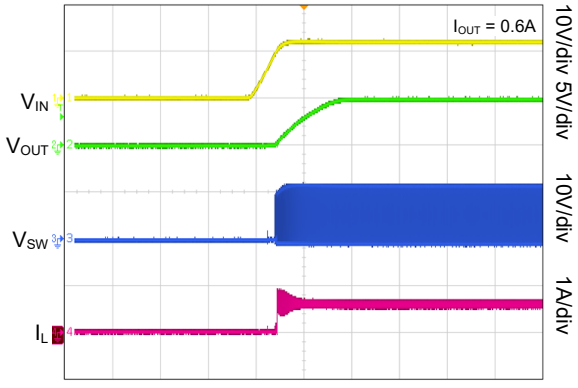
Time (2ms/div)

Start-Up by VIN



Time (2ms/div)

Start-Up by VIN

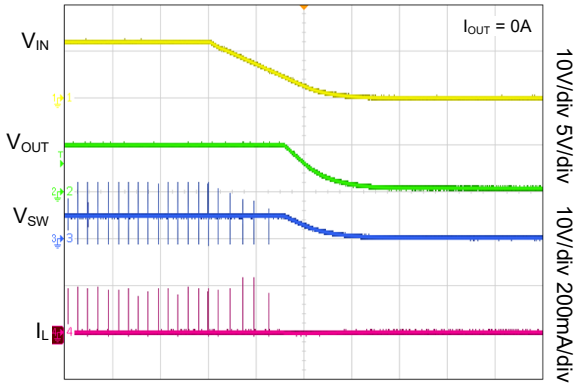


Time (2ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

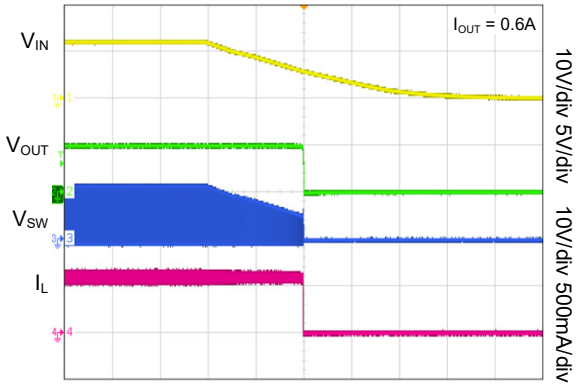
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, L = 10μH (DCR = 35.4mΩ) and C_{OUT} = 10μF, unless otherwise noted.

Shutdown by VIN



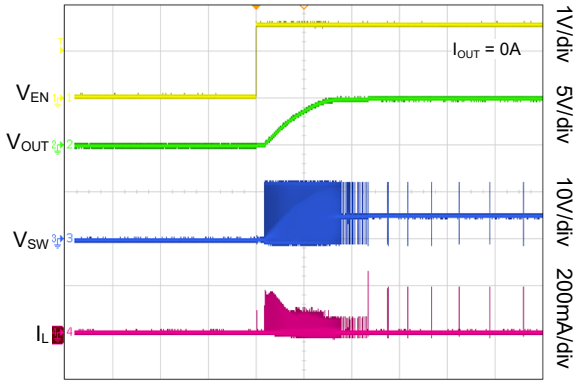
Time (10ms/div)

Shutdown by VIN



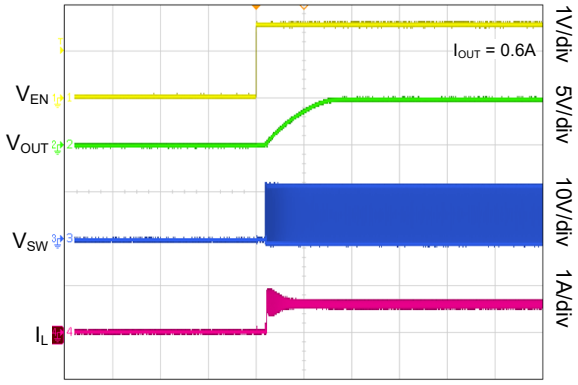
Time (5ms/div)

Start-Up by EN



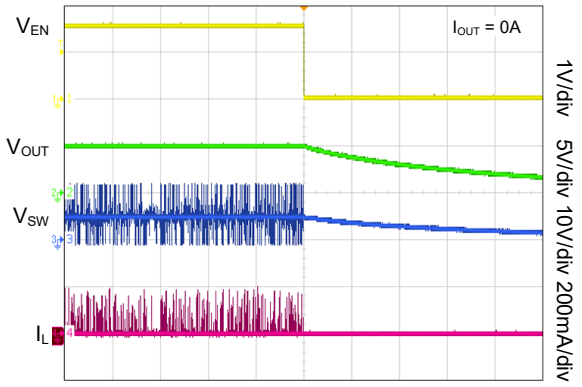
Time (2ms/div)

Start-Up by EN



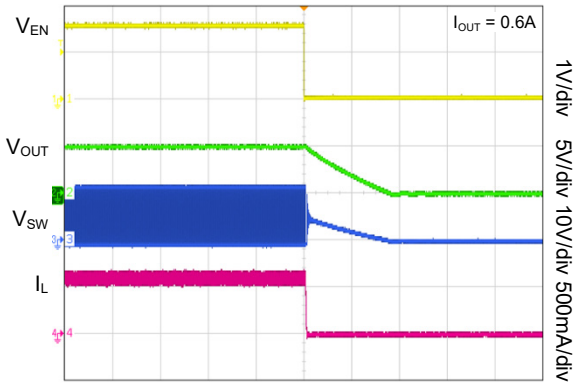
Time (2ms/div)

Shutdown by EN



Time (200ms/div)

Shutdown by EN

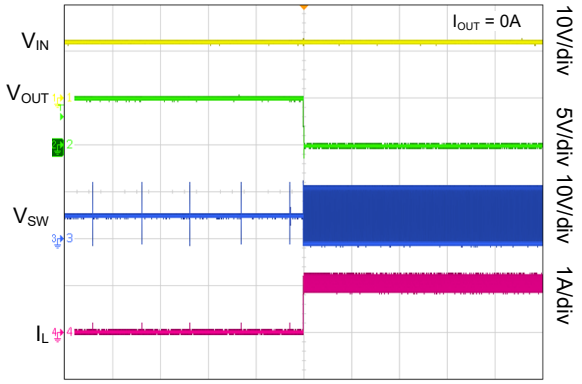


Time (50μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

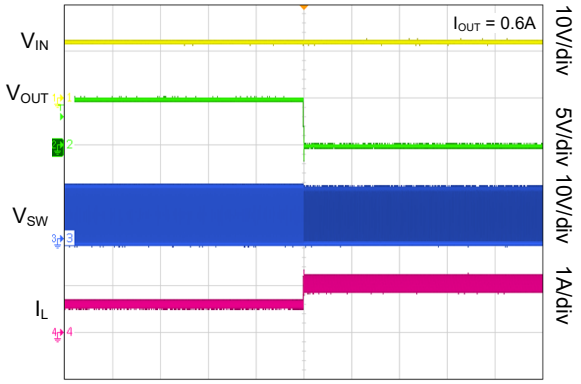
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, L = 10μH (DCR = 35.4mΩ) and C_{OUT} = 10μF, unless otherwise noted.

Short-Circuit Entry



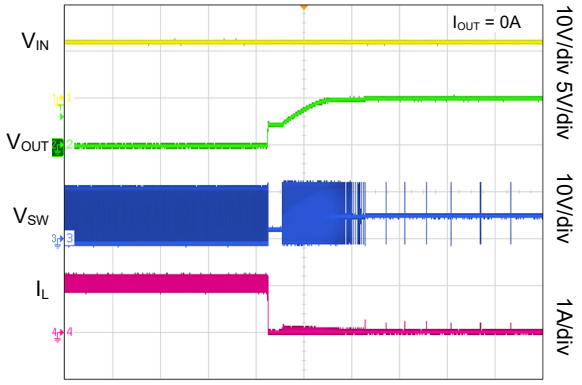
Time (2ms/div)

Short-Circuit Entry



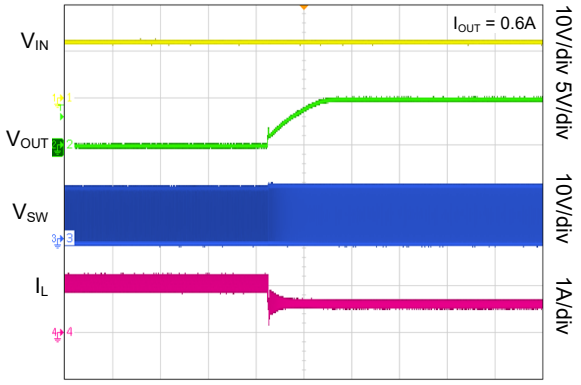
Time (2ms/div)

Short-Circuit Recovery



Time (2ms/div)

Short-Circuit Recovery



Time (2ms/div)

FUNCTIONAL BLOCK DIAGRAM

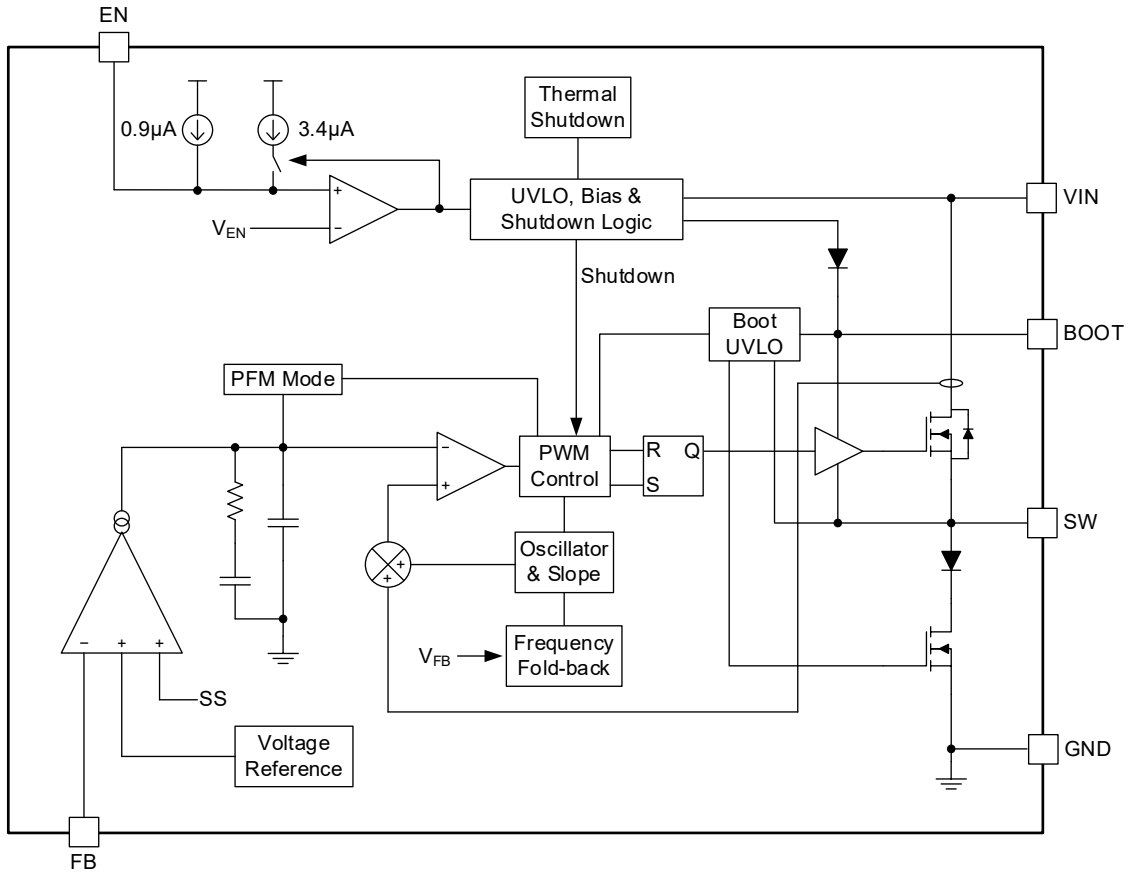


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61606-ADJQ device is an internally compensated peak current mode controlled non-synchronous Buck converter with operation voltage up to 60V. The SGM61606-ADJQ implements a constant 2.1MHz switching frequency control. The SGM61606-ADJQ has a very low non-switching quiescent current (33μA TYP). The integrated high-side MOSFET driver voltage is biased by a capacitor on the BOOT to SW pin. The boot UVLO circuit will turn the internal refresh MOSFET on to recharge the BOOT capacitor when the BOOT-SW voltage falls below a preset threshold. Internal soft-start can suppress inrush currents.

Enable and VIN Under-Voltage Lockout

The EN pin can be used to turn the device on and off or to change the UVLO thresholds. The device is enabled when the EN pin voltage exceeds its high threshold. A low EN voltage disables the device and brings it to the shutdown state.

The EN pin is internally pulled up by a small current source (I_{EN_L}) so the device is enabled if EN pin is floated. An open-drain or open collector output can be used to control the EN pin.

V_{IN} is monitored by the internal under-voltage lockout circuit and if it is below UVLO threshold, the device is disabled. The internal UVLO has a 400mV hysteresis. If higher thresholds are needed, EN pin can be used as shown in Figure 3.

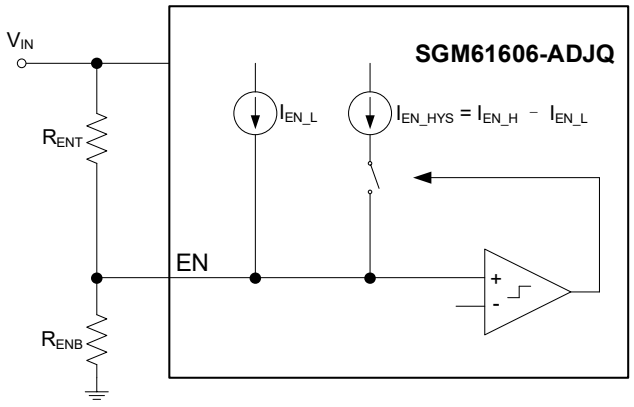


Figure 3. Adjustable VIN Under-Voltage Lockout

The EN pull-up current is used to set the hysteresis. The pull-up current is increased by I_{EN_H} - I_{EN_L} when the EN pin exceeds its high threshold. Use Equations 1 and 2 to calculate the R_{ENT} and R_{ENB} values for the desired UVLO low (V_{UV_L}) and high (V_{UV_H}) thresholds.

$$R_{ENT} = \frac{V_{UV_H} \times V_{EN_L} - V_{UV_L} \times V_{EN_H}}{I_{EN_H} \times V_{EN_H} - I_{EN_L} \times V_{EN_L}} \quad (1)$$

$$R_{ENB} = \frac{R_{ENT} \times V_{EN_L}}{V_{UV_L} - V_{EN_L} + R_{ENT} \times I_{EN_H}} \quad (2)$$

where:

I_{EN_L} = 0.9μA (TYP)

I_{EN_H} = 4.3μA (TYP)

V_{EN_L} = 1.15V (TYP)

V_{EN_H} = 1.2V (TYP)

Bootstrap Voltage (BOOT)

To power the upper switch gate driver, a voltage higher than VIN is needed. Bootstrap technique is used to provide this voltage from the switching node by using a 0.1μF bootstrap capacitor between SW and BOOT pins along with an internal bootstrap diode. The voltage is internally regulated for driving the high-side switch. An X5R or X7R ceramic capacitor is recommended for C_{BOOT} to have stable capacitance against temperature and voltage variations. If the voltage between BOOT and SW nodes falls below BOOT UVLO threshold (2.8V TYP), the internal refresh MOSFET will be turned on to recharge the BOOT capacitor.

Internal Voltage Reference and Soft-Start

The SGM61606-ADJQ device has an internal 0.764V reference (V_{REF}) to program the output at the desired level. When the converter starts, an internal ramp voltage begins to rise from near 0V to slightly above 0.764V with a ramp time of 3ms. The lower of V_{REF} and this ramp is used as reference for the error amplifier, therefore, during start-up the ramp provides a soft-start for the output. The soft-start is essential to prevent high inrush currents caused by rapid increase of output voltage across output capacitors and the load.

DETAILED DESCRIPTION (continued)

Peak-Current Mode Control

Figure 4 shows the switching node operating waveforms of the SGM61606-ADJQ. Switching node voltage is generated by controlling the duty cycle of the high-side MOSFET. The high-side duty cycle is used as control parameter of the Buck converter to regulate output voltage and is defined as: $D = t_{ON}/t_{SW}$, where t_{ON} is the high-side MOSFET on-time and t_{SW} is the switching period. When high-side MOSFET is turned on, the SW pin voltage sharply rises towards V_{IN}, and the inductor current (I_L) starts ramping up with (V_{IN} - V_{OUT})/L slope. When high-side MOSFET is turned off, the inductor current freewheels through the external Schottky diode, and I_L ramps down with -V_{OUT}/L slope. In ideal case, the output voltage is proportional to the input voltage and duty cycle ($D = V_{OUT}/V_{IN}$) if component parasitic parameters are ignored.

The SGM61606-ADJQ implements peak-current mode control in continuous conduction mode. In light load conditions, the SGM61606-ADJQ will enter PFM mode to reduce the switching frequency and the associated switching and gate driving losses.

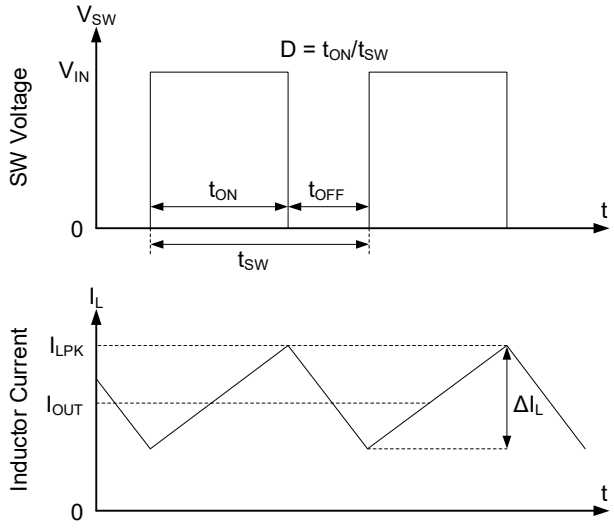


Figure 4. Converter Switching Waveforms in CCM

In continuous conduction mode, SGM61606-ADJQ operates at fixed-frequency using peak-current mode control scheme. Inductor current (I_L) is monitored and when sensed inductor current (I_L) exceeds the COMP (the output of the error amplifier), the high-side MOSFET is turned off. And the inductor current freewheels through the external Schottky diode. High-side MOSFET will not turn on again until a new switching cycle begins.

PFM Mode Control

As the load decreases, the COMP voltage drops. When COMP voltage falls below a preset threshold, the device will enter PFM mode and the COMP voltage is clamped to V_{CLAMP}. After entering PFM for a delay time, some modules are shut down to minimize input current, and the device draws only 33μA (TYP) input quiescent current. The high-side MOSFET will not switch until the FB voltage falls below a low threshold (TYP 101% V_{REF}). Since the integrated current comparator catches the inductor peak-current only, the average load current entering PFM varies with the V_{IN}, V_{OUT}, and external output filters.

Output Voltage Setting

For SGM61606-ADJQ, The output voltage is set by a resistor divider between V_{OUT} and GND that is tapped to the FB pin. It is recommended to use 1% or higher quality resistors with low thermal tolerance for an accurate and thermally stable output voltage.

Use Equation 3 and Figure 5 to calculate the output voltage. Lower divider resistor values increase loss and reduce light load efficiency. Consider larger resistors to improve efficiency at light load, and start with 100kΩ for the upper resistor (R_{FBT}). Note that if R_{FBT} is too high (> 1MΩ), the FB pin leakage current and other noises can easily affect the accuracy and performance of the regulator.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{FBT}}{R_{FBB}}\right) \quad (3)$$

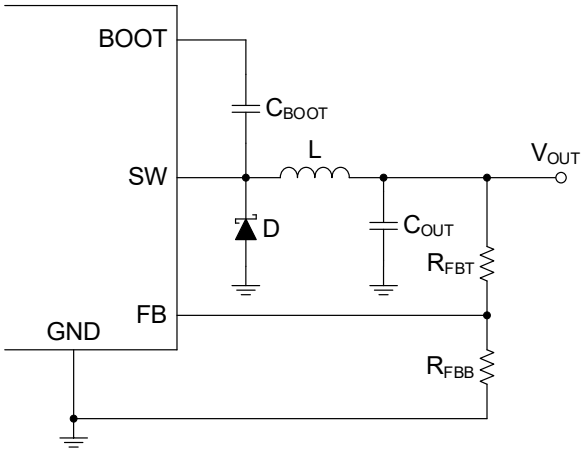


Figure 5. Adjustable Output Voltage

DETAILED DESCRIPTION (continued)

Over-Current Limit Protection

The SGM61606-ADJQ implements peak-current mode control which uses the internal COMP voltage to turn off the high side MOSFET on a cycle-by-cycle basis. In each cycle, the high-side current sensing starts after the high-side MOSFET has been turned on for a short time (blanking time). The sensed high-side MOSFET current is compared with the Error Amplifier (EA) output (V_{COMP}) minus slope compensation. When the peak switch current intersects the V_{COMP}, the high-side MOSFET is turned off. If the output is overload and V_{OUT} drops, the peak current of high-side switch is limited by a maximum peak current I_{LIMIT} when V_{COMP} is higher than I_{LIMIT}.

In the SGM61606-ADJQ, there is frequency fold-back function, which can prevent inductor current from running away. As the feedback voltage falls from 0.764V to 0V, the switching frequency will linearly decrease to the minimum switching frequency.

Output Over-Voltage Protection (OVP)

The SGM61606-ADJQ contains an over-voltage comparator that monitors the FB pin voltage. The over-voltage threshold is approximately 108% of reference voltage (V_{REF}). When the voltage at the FB pin exceeds the over-voltage threshold, PWM switching will be stopped and high-side MOSFET will be turned off. If the over-voltage fault is removed, the regulator will automatically recover.

Thermal Shutdown

If the junction temperature exceeds +170℃ (TYP), the device is forced to stop switching. It will recover automatically when T_J falls below the recovery threshold.

APPLICATION INFORMATION

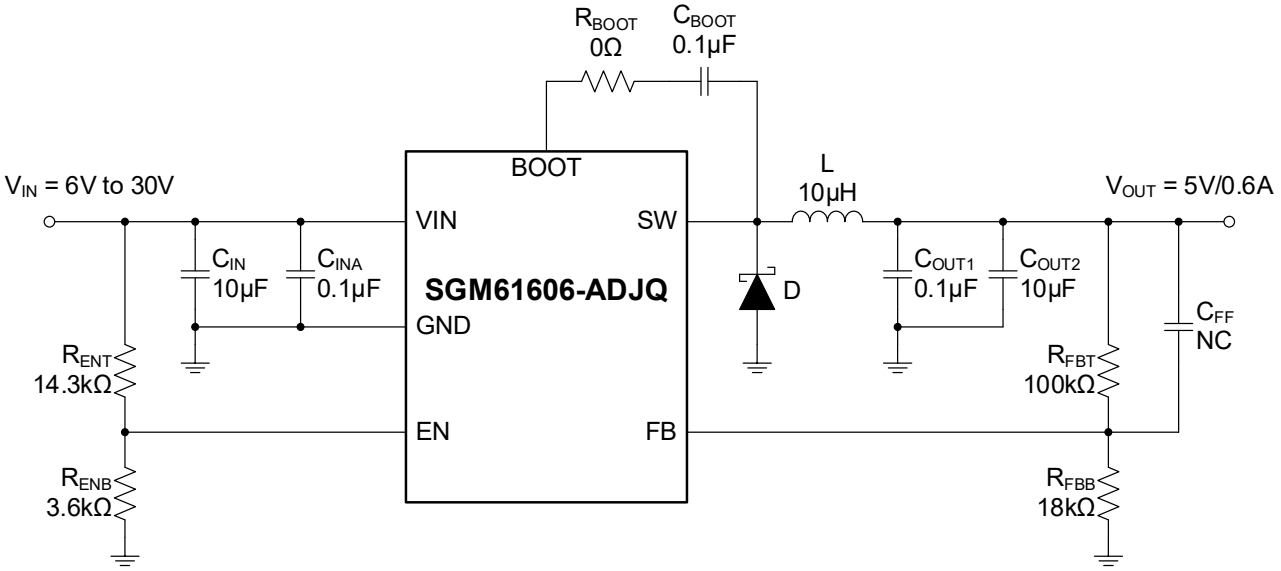


Figure 6. A Reference Design for 5V/0.6A Application

The design method and component selection for the SGM61606-ADJQ Buck converter is explained in this section. Schematic of a basic design is shown in Figure 6. Only a few external components are needed to provide a constant output voltage from a wide input voltage range.

The external components are designed based on the application requirements and device stability. Some suitable output filters (L and C_{OUT}) and divider resistor values are provided in Table 1 to simplify component selection.

Table 1. Recommended Component Values

f_{SW} (MHz)	V_{OUT} (V)	L (μH)	C_{OUT} (μF)	R_{FBT} (kΩ)	R_{FBB} (kΩ)
2.1	5	10	10	100	18
	12	27	10	100	6.8

Design Requirements

A typical application circuit for the SGM61606-ADJQ as a Buck converter is shown in Figure 6. It is used for converting a 6V to 30V supply voltage to a lower voltage level supply voltage (5V) suitable for the system. The design parameters given in Table 2 are used for this design example.

Table 2. Design Parameters

Design Parameters	Example Values
Input Voltage	12V (TYP), 6V to 30V
Start Input Voltage (Rising V_{IN})	6V
Stop Input Voltage (Falling V_{IN})	5.7V
Output Voltage	5V
Output Voltage Ripple	50mV, 1% of V_{OUT}
Transient Response, 0.3A to 0.6A Load Step	250mV, 5% of V_{OUT}
Output Current Rating	0.6A
Operation Frequency	2.1MHz

Input Capacitor Selection

A high-quality ceramic capacitor (X5R or X7R or better dielectric grade) must be used for input decoupling of the SGM61606-ADJQ. The VIN capacitor ripple current rating must be greater than the maximum input current ripple. The input current ripple can be calculated using Equation 4 and the maximum value occurs at 50% duty cycle. Using the design example values, I_{OUT} = 0.6A, yields an RMS input ripple current of 0.3A.

$$I_{CIN_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \frac{(V_{IN} - V_{OUT})}{V_{IN}}} = I_{OUT} \times \sqrt{D \times (1-D)} \quad (4)$$

APPLICATION INFORMATION (continued)

For this design, a ceramic capacitor with at least 50V voltage rating is required to support the maximum input voltage. So, a 10μF/50V capacitor is selected for VIN to cover all DC bias, thermal and aging de-ratings. The input capacitance determines the regulator input voltage ripple. This ripple can be calculated from Equation 5. In this example, the total effective capacitance of the 10μF/50V capacitor is around 4μF at 12V input, and the input voltage ripple is 17mV.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1-D)}{C_{IN} \times f_{SW}} \quad (5)$$

It is recommended placing an additional small size 0.1μF ceramic capacitor right beside VIN and GND pins for high frequency filtering.

Inductor Selection

Equation 6 is conventionally used to calculate the output inductance of a Buck converter. The ratio of inductor current ripple (ΔI_L) to the maximum output current (I_{OUT}) is represented as K_{IND} factor ($\Delta I_L/I_{OUT}$). The inductor ripple current is bypassed and filtered by the output capacitor and the inductor DC current is passed to the output. Inductor ripple is selected based on a few considerations. The peak inductor current (I_{OUT} + $\Delta I_L/2$) must have a safe margin from the saturation current of the inductor in the worst-case conditions especially if a hard-saturation core type inductor (such as ferrite) is chosen. The ripple current also affects the selection of the output capacitor. C_{OUT} RMS current rating must be higher than the inductor RMS ripple. Typically, a 30% ripple is selected (K_{IND} = 0.3).

$$L = \frac{V_{IN_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN_MAX} \times f_{SW}} \quad (6)$$

In this example, the calculated inductance will be 11.02μH with K_{IND} = 0.3, so the nearest inductance of 10μH is selected. The ripple, RMS and peak inductor current calculations are summarized in Equations 7, 8 and 9 respectively.

$$\Delta I_L = \frac{V_{IN_MAX} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{IN_MAX} \times f_{SW}} \quad (7)$$

$$I_{L_RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}} \quad (8)$$

$$I_{L_PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (9)$$

Note that during start-up, load transients or fault conditions, the peak inductor current may exceed the calculated I_{L_PEAK}. Therefore, it is always safer to choose the inductor saturation current higher than the switch current limit.

Output Capacitor Selection

The output capacitors and inductor filter the AC part of the PWM switching voltage and provide an acceptable level of output voltage ripple superimposed on the desired output DC voltage. Additionally, the capacitors store energy to assist in maintaining output voltage regulation during load transient. The output voltage ripple (ΔV_{OUT}) depends on the output capacitor value at the operating voltage, temperature and its parasitic parameters (ESR and ESL):

$$\Delta V_{OUT} = \Delta I_L \times ESR + \frac{V_{IN} - V_{OUT}}{L} \times ESL + \frac{\Delta I_L}{8 \times f_{SW} \times C_{OUT}} \quad (10)$$

The voltage rating of the output capacitors should be selected with enough margins to ensure that capacitance drop (voltage and temperature de-rating) is not significant. The type of output capacitors will determine which terms of Equation 10 are dominant. For ceramic output capacitors, the ESR and ESL are virtually zero, so the output voltage ripple will be dominated by the capacitive term.

To reduce the voltage ripple, either inductance or the total capacitance is increased. For electrolytic output capacitors, the value of capacitance is relatively high, and compared with ESR and ESL terms, the third term in Equation 10 can be ignored:

Higher quality capacitors, larger inductance or using parallel capacitors can help reduce the output ripple in a design using electrolytic output capacitors.

APPLICATION INFORMATION (continued)

The ESR of some commercial electrolytic capacitors can be quite high, and it is recommended using quality capacitors with the ESR or the total impedance clearly documented in the datasheet. ESR of an electrolytic capacitor may increase significantly at cold ambient temperatures with a factor of 10 or so, which increases the ripple and can deteriorate the regulator stability.

The design of the output capacitor typically satisfies the typical 1% ripple requirement. The appropriate output capacitor value can be selected through calculations based on the capacitor ripple and ESR ripple. However, in scenarios involving low voltage, it is crucial to consider the overshoot and undershoot of the output voltage during load transient. Therefore, the design of the output capacitor must always take into account the load transient response. Equation 11 and Equation 12 calculate the minimum capacitor required to keep the output voltage overshoot or undershoot to a desired value.

$$C_{OUT} > \frac{L \times I_{STEP}^2}{2 \times V_{UNDER} \times D_{max} \times (V_{IN} - V_{OUT})} \quad (11)$$

$$C_{OUT} > \frac{L \times I_{STEP}^2}{2 \times V_{OVER} \times V_{OUT}} \quad (12)$$

Where:

V_{OVER} is the output overshoot during load transient from full load to half load.

V_{UNDER} is the output undershoot during load transient from half load to full load.

I_{STEP} is the magnitude of the load step change.

In this case according to Table 2, a 10μF/25V X5R ceramic capacitor in parallel with a 0.1μF/25V X5R ceramic capacitor can meet the above conditions.

External Diode

An external power diode between the SW and GND pins is needed by the SGM61606-ADJQ to complete the converter. This diode must tolerate the application's absolute maximum ratings. The reverse blocking voltage must be higher than V_{IN_MAX} and its peak current must be above the maximum inductor current. Choose a diode with small forward voltage drop for higher efficiency. Typically, diodes with higher voltage and current ratings have higher forward voltages. A diode with a minimum of 60V reverse voltage is preferred to allow input voltage transients up to the rated voltage of the SGM61606-ADJQ.

Bootstrap Capacitor Selection

Use a 0.1μF high-quality ceramic capacitor (X5R or X7R) with 10V or higher voltage rating for the bootstrap capacitor (C_{BOOT}).

VIN UVLO Setting

The input UVLO can be programmed by using an external voltage divider on the EN pin of the SGM61606-ADJQ. In this design, R_{ENT} is connected between VIN pin and EN pin and R_{ENB} is connected between EN pin and GND (see Figure 6). The UVLO has two thresholds, one for power-up (turn-on) when the input voltage is rising and one for power-down (turn-off) when the voltage is falling. In this design, the turn-on (enable to start switching) occurs when V_{IN} rises above 6V (UVLO rising threshold). When the regulator is working, it will not stop switching (disabled) until the input falls below 5.7V (UVLO falling threshold). Equations 1 and 2 are provided to calculate the resistors. For this example, the nearest standard resistor values are R_{ENT} = 14.3kΩ and R_{ENB} = 3.6kΩ.

Output Voltage Setting

Use an external resistor divider (R_{FBT} and R_{FBB}) to set the output voltage using Equation 13:

$$R_{FBB} = R_{FBT} \times \frac{V_{REF}}{V_{OUT} - V_{REF}} \quad (13)$$

where V_{REF} = 0.764V is the internal reference. For example, by choosing R_{FBT} = 100kΩ, the R_{FBB} value for 5V output will be calculated as 18.04kΩ, a standard value of 18kΩ is selected.

APPLICATION INFORMATION (continued)

Layout Guide

PCB is an essential element of any switching power supply. The converter operation can be significantly disturbed due to the existence of the large and fast rising/falling voltages that can couple through stray capacitances to other signal paths, and also due to the large and fast changing currents that can interact through parasitic magnetic couplings, unless those interferences are minimized and properly managed in the layout design. Insufficient conductance in copper traces for the high current paths results in high resistive losses in the power paths and voltage errors. The following guidelines provided here are necessary to design a good layout:

- Bypass VIN pin to GND pin with low-ESR ceramic capacitors (X5R, X7R or better dielectric) placed as close as possible to VIN pin.
- Use short, wide and direct traces for high-current connections (VIN, SW and GND).
- Keep the BOOT-SW voltage path as short as possible.
- Place the feedback resistors as close as possible to the FB pin that is sensitive to noise.
- Minimize the area and path length of the loop formed by VIN pin, bypass capacitors connections and SW pin.

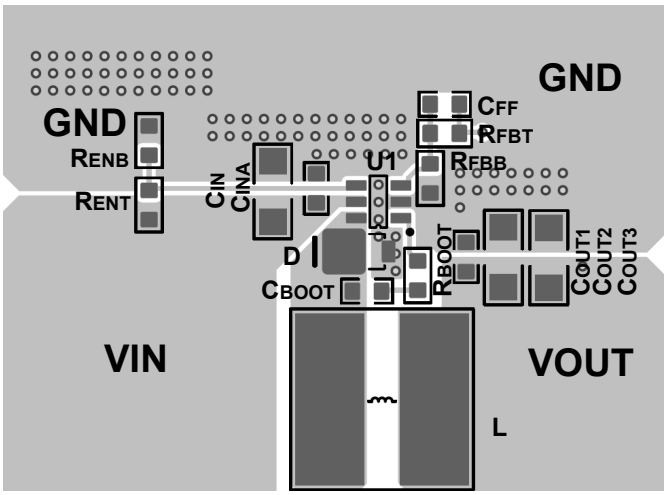


Figure 7. PCB Top Layer

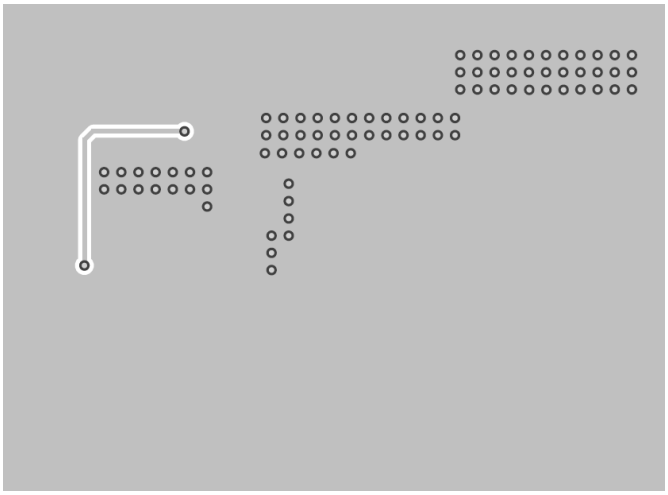


Figure 8. PCB Bottom Layer

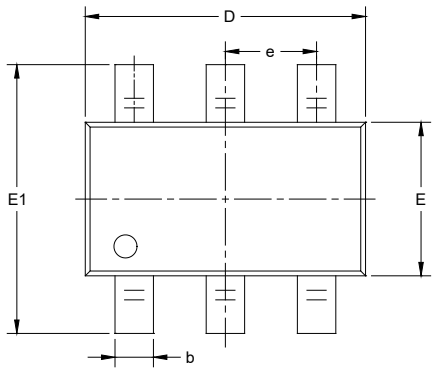
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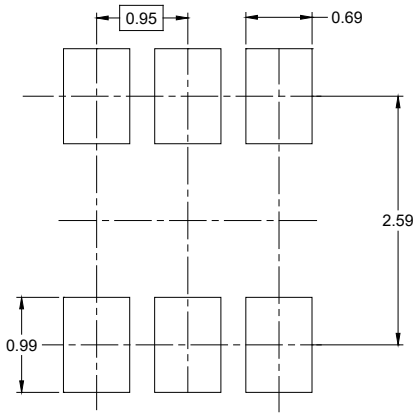
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (JUNE 2026)	Page
Changed from product preview to production data	All

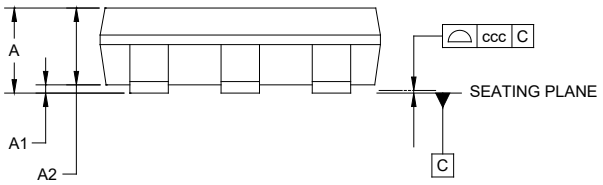
PACKAGE OUTLINE DIMENSIONS

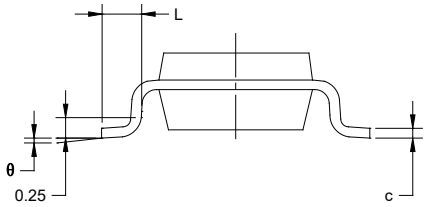
TSOT-23-6





RECOMMENDED LAND PATTERN (Unit: mm)



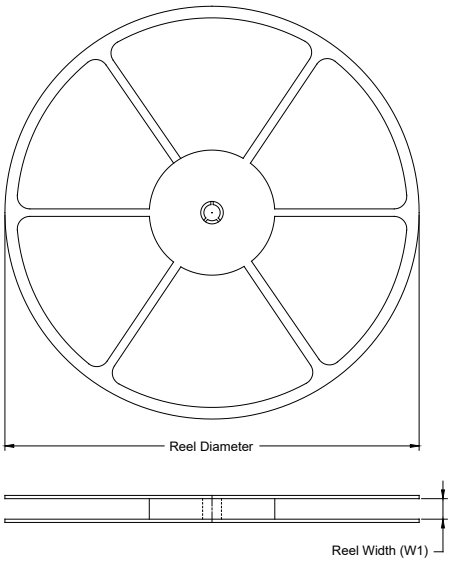


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.100
A1	0.000	-	0.100
A2	0.700		1.000
b	0.300	-	0.500
c	0.080		0.200
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

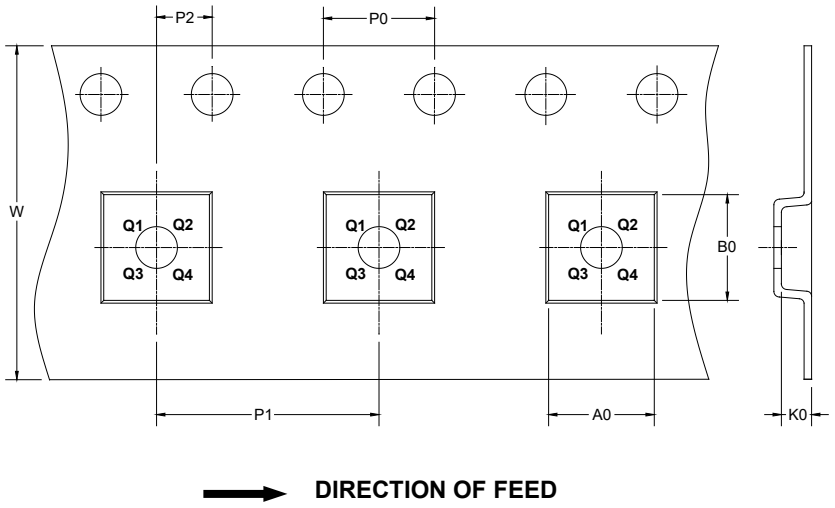
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-193.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



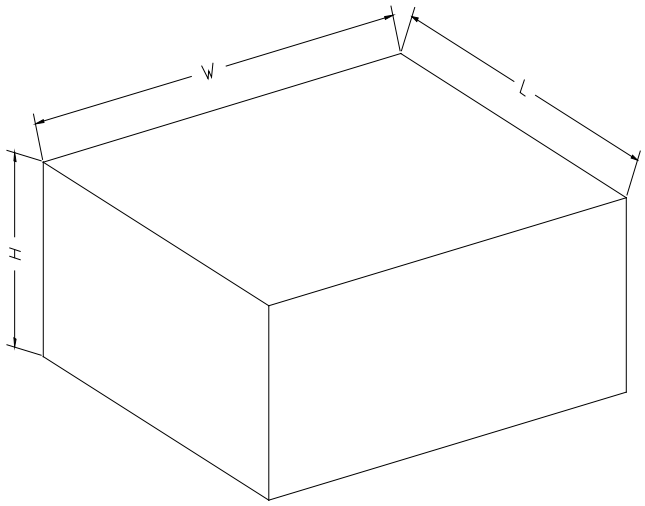
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSOT-23-6	7"	9.5	3.20	3.10	1.10	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002