# SGMGQ11810
# 100V Half-Bridge GaNFETs Power Stage

## GENERAL DESCRIPTION

The SGMGQ11810 is a 100V, 60A power stage with integrated half-bridge GaNFETs in a compact 5mm × 6.5mm LGA package. Included in the package are two high-performance GaN FETs, drivers, and driver supply capacitors, offering the industry's most compact and efficient GaN power solution.

The SGMGQ11810 provides two logic inputs for controlling the high-side and low-side GaN FETs for maximum flexibility. The split driver outputs allow for independent adjustment of turn-on and turn-off strengths, optimizing both EMI and efficiency.

The SGMGQ11810 features input interlocking with an internal adaptive shoot-through protection circuit, ensuring no simultaneous output conduction even at near zero dead time. Comprehensive fault protection is built into the SGMGQ11810, including active bootstrap (BST) voltage control to prevent overcharge and ensure stable gate drive voltage, independent UVLO and OVLO for both VCC and BST, and over-temperature protection.

With fast propagation delay, excellent delay matching, superior dv/dt immunity, and ultra-low in-package parasitic inductance loop, the SGMGQ11810 enables designers to achieve substantial improvement in power density and efficiency.

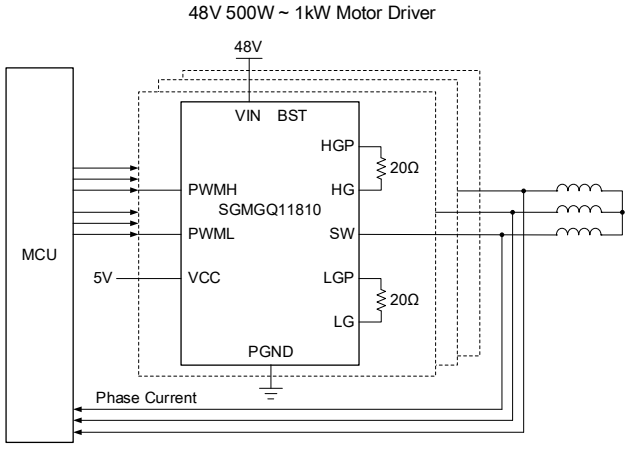
## FEATURES

- **2.4mΩ Half-Bridge GaN FETs with Gate Driver**
- **80V Continuous, 100V Transient Voltage Rating**
- **Capable of Providing up to 5MHz Switching**
- **Independent High-side and Low-side PWM Inputs**
- **High-side and Low-side Driver Interlocking**
- **Internal Strong and Smart Bootstrap Switch**
- **Adaptive Shoot-Through Protection**
- **Fast Propagation Delay (20ns TYP)**
- **Excellent Delay Matching (1ns TYP)**
- **Built-In UVLO, OVLO, OTP Protections**
- **35μA Low VCC Quiescent Current**
- **Integrated VCC/BST Capacitors**
- **High dv/dt Immunity up to 50V/ns**
- **Adjustable Turn-On Speeds**
- **Optimized for Easy and Low-EMI PCB Layout**
- **Available in a Green LGA-5×6.5-30L Package**

## APPLICATIONS

Motor Drive Applications

## SIMPLIFIED SCHEMATIC



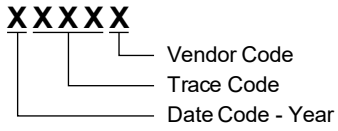

代理商 威尔逊 www.visvie.com 联系电话 138 2526 5270

# PACKAGE/ORDERING INFORMATION

| MODEL | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKAGE MARKING | PACKING OPTION |
|---|---|---|---|---|---|
| SGMGQ11810 | LGA-5×6.5-30L | -40℃ to +150℃ | SGMGQ11810TLBK30G/TR | 11810<br>LBK30<br>XXXXX | Tape and Reel, 2500 |

## MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.




Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

## ABSOLUTE MAXIMUM RATINGS

Drain-to-Source Voltage of Internal GaN FET ..... 100V
VIN ..... 100V
VCC, BST to SW ..... -0.3V to 6V
SW ..... -5V to 100V
BST ..... -0.3V to 105V
HGP, HG ..... ($V_{SW}$ - 0.3V) to ($V_{BST}$ + 0.3V)
LGP, LG ..... -0.3V to 6V
PWMH, PWML ..... -0.3V to 6V
Continuous Current for Internal GaN FET (1) ..... 60A
Current for Internal GaN FET (Pulse) ..... 230A
Package Thermal Resistance
LGA-5×6.5-30L, $R_{\theta JA}$ (2) ..... 59℃/W
LGA-5×6.5-30L, $R_{\theta JC_TOP}$ ..... 14.8℃/W
LGA-5×6.5-30L, $R_{\theta JC_BOTTOM}$ ..... 4.1℃/W
Junction Temperature ..... -40℃ to +150℃
Storage Temperature Range ..... -40℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (3) (4)
HBM ..... ±1000V
CDM ..... ±1000V

NOTES:

1. Ideal thermal condition. In real application the current capability depends on system thermal design.

2. According to standards defined in JESD51 and JESD51-1, thermal characteristic of the package is simulated. $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2oz copper on FR4 board.

3. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

4. JEDEC document JEP155 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## RECOMMENDED OPERATING CONDITIONS

VIN ..... 0V to 80V
VCC ..... 4.5V to 5.5V
PWMH, PWML ..... 0V to 5.5V
SW ..... -4V to 80V
BST ..... (SW + 4.5V) to (SW + 5.5V)
SW Slew Rate ..... 50V/ns
Operating Junction Temperature Range ..... -40℃ to +125℃

## OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

## ESD SENSITIVITY CAUTION

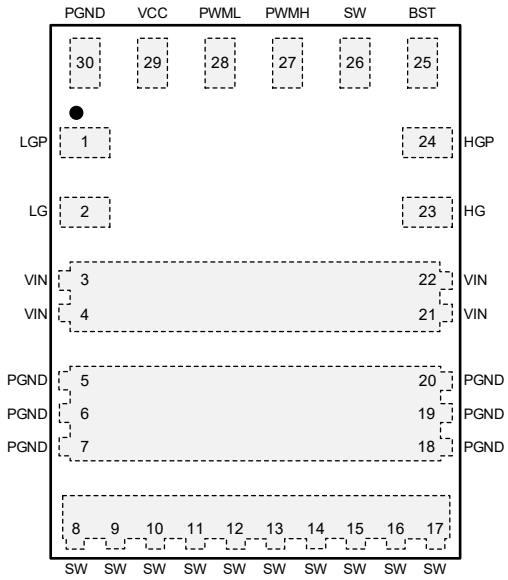
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

## PIN CONFIGURATION

**(TOP VIEW)**




**LGA-5×6.5-30L**

## PIN DESCRIPTION

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | LGP | Low-side Gate Driver Source-Current Output. An optional resistor between LGP and LG can be employed to adjust turn-on speed of low-side GaN FET. |
| 2 | LG | Low-side Gate Terminal. |
| 3-4, 21-22 | VIN | Input Voltage Supply. Locally bypass this pin to PGND with ceramic capacitors. |
| 5-7, 18-20, 30 | PGND | Power Ground. |
| 8-17 | SW | Switching Node for Main Power. |
| 23 | HG | High-side Gate Terminal. |
| 24 | HGP | High-side Gate Driver Source-Current Output. An optional resistor between HGP and HG can be employed to adjust turn-on speed of high side GaN FET. |
| 25 | BST | High-side Gate Driver Bootstrap Rail. Two 0.1μF ceramic capacitors are integrated between BST and SW pins, and external bootstrap capacitor is optional. |
| 26 | SW | Switching Node for Gate Drive Loop. SW waveform can be monitored. Pin 26 is connected to Pin 8-17 internally and no external connection is necessary. |
| 27 | PWMH | High-side Driver PWM Input. This pin has an internal 200kΩ pull-down resistor. |
| 28 | PWML | Low-side Driver PWM Input. This pin has an internal 200kΩ pull-down resistor. |
| 29 | VCC | External 5V Driver Supply. Two 0.1μF ceramic capacitors are integrated between VCC and PGND pins, and external decoupling capacitor is optional. |

# ELECTRICAL CHARACTERISTICS

($T_J$ = +25℃, VCC = BST = 5V, SW = PGND = 0V, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Supply Input** | | | | | | |
| VCC Quiescent Current | $I_{CC-Q}$ | PWMH = PWML = 0 | | 35 | 60 | μA |
| VCC Operating Current | $I_{CC-OP}$ | f = 1MHz | | 20 | 30 | mA |
| BST Quiescent Current | $I_{BST-Q}$ | PWMH = PWML = 0 | | 40 | 70 | μA |
| BST Operating Current | $I_{BST-OP}$ | f = 1MHz | | 20 | 30 | mA |
| VCC Over-Voltage Rising Threshold | $V_{CC-OVR}$ | | 5.7 | 6 | 6.3 | V |
| VCC Over-Voltage Hysteresis | $V_{CC-OVHYS}$ | | | 0.25 | | |
| VCC Under-Voltage Rising Threshold | $V_{CC-UVR}$ | | 3.9 | 4.1 | 4.3 | |
| VCC Under-Voltage Hysteresis | $V_{CC-UVHYS}$ | | | 0.3 | | |
| BST Under-Voltage Rising Threshold | $V_{BST-UVR}$ | | | 3.6 | | |
| BST Under-Voltage Hysteresis | $V_{BST-UVHYS}$ | | | 0.5 | | |
| **PWM Input** | | | | | | |
| Input High Threshold | $V_{IH}$ | | | 1.8 | 2.2 | V |
| Input Low Threshold | $V_{IL}$ | | 0.8 | 1.2 | | |
| Input Hysteresis | $V_{I-HYS}$ | | | 0.6 | | |
| Input Pull-Down Resistance | $R_I$ | | | 200 | | kΩ |
| **Bootstrap Switch** | | | | | | |
| Switch On Resistance | $R_{BST_ON}$ | | | 4 | | Ω |
| **High and Low-side Gate Driver** | | | | | | |
| Output Pull-Down Resistance | $R_{DN}$ | $I_{HG}$ or $I_{LG}$ = 10mA | | 0.2 | 1 | Ω |
| Output Pull-Up Resistance | $R_{UP}$ | $I_{HGP}$ or $I_{LGP}$ = -10mA | | 1 | 2 | |
| Output Peak Source Current (1) | $I_{OH}$ | HGP = SW or LGP = PGND | | 1.7 | | A |
| Output Peak Sink Current (1) | $I_{OL}$ | HG = BST or LG = VCC | | 4.3 | | |
| **Over-Temperature Protection** | | | | | | |
| OTP Shutdown Rising Threshold (1) | $T_{OTP}$ | | | 165 | | ℃ |
| OTP Shutdown Hysteresis (1) | $T_{OTP-HYS}$ | | | 20 | | |
| **GaN FETs** | | | | | | |
| Drain-to-Source Breakdown Voltage | $V_{BR_DSS}$ | $I_D$ = 400μA, PWML = 0V or PWMH = 0V | 100 | | | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 80V, PWML = 0V or PWMH = 0V | | 4 | 28 | μA |
| Drain-to-Source On-State Resistance | $R_{DSON}$ | $I_D$ = 25A, PWML = 5V or PWMH = 5V | | 2.4 | 3.2 | mΩ |
| Source-to-Drain Forward Voltage | $V_{SD}$ | $I_S$ = 0.5A, PWML = 0V or PWMH = 0V | | 1.5 | | V |
| Output Capacitance (1) | $C_{OSS}$ | $V_{DS}$ = 50V, PWML = 0V or PWMH = 0V | | 463 | | pF |
| Reverse Transfer Capacitance (1) | $C_{RSS}$ | | | 8.2 | | |
| Effective Output Capacitance, Energy Related (1) | $C_{O_ER}$ | $V_{DS}$ = 0V to 50V, PWML = 0V or PWMH = 0V | | 700 | | pF |
| Effective Output Capacitance, Time Related (1) | $C_{O_TR}$ | | | 1020 | | |
| Output Charge (1) | $Q_{OSS}$ | | | 50 | | nC |

NOTE: 1. Not 100% tested and guaranteed by design.

## SWITCHING CHARACTERISTICS

($T_J$ = +25℃, VCC = BST = 5V, SW = PGND = 0V, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Minimum Input Pulse Width that Changes the Output (1) | $t_{IPW}$ | | | 10 | | ns |
| Minimum Gate Output Pulse Width (1) | $t_{OPW}$ | | | 12 | | |
| HGP Rise Time (0.5V-4.5V) (1) | $t_{R_SW}$ | | | 10 | | |
| HG Fall Time (4.5V-0.5V) (1) | $t_{F_SW}$ | | | 3 | | |
| LGP Rise Time (0.5V-4.5V) (1) | $t_{R_LS}$ | | | 10 | | |
| LG Fall Time (4.5V-0.5V) (1) | $t_{F_LS}$ | | | 3 | | |
| Dead time, LG off to HGP on (1) | $t_{DTH}$ | | | 1 | | |
| Dead time, HG off to LGP on (1) | $t_{DTL}$ | | | 1 | | |
| HG Turn-Off Propagation Delay (1) | $t_{HPHL}$ | PWMH falling to HG falling | | 20 | | |
| HGP Turn-On Propagation Delay (1) | $t_{HPLH}$ | PWMH rising to HGP rising | | 20 | | |
| LG Turn-Off Propagation Delay (1) | $t_{LPHL}$ | PWML falling to LG falling | | 20 | | |
| LGP Turn-On Propagation Delay (1) | $t_{LPLH}$ | PWML rising to LGP rising | | 20 | | |
| Delay Matching LGP On and HG Off (1) | $t_{MON}$ | | | 1 | | |
| Delay Matching LG Off and HGP On (1) | $t_{MOFF}$ | | | 1 | | |

NOTE: 1. Not 100% tested and guaranteed by design.

## TYPICAL PERFORMANCE CHARACTERISTICS

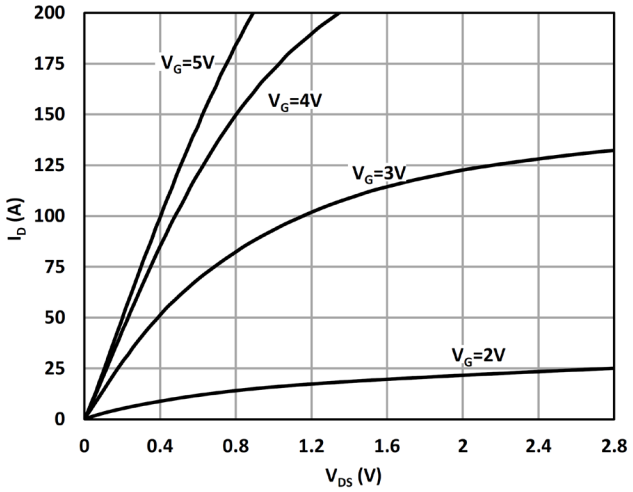



Figure 1. Pulsed Drain Current vs. Drain Voltage (25°C)

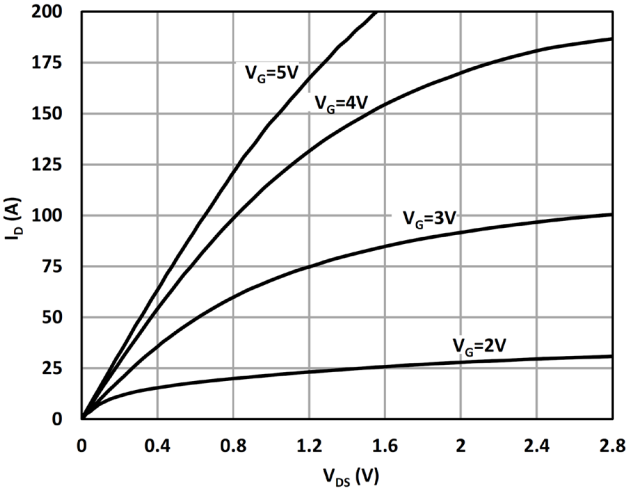



Figure 2. Pulsed Drain Current vs. Drain Voltage (125°C)

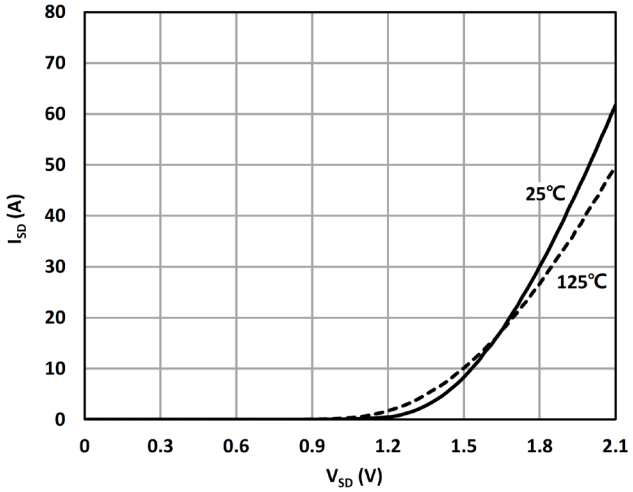



Figure 3. Source-Drain Reverse Conduction Voltage

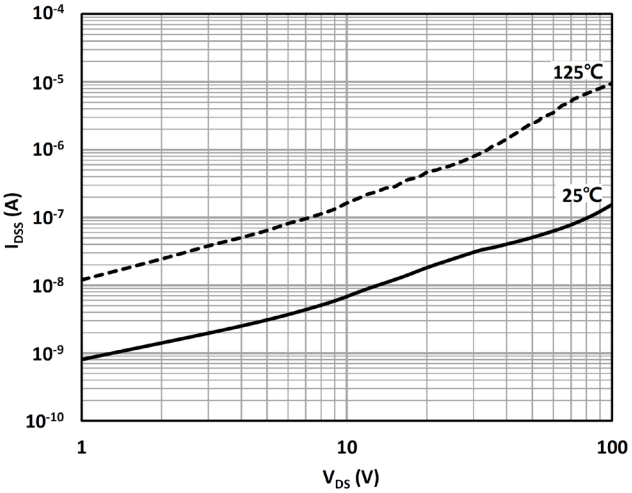



Figure 4. Drain Leakage Current vs Drain Voltage

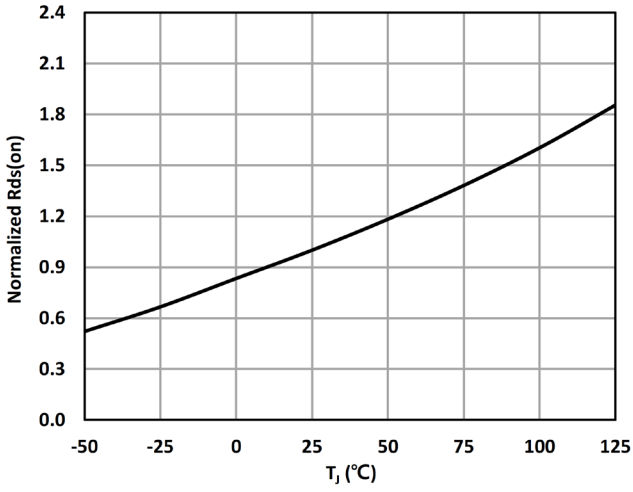



Figure 5. Normalized $R_{DS(ON)}$ vs Temperature

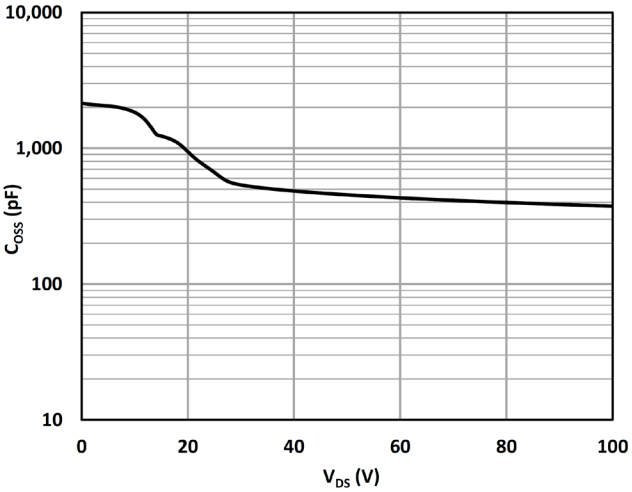



Figure 6. Output Capacitance vs Drain Voltage

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

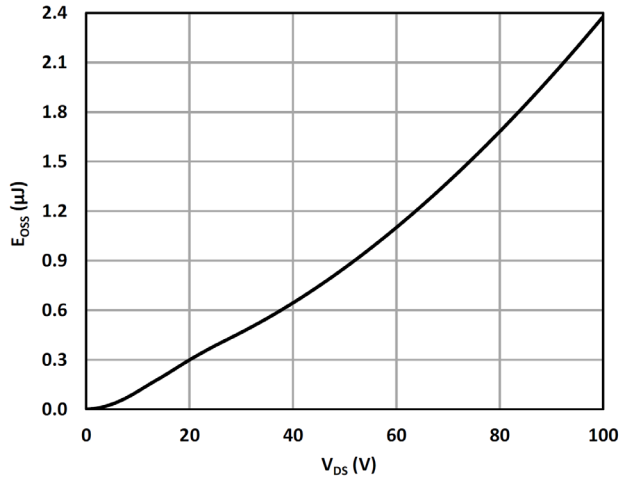



Figure 7. Output Capacitance Stored Energy vs Drain Voltage

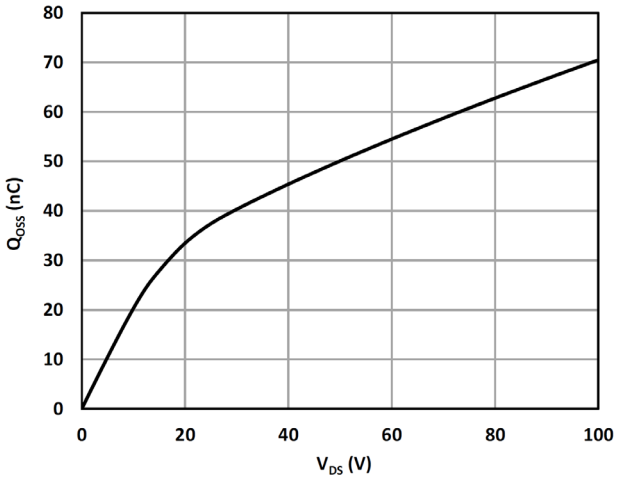



Figure 8. Output Charge vs Drain Voltage

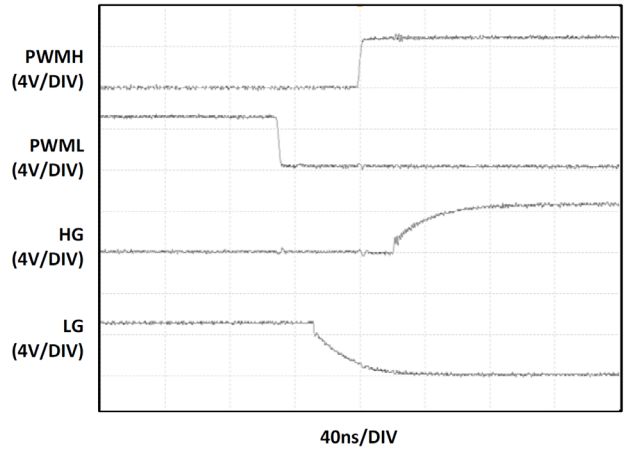



Figure 9. HG Turn-On and LG Turn-Off Waveform with 20Ω external gate resistors

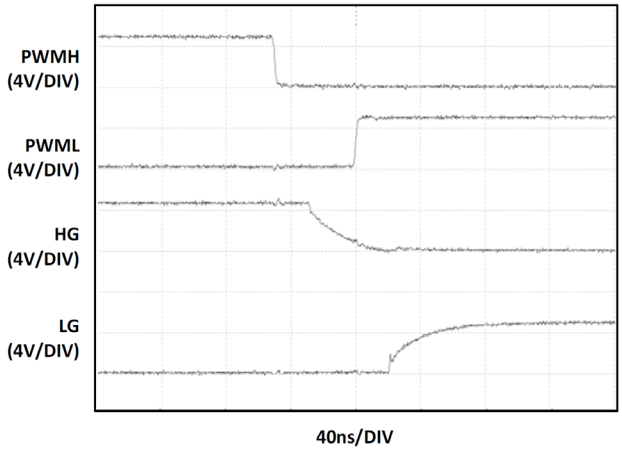



Figure 10. HG Turn-Off and LG Turn-On Waveform with 20Ω external gate resistors

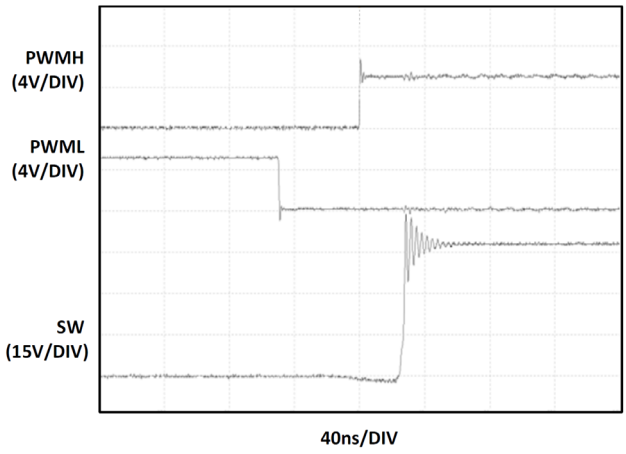



Figure 11. SW Rising Waveform at $V_{IN}$=48V and $I_{OUT}$=20A

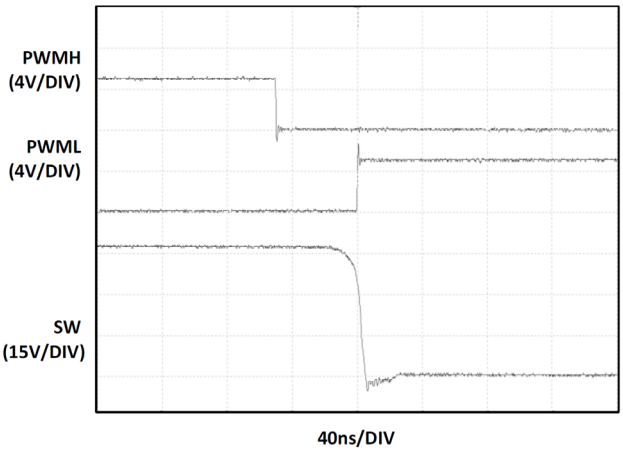



Figure 12. SW Falling Waveform at $V_{IN}$=48V and $I_{OUT}$=20A

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

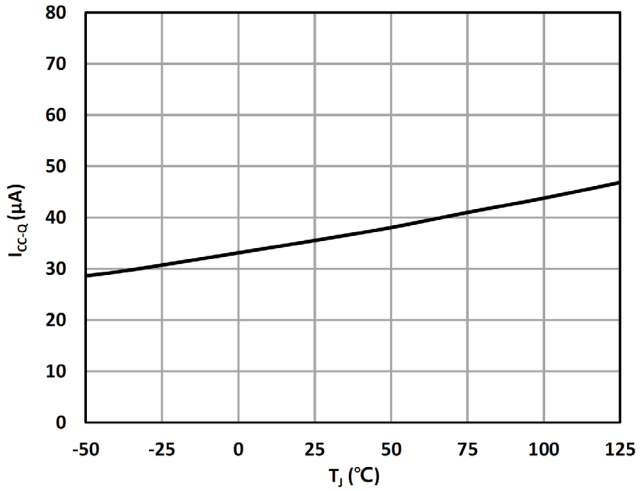



Figure 13. VCC Quiescent Current vs Temperature

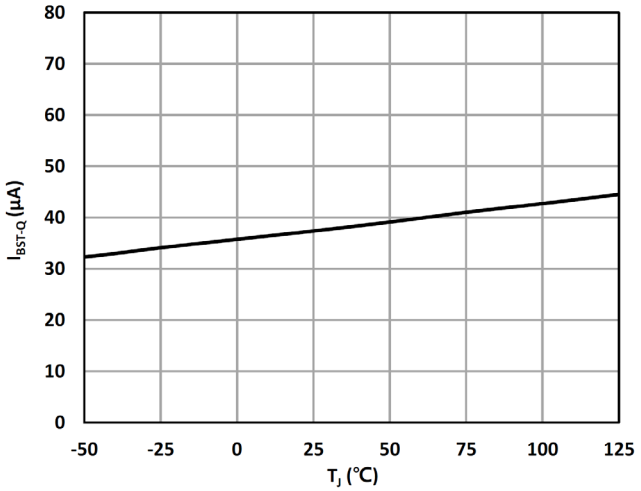



Figure 14. BST Quiescent Current vs Temperature

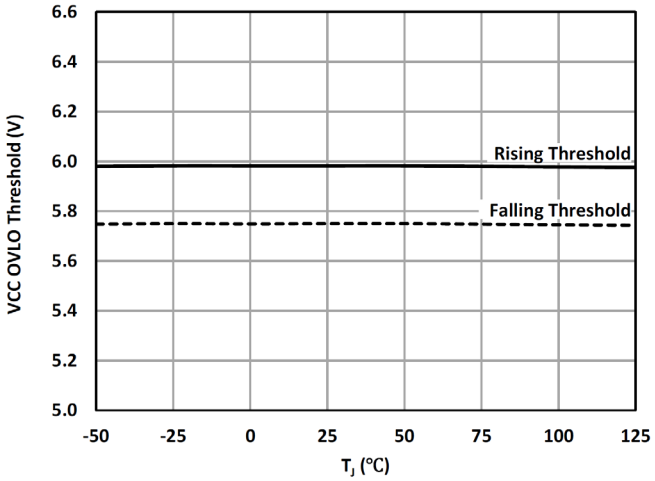



Figure 15. VCC OVLO Threshold vs Temperature

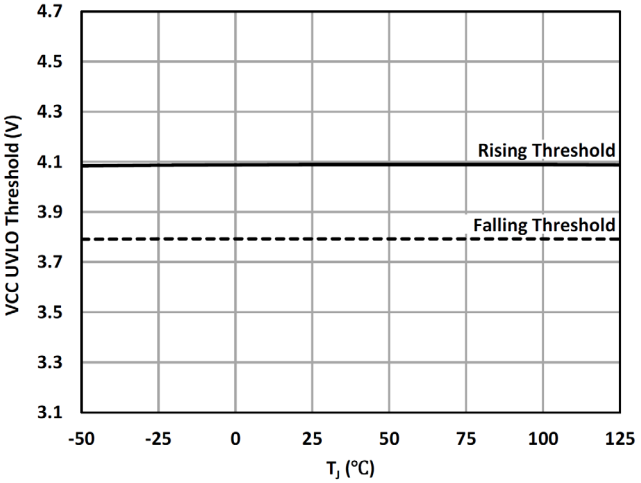



Figure 16. VCC UVLO Threshold vs Temperature

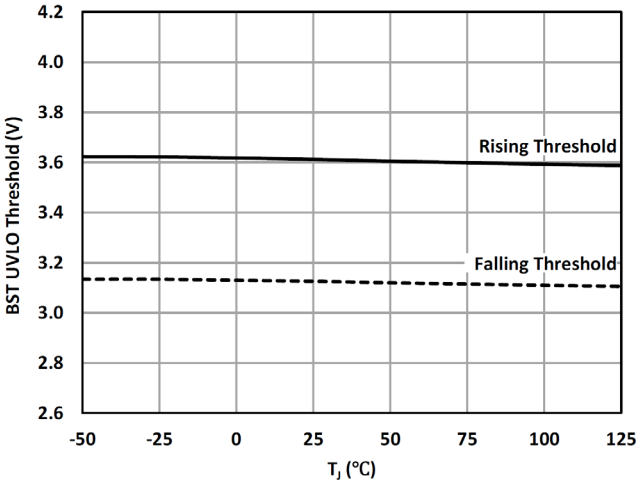



Figure 17. BST UVLO Threshold vs Temperature

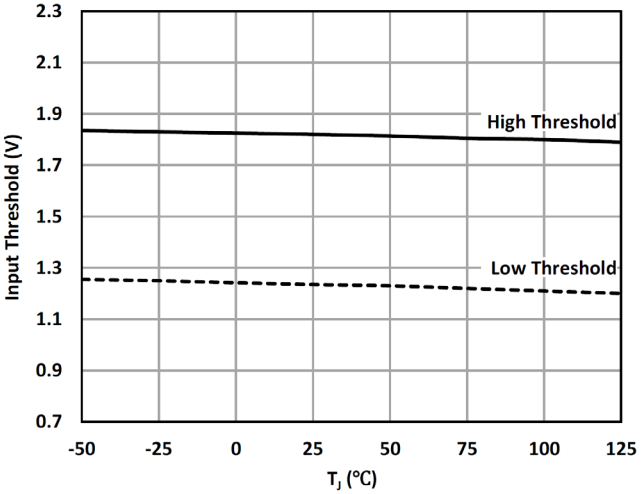



Figure 18. PWM Input Threshold vs Temperature

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

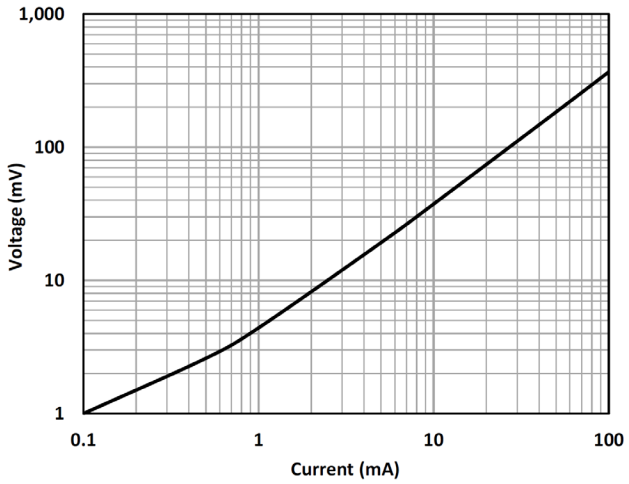



Figure 19. Bootstrap Forward Voltage vs Current

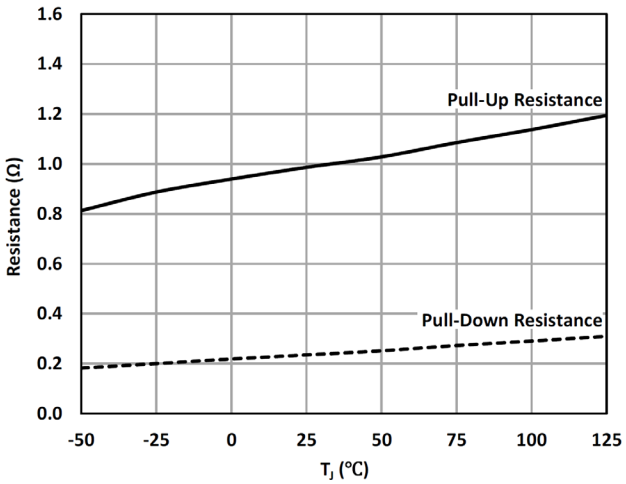



Figure 20. Output Pull-Down/Pull-Up Resistance vs Temperature

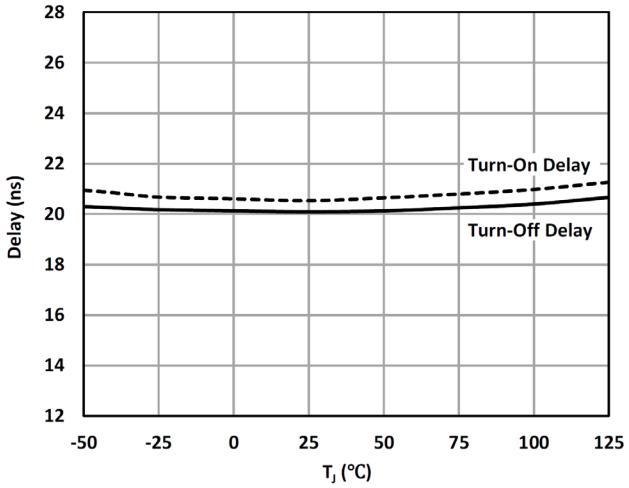



Figure 21. Low-Side Propagation Delay vs Temperature

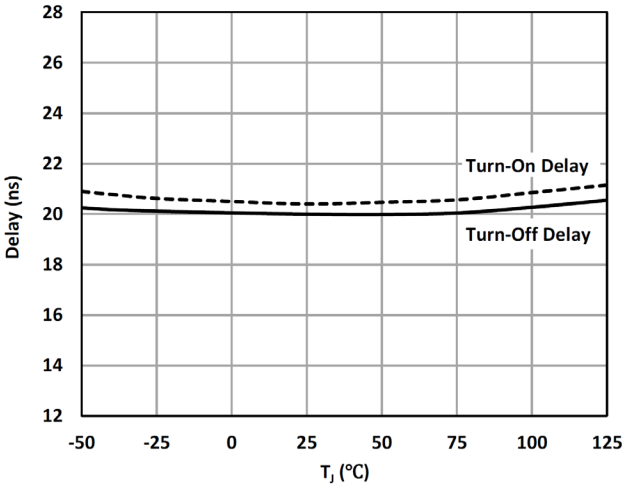



Figure 22. High-Side Propagation Delay vs Temperature

## FUNCTIONAL BLOCK DIAGRAM

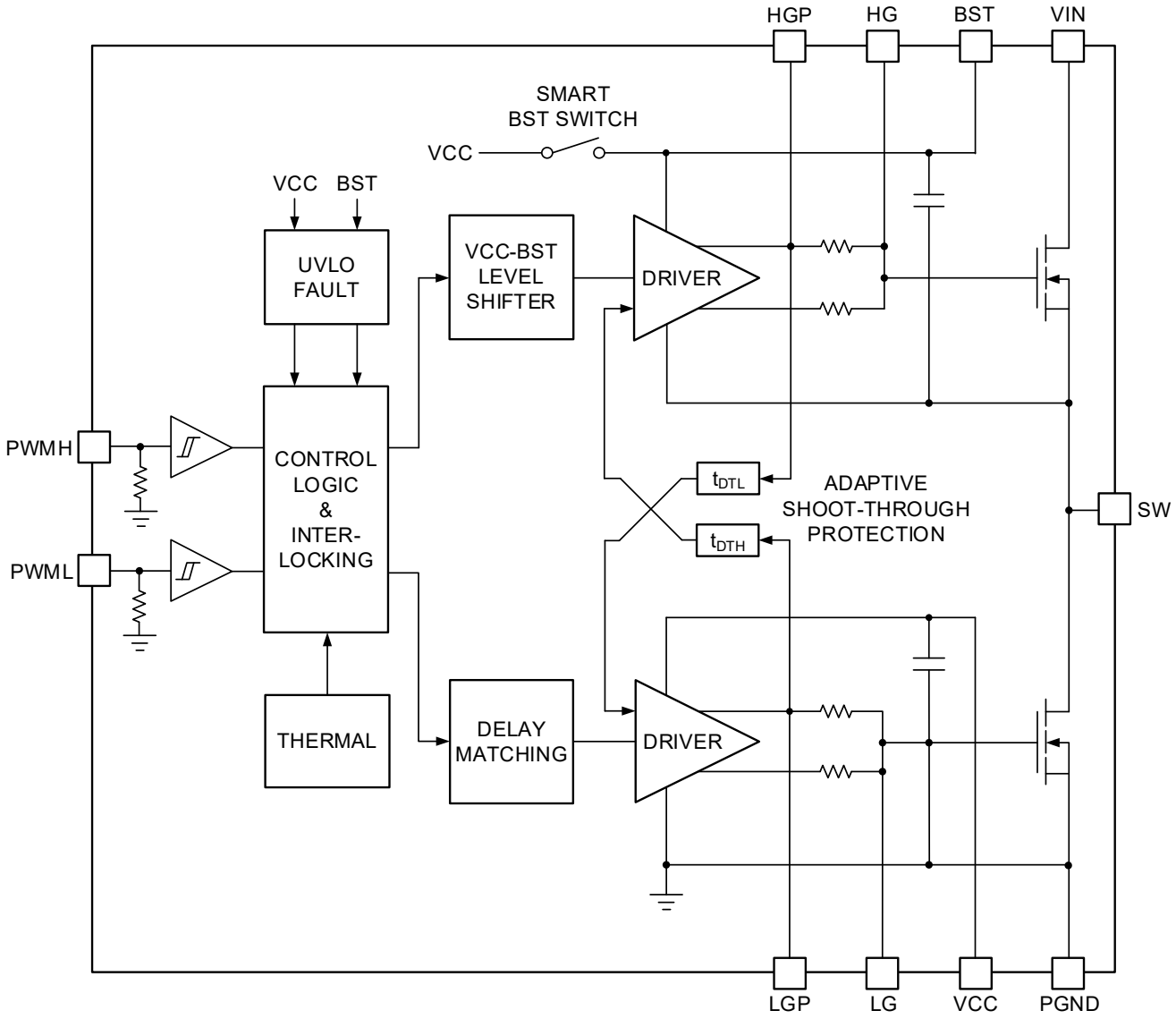



**Figure 23. Block Diagram**

# DETAILED DESCRIPTION

The SGMGQ11810 is a 100V, 60A power stage with integrated half-bridge GaNFETs in a compact 5mm × 6.5mm LGA package. Included in the package are two high-performance enhancement-mode GaN FETs, gate drivers, gate resistors, and VCC and BST supply capacitors, offering the smallest, most efficient, and easiest-to-use GaN power stage solution.

The SGMGQ11810 features two independent and TTL logic compatible inputs to offer control flexibility. It provides split gate driver outputs for the independent control of turn-on and turn-off speeds of both high-side and low-side GaN FETs by adding external gate resistors. The SGMGQ11810's PWM input interlocking function with integrated adaptive shoot-through protection ensures that no output conducts simultaneously, even under near zero dead time delay conditions. Active bootstrap (BST) voltage control in SGMGQ11810 prevents overcharging of the BST supply during dead times, protecting the gate of the GaN FETs. Additionally, rich fault protection is provided including independent VCC and BST under-voltage lockout (UVLO), VCC over-voltage lockout (OVLO), and over-temperature protection (OTP). Highly integrated with ultra-low inductance, fast propagation delay, and superior dv/dt immunity, the SGMGQ11810 drives next-generation high-frequency, high-power-density applications across diverse topologies including Buck, Boost, and Buck-Boost.

## Input and Output

The SGMGQ11810 input pins, PWMH and PWML, are independent and TTL logic compatible with the ability to withstand input voltages up to 5.5V regardless of VCC voltage. The SGMGQ11810 offers fast propagation delay (20ns TYP) with excellent delay matching (1ns TYP) between the high-side and low-side driver channels, making it ideal for high-frequency applications. Both inputs feature a 10ns (TYP) input deglitch filter to remove any unwanted pulses from a PWM input. A narrow input pulse exceeding this deglitch delay time will be extended to a minimum output pulse of 12ns (TYP) to ensure proper gate turn-on and turn-off transients. Figure 24 shows the switching characteristics of the input and output. The SGMGQ11810 features the interlocking function to prevent shoot-through condition. When both input pins, PWMH and PWML, are high, the internal logic turns off both output pins, HG and LG, as illustrated in Figure 25. Both input pins have an internal pull-down resistor of 200kΩ. Table 1 shows the truth table of input and output.

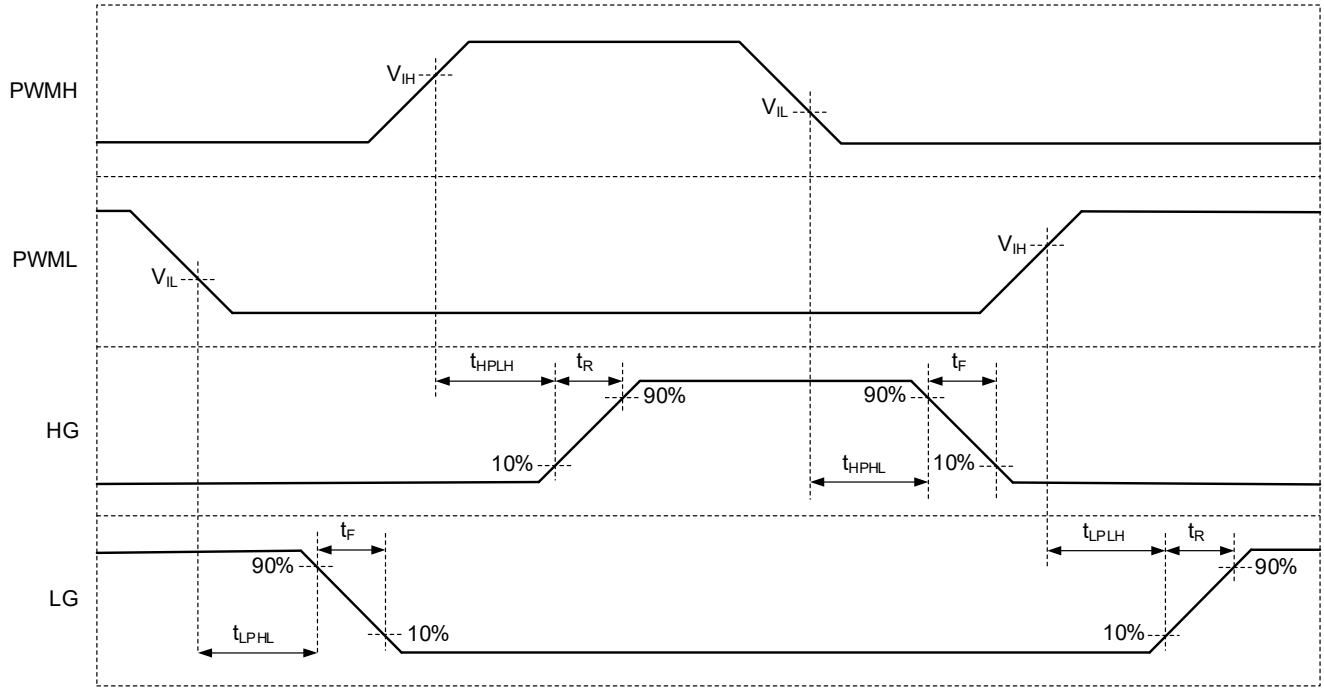



**Figure 24. Timing Diagram of Input and Output**

## DETAILED DESCRIPTION (continued)

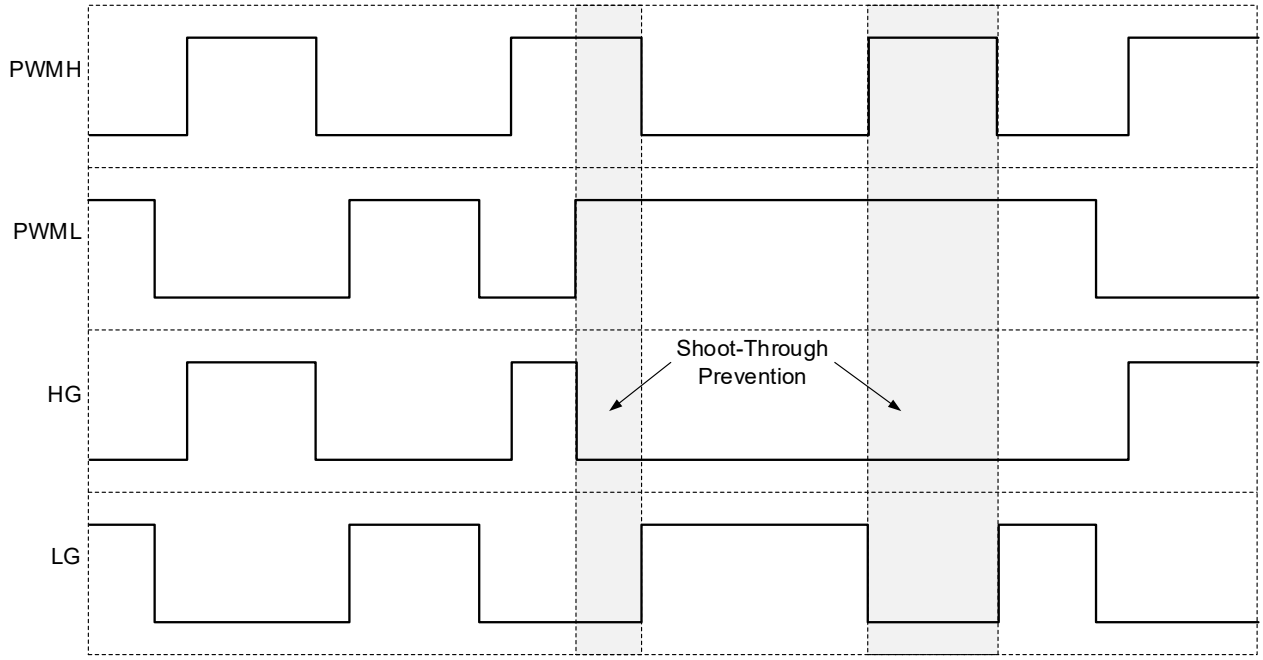



**Figure 25. Timing Diagram of Interlocking Function**

**Table 1. Input and Output Truth Table**

| PWMH | PWML | HG | LG | COMMENT |
|---|---|---|---|---|
| H | L | H | L | High-side GaN FET On |
| L | H | L | H | Low-side GaN FET On |
| L | L | L | L | Both GaN FETs Off |
| H | H | L | L | Both GaN FETs Off |

### Adaptive Shoot-Through Protection

The SGMGQ11810 features an internal shoot-through protection circuit, leveraging shunt sensing of the true gate voltage of GaN FETs through its split outputs structure. It offers precise switching timing control for immediate turn-on after complete turn-off of the opposite side to ensure that they do not conduct simultaneously in any situation. This is processed within a 1ns (TYP) period to achieve near-zero dead time delay, enhancing efficiency and enabling high-frequency operation.

### Half-Bridge Output Stage

The SGMGQ11810 integrates 2.4mΩ, 100V, enhancement-mode GaN FETs with drivers in a half-bridge configuration. It offers increased flexibility by providing split gate driver outputs for both high-side and low-side GaN FETs. As depicted in Figure 26, the internal gate drive output provides a default 20Ω internal pull-up resistor and a 10Ω internal pull-down resistor. Designers can further fine-tune turn-on strength by adding an external resistor in parallel between designated pins of HGP/HG and/or LGP/LG. While turning off the GaN FETs, the integrated strong 0.2Ω pull-down FET offers a robust, low impedance path necessary for eliminating high dv/dt induced gate turn-on. Additionally, the SGMGQ11810 integrates the 0.2μF BST and VCC supply capacitors within the package, thereby significantly reducing parasitic inductance loop paths and effectively minimizing voltage spikes at the gates of the GaN FETs. HG and LG pins have internal 50kΩ pull-down resistors to SW and PGND, respectively.

## DETAILED DESCRIPTION (continued)

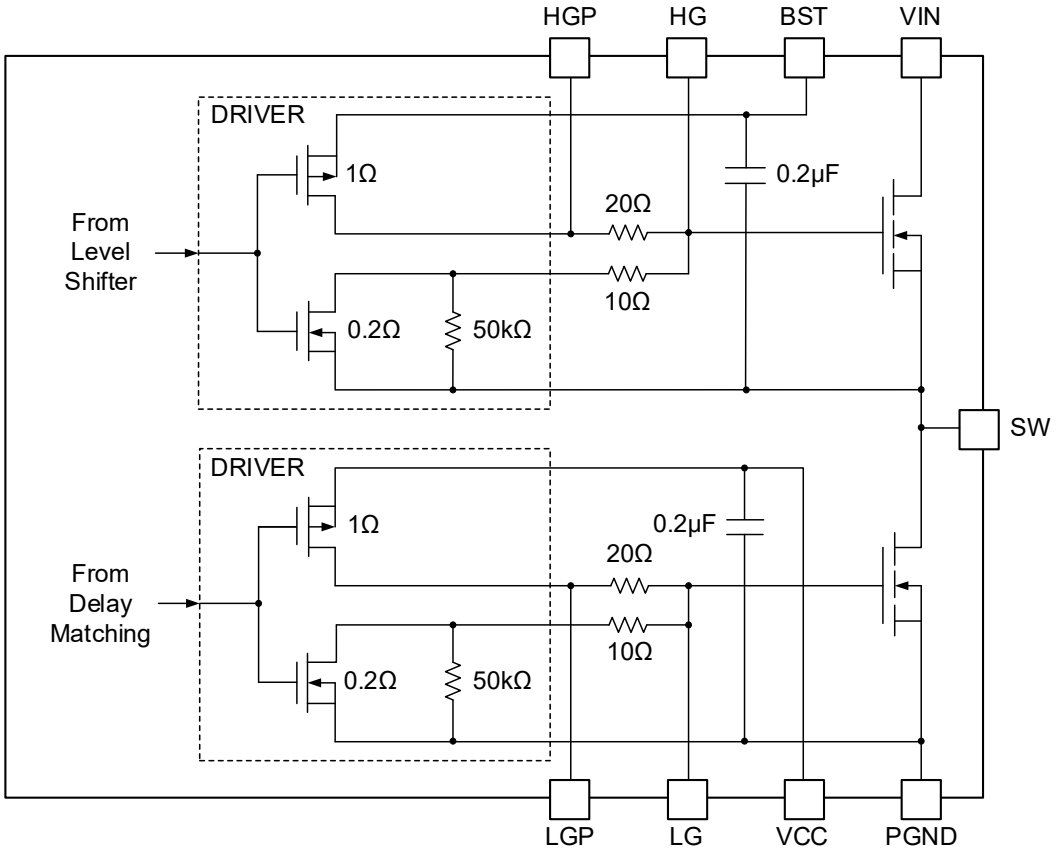



**Figure 26. Simplified Output-Stage Block Diagram**

### VCC UVLO/OVLO Protections

The SGMGQ11810 features UVLO and OVLO for VCC, providing the operation under the safe conditions of devices. When the VCC voltage falls below its UVLO threshold of 3.8V (TYP) or exceeds its OVLO threshold of 6V (TYP), the SGMGQ11810 turns off both the high-side and low-side GaN FETs and ignores the PWMH and PWML inputs.

### High dv/dt Rate GaN FET Switching

GaN FETs can switch much faster than traditional silicon-based MOSFETs, requiring gate drivers capable of delivering precise and fast switching signals to fully leverage their potential. Managing high dv/dt rates during switching is important for stable gate driver circuitry, ensuring reliable and efficient operation. The SGMGQ11810 features an advanced level-shifting technology circuit designed to overcome these challenges associated with driving GaN FETs. Its advanced noise rejection mechanism ensures precise and accurate signal transmission between the control logic and driver outputs even in extreme high dv/dt environments up to 50V/ns.

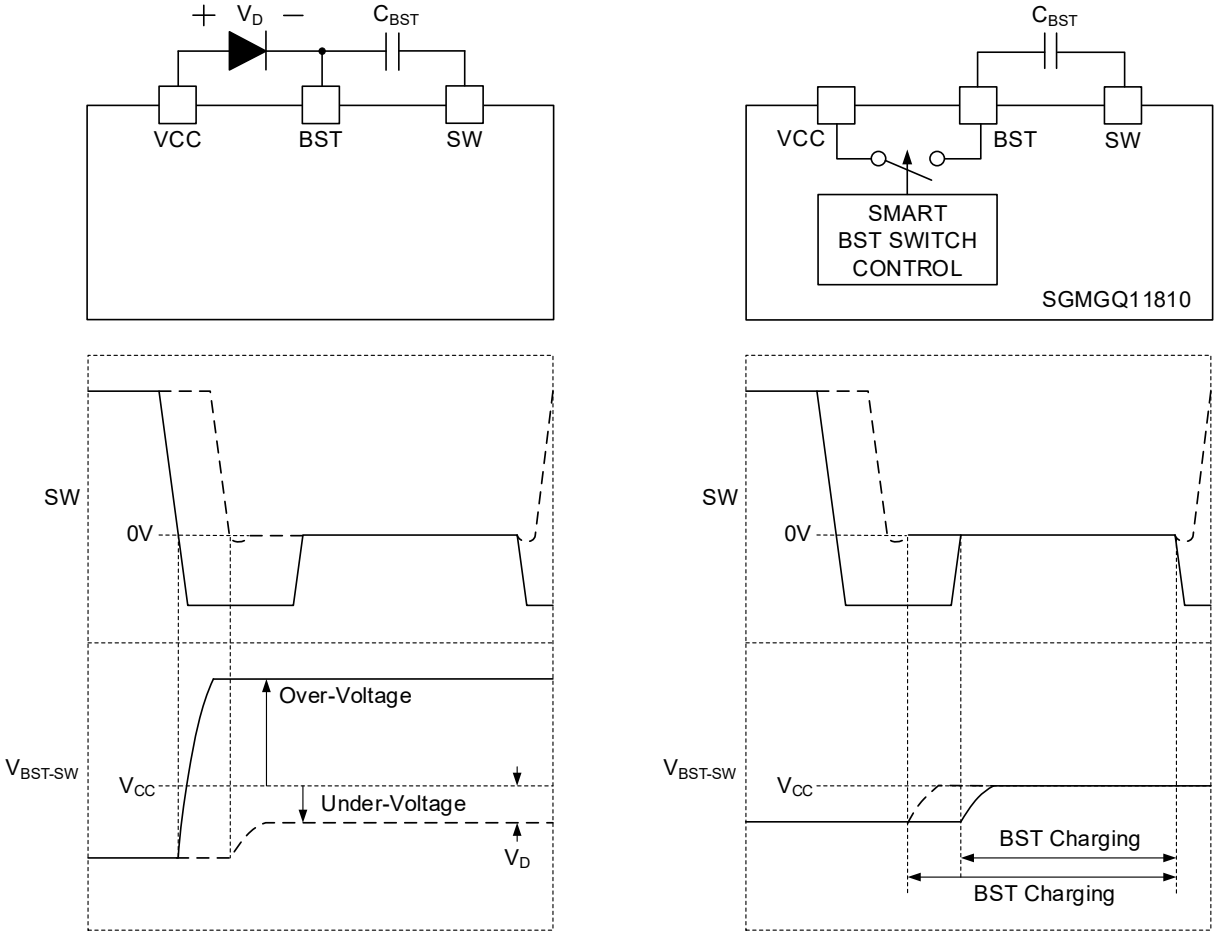
Another challenge in driving GaN FETs is the issue of high reverse conduction voltage. When the SW node drops below 0V due to this reverse conduction, it can temporarily lower the level shifter's supply rail, causing a disruption in the level shifter's output signals. This disruption can appear as a delay mismatch between signals transmitted to each side of the driver, resulting in timing inaccuracies and potential performance degradation. The proposed level shifter in the SGMGQ11810 is designed to prevent such conditions, ensuring that delay variation is kept to a minimum (1ns TYP) even when the SW node fluctuates by up to -4V. Furthermore, the SGMGQ11810 features an additional delay matching circuit that parallels the proposed level shifter circuit, matching its process and temperature variation characteristics. This additional feature further improves delay matching to 1ns (TYP).

# DETAILED DESCRIPTION (continued)

## High-side Gate-Driver Supply

Despite GaN devices featuring a superior figure of merit ($Q_G \times R_{DSON}$) over silicon-based MOSFETs, their sensitivity to gate drive voltage presents a challenging concern. GaN devices are more vulnerable to both over-voltage and under-voltage conditions at the gate, which can have negative effects on their reliability and performance. The concern over gate over-voltage is more significant for GaN FETs, given that they are considerably more fragile compared to their silicon counterparts. Conversely, insufficient gate voltage, or gate under-voltage, can result in increased switching losses and reduced efficiency.

To mitigate these challenges, the SGMGQ11810 features a smart BST switch that allows precise control for BST charging and blocking. Figure 27 illustrates the operation principle of the smart BST switch. Unlike silicon MOSFETs, GaN FETs typically lack an intrinsic body diode, resulting in higher reverse conduction voltages (typically 2V to 3V or even higher at high current) during dead time. This can lead to overcharging of the BST capacitor, potentially causing permanent damage to the gate of the high-side GaN FET. In the SGMGQ11810, the BST switch's turning on and off are precisely controlled so that it allows charging of the BST capacitor only during SW node is fully reached at PGND voltage when the low-side power switch is being turned on. Moreover, the BST switch exhibits a low on-impedance of 4Ω (TYP), ensuring minimal dropout voltage. Accordingly, the SGMGQ11810 always maintains a well-balanced BST rail voltage close to VCC, achieving excellent delay matching and balanced gate driving strength between the high-side and low-side drivers.




(a) Conventional Bootstrap Diode (b) Smart Bootstrap Switch

**Figure 27. Operation Principle of Bootstrap Supply**

## DETAILED DESCRIPTION (continued)

Additionally, the SGMGQ11810 provides BST UVLO protection with a falling threshold of 3.1V (TYP) and a rising threshold of 3.6V (TYP). When BST-SW falls below the BST UVLO threshold, the SGMGQ11810 enters BST UVLO mode, turns off the high-side GaN FET, but the low-side driver and GaN FET remain activated.

### Over-Temperature Protection (OTP)

The SGMGQ11810 employs OTP. If the internal junction temperature, $T_J$, exceeds +165℃ (TYP), the PWMH and PWML inputs are ignored, and both the high-side and low-side GaN FETs are turned off. When the temperature drops below +145℃ (TYP), the SGMGQ11810 will resume normal operation.

### Layout Recommendation

Due to the small input capacitance of the GaN FET, the SGMGQ11810 can support high-frequency operation, but it causes high dv/dt and high di/dt in the power loop. To avoid the voltage and current spike caused by high dv/dt and high di/dt, the parasitics of the gate driving loop and power loop must be reduced by proper layout techniques.

The SGMGQ11810 employs an excellent layout on internal substrate to reduce the gate driving loop and power loop. (1) The driver has been placed very close to the GaN FETs to minimize the loops of parasitic inductance and reduce the noise on the gate loop. (2) The bootstrap capacitor is integrated in the module and the distance between BST and VCC to the driver has been minimized to minimize power loop impedance. (3) The distance between high-side GaN FET and low-side GaN FET has been minimized to avoid excessive voltage spike on the driver caused by the parasitic inductance between high-side GaN FET and low-side GaN FET.

Although the optimized pinout of the SGMGQ11810 simplifies the power stage layout significantly, a proper layout of PCB board is required to fully utilize the benefit of the SGMGQ11810. The layout guidelines are as follows:

1. The optional resistor between HGP (LGP) pin and HG (LG) pin to adjust the turn-on speed of the GaN FETs should be placed close to SGMGQ11810.

2. The optional VCC decoupling capacitor should be placed close to SGMGQ11810.

3. Use planes for VIN and PGND to minimize power losses and ensure effective voltage filtering. The power input decoupling capacitors should be placed close to SGMGQ11810.

## TYPICAL APPLICATION CIRCUITS

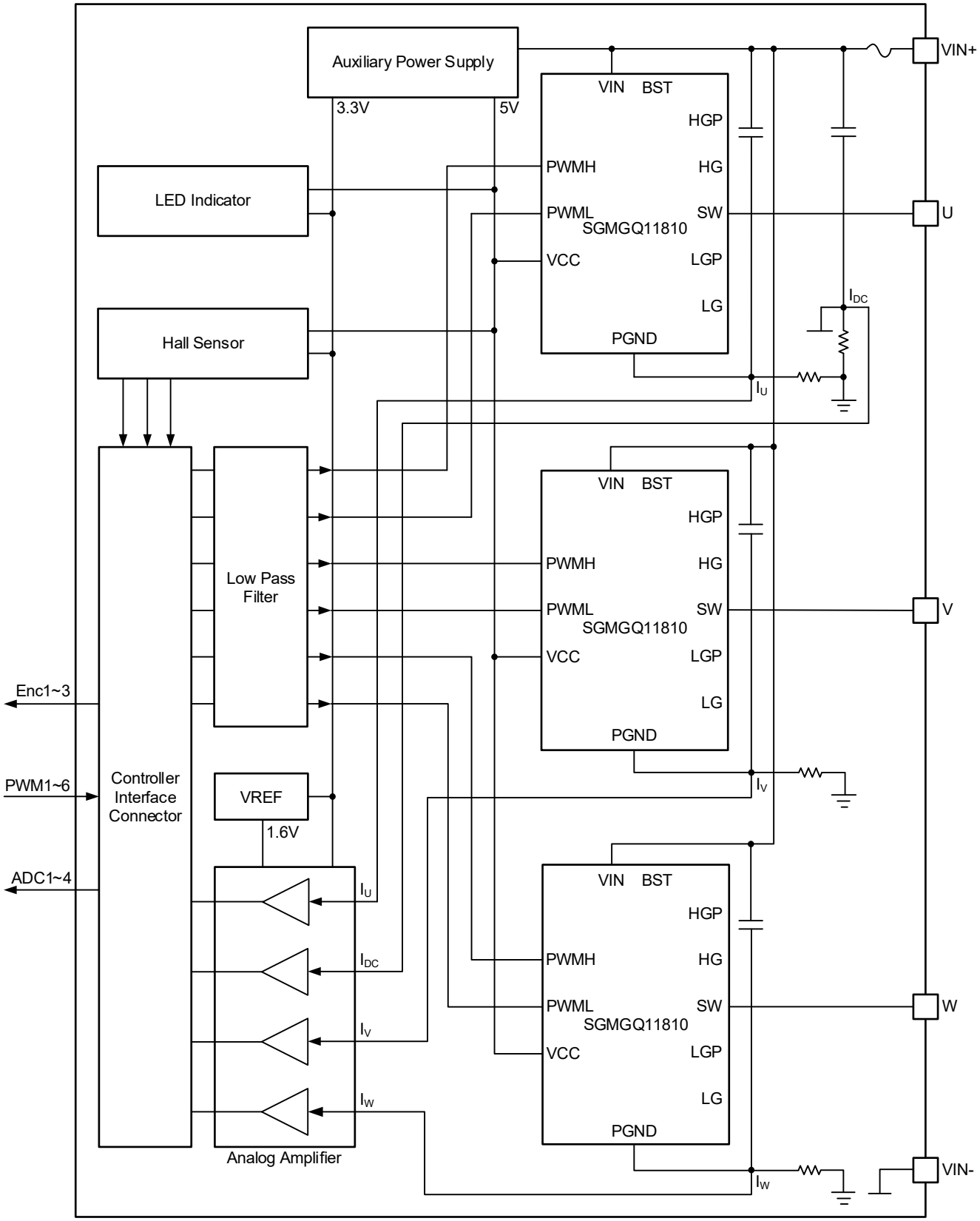



**Figure 28. 500W Continuous/1000W Pulse Power Capability Motor Driver**

# REVISION HISTORY

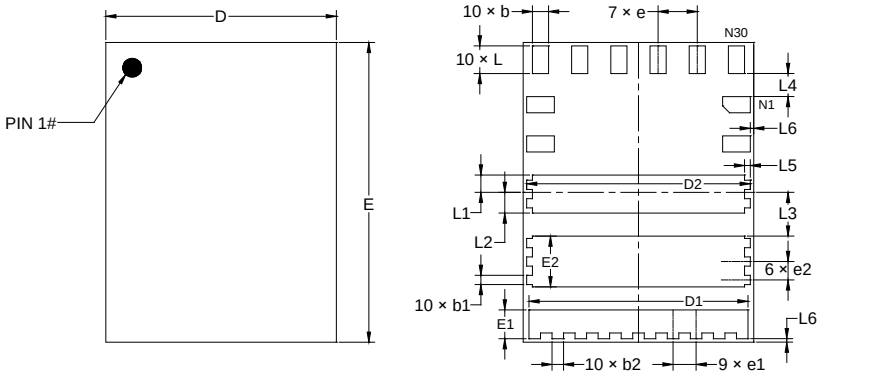
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

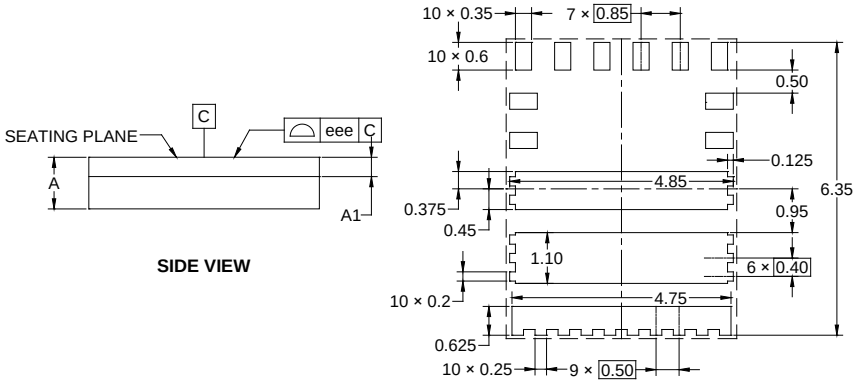
| AUGUST 2026 – REV.A to REV.A.1 | Page |
|---|---|
| Updated Layout Recommendation | 15 |

| Changes from Original to REV.A (JUNE 2026) | Page |
|---|---|
| Changed from product preview to production data | All |

# PACKAGE OUTLINE DIMENSIONS

## LGA-5×6.5-30L



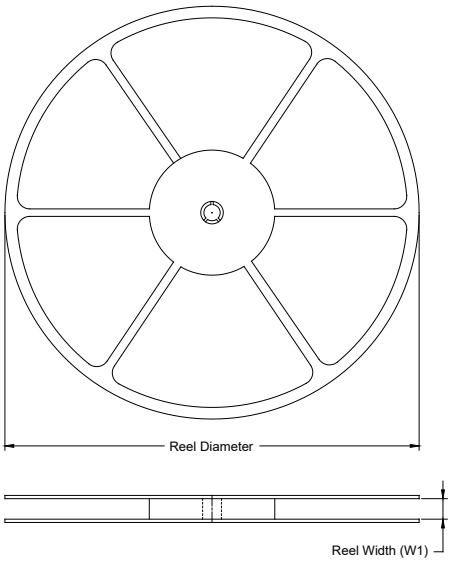

**RECOMMENDED LAND PATTERN** (Unit: mm)

| Symbol | Dimensions In Millimeters | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 1.020 | - | 1.220 |
| A1 | | 0.420 REF | |
| b | 0.300 | - | 0.400 |
| b1 | 0.150 | - | 0.250 |
| b2 | 0.200 | - | 0.300 |
| D | 4.900 | - | 5.100 |
| D1 | 4.650 | - | 4.850 |
| D2 | 4.750 | - | 4.950 |
| E | 6.400 | - | 6.600 |
| E1 | 0.525 | - | 0.725 |
| E2 | 1.000 | - | 1.200 |
| e | | 0.850 BSC | |
| e1 | | 0.500 BSC | |
| e2 | | 0.400 BSC | |
| L | 0.550 | - | 0.650 |
| L1 | | 0.375 REF | |
| L2 | | 0.450 REF | |
| L3 | | 0.950 REF | |
| L4 | | 0.500 REF | |
| L5 | | 0.125 REF | |
| L6 | | 0.075 REF | |
| eee | | 0.100 | |

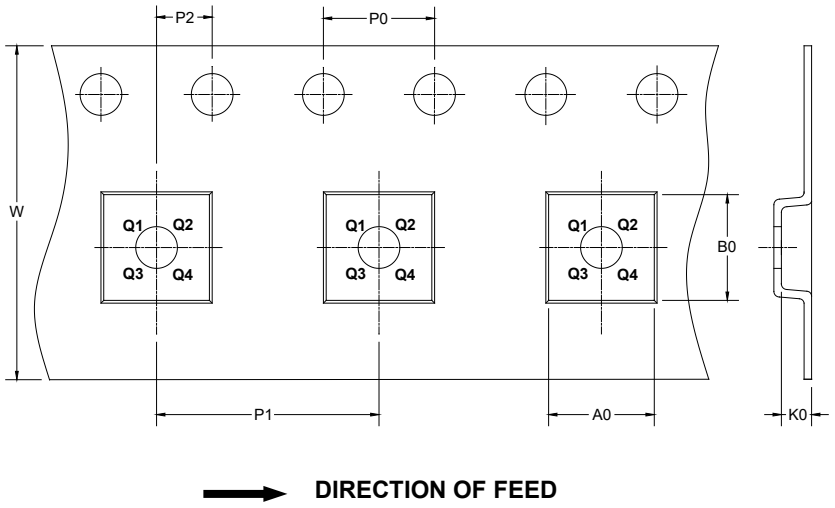
NOTE: This drawing is subject to change without notice.

# TAPE AND REEL INFORMATION

### REEL DIMENSIONS




### TAPE DIMENSIONS



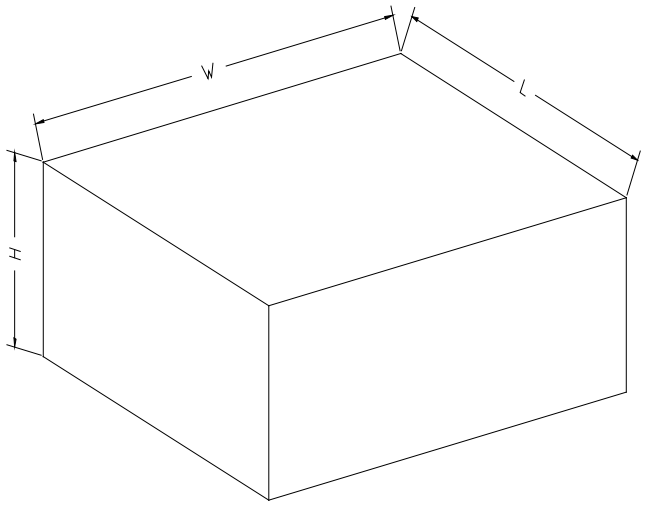

NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|
| LGA-5×6.5-30L | 13" | 16.4 | 5.30 | 6.80 | 1.38 | 4.0 | 12.0 | 2.0 | 16.0 | Q1 |

DD0001

## CARTON BOX DIMENSIONS




NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

| Reel Type | Length (mm) | Width (mm) | Height (mm) | Pizza/Carton |
|---|---|---|---|---|
| 13″ | 386 | 280 | 370 | 5 |

DD0002