Rev D, August 2026

1. 特性

- 车规级 AEC-Q100 认证
  - 器件温度等级 1：
    –40°C 至 125°C 工作环境温度
- 单 H 桥栅极驱动器
  - 驱动四个外部 N 沟道 MOSFET
  - 支持 100% PWM 占空比
- 电源电压范围：
  - 运行电压：5.5V 至 45V
  - 最大绝对额定值：55V
- 三种控制方式
  - PH/EN，独立 H-bridge 和标准 PWM
- SPI 接口(DR703Q)
- 智能栅极驱动架构
  - 可调转换率控制
  - 可调输出死区时间
- 支持 1.8V、3.3V 和 5V 逻辑输入
- 集成电流采样放大器
- 集成 PWM 电流调节
- 低功耗睡眠模式
- 保护功能
  - 电源欠压闭锁(UVLO)
  - 电荷泵欠压闭锁(CPUV)
  - 过流保护(OCP)
  - 栅极驱动器故障(GDF)
  - 热关断(TSD)
  - 看门狗定时器(DR703Q)
  - 故障状态输出管脚(nFAULT)

2. 应用

- 电动车窗升降器、天窗、座椅、推拉门和尾门
- 继电器驱动
- 电动驻车制动器(EPB)
- 直流有刷泵

3. 说明

DR702Q/703Q 是针对汽车应用的智能单 H 桥驱动器，可同时驱动四个外部 N 沟道 MOSFET 以驱动双向有刷直流电机。

DR702Q 支持硬件配置接口，DR703Q 支持 SPI 配置接口。两款器件均支持 PH/EN、独立 H-Bridge 或标准 PWM 接口，可实现正转、反转、慢刹(slow decay)、滑行(coast)等多种电机控制。此外，集成电荷泵架构支持 100% 占空比输出，也可用于驱动外部电池反接保护开关。DR702Q/703Q 还可以通过独立半桥模式以经济高效的方式顺序控制多个直流电机。

DR702Q/703Q 集成了电流采样放大器，并包含使用固定关断时间 PWM 电流斩波来调节绕组电流的功能。通过集成智能栅极驱动器模块，DR702Q/703Q 器件可以保护外部 FET，而无需额外增加任何外部栅极组件，如电阻器和齐纳二极管等。DR702Q/703Q 器件结合了保护功能和栅极驱动可配置性，以简化设计并将电机系统的智能提升到一个新的水平。例如，可配置死区时间优化可避免直通、有源/无源下拉，并防止 DV/DT 栅极转动；可编程转换率控制在降低 EMI 方面提供了灵活性。DR702Q/703Q 还集成了各种保护功能—UVLO、CPUV、OCP、TSD、GDF、看门狗定时器等。

DR702Q/703Q 器件采用 QFN-32 封装。有关订购信息，请参见 Table 1。

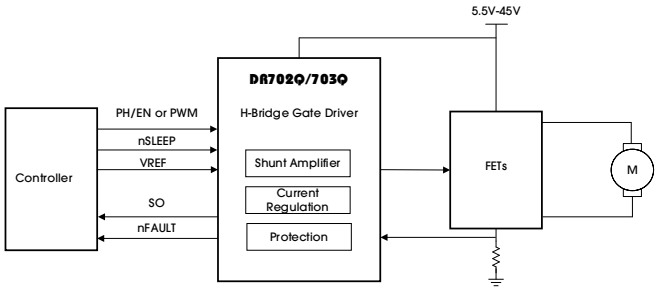


Table 1 lists the order information.

Table 1. Order Information

ORDER NUMBER[1]	PART NUMBER	MARK	PKG.	VM MAX (V)	INTERFACE	UNDERVOLTAGE PROTECT	BRIDGE	OPEN LOAD DETECT	OP. TEMP (°C)	MSL	PKG. OPTION
DR702QAQFN32	DR702Q	DR702Q XXXXXX XXXXX	QFN-32	55	Hardware	VM and VDRAIN	H-bridge	No	–40-125	2	T/R-4000
DR703QAQFN32	DR703Q	DR703Q XXXXXX XXXXX	QFN-32	55	SPI	VM and VDRAIN	H-bridge	No	–40-125	2	T/R-4000
DR702QBQFN32[3]	DR702Q	DR702Q XXXXXX XXXXX	QFN-32	55	Hardware	VM and VDRAIN	H-bridge	No	–40-125	2	T/R-4000
DR703QBQFN32[3]	DR703Q	DR703Q XXXXXX XXXXX	QFN-32	55	SPI	VM and VDRAIN	H-bridge	No	–40-125	2	T/R-4000

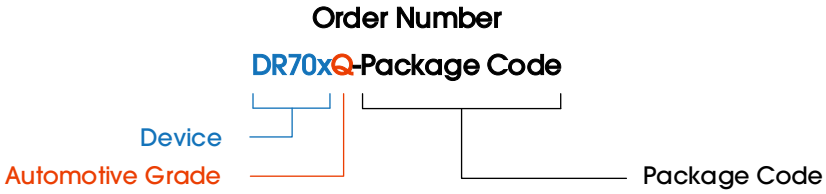
Table 2. Family Selection Guide

ORDER NUMBER[1]	PART NUMBER	MARK	PKG.	VM MAX (V)	INTERFACE	UNDERVOLTAGE PROTECT	BRIDGE	OPEN LOAD DETECT	OP. TEMP (°C)	MSL	PKG. OPTION
DR704QAQFN32	DR704Q	DR704Q XXXXXX XXXXX	QFN-32	55	SPI	VM and VDRAIN	H-bridge	Yes	–40-125	2	T/R-4000
DR704QBQFN32[3]	DR704Q	DR704Q XXXXXX XXXXX	QFN-32	55	SPI	VM and VDRAIN	H-bridge	Yes	–40-125	2	T/R-4000

Devices can be ordered via the following two ways:

1. Place orders directly on our website (www.analogysemi.com), or;
2. Contact our sales team by mailing to sales@analogysemi.com.

Note 1:



Note 2: "XXXXX": For internal use.
Note 3: This part does not affect specifications, software control, or hardware design. For new design, it is recommended that orders be placed for this part.

4. PIN CONFIGURATION AND FUNCTIONS

Figure 1 illustrates the pin configuration.

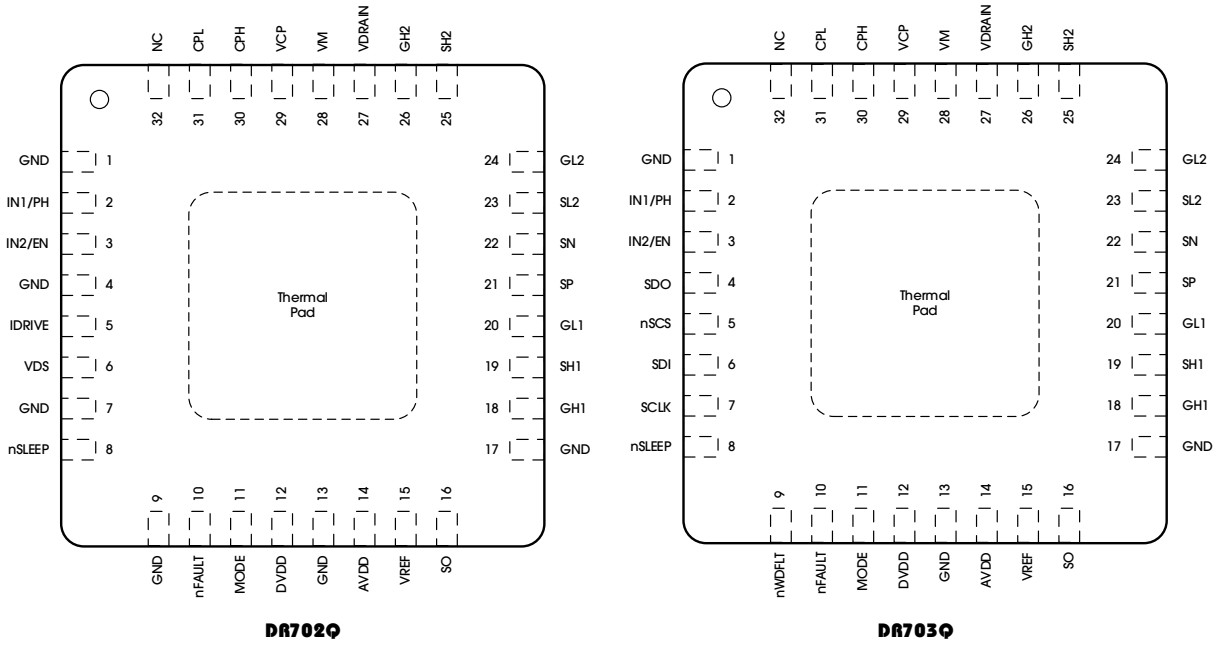


Figure 1. Pin Configuration

Table 3 lists the pin functions

Table 3. Pin Functions

POSITION		NAME	TYPE	DESCRIPTION
DR702Q	DR703Q			
1	1	GND	Power	Device ground. Connect this pin to the system ground.
2	2	IN1/PH	Input	Input control pins. The logic of this pin is dependent on the MODE pin. This pin is connected to an internal pulldown resistor.
3	3	IN2/EN	Input	Input control pins. The logic of this pin is dependent on the MODE pin. This pin is connected to an internal pulldown resistor.
4	—	GND	Power	NC or connect this pin to the system ground.
5	—	IDRIVE	Input	Current setting pin for the gate drive. The resistor value or voltage forced on this pin sets the gate drive current. For more information, see the IDRIVE CONFIGURATION section.
6	—	VDS	Input	VDS monitor setting pin. The resistor value or voltage forced on this pin sets the VDS monitor threshold. For more information, see the VDS CONFIGURATION section.
7	—	GND	Power	NC or connect this pin to the system ground.
8	8	nSLEEP	Input	Device sleep mode. Pull this pin to logic low to put device into a low-power sleep mode with the FETs in high impedance (Hi-Z). This pin is connected to an internal pulldown resistor.
9	—	GND	Power	NC or connect this pin to the system ground.
10	10	nFAULT	Open-Drain Output	Fault indication pin. This pin is pulled logic low when a fault condition occurs. This pin is an open-drain output that requires an external pullup resistor.
11	11	MODE	Input	Mode control pin. Pull this pin to logic low for H-bridge operation. Pull this pin to logic high for independent half-bridge operation. Leave it in Hi-Z state for standard PWM operation. This pin is connected to an internal resistor divider and features both internal pull-up and pull-down resistors. Operation of this pin is latched on power-up or when exiting sleep mode.
12	12	DVDD	Power	Logic regulator. This pin is the regulator for the 3.3V logic supply. Bypass this pin to ground with a 6.3V, 1µF ceramic capacitor.

POSITION		NAME	TYPE	DESCRIPTION
DR702Q	DR703Q			
13	13	GND	Power	Device ground. Connect this pin to the system ground.
14	14	AVDD	Power	Analog regulator. This pin is the 5V analog supply regulator. Bypass this pin to ground with a 6.3V, 1µF ceramic capacitor.
15	15	VREF	Input	Current set reference input. The voltage on this pin sets the driver chopping current.
16	16	SO	Output	Shunt amplifier output. The voltage on this pin is equal to the SP voltage times A_V plus an offset. Place no more than 1nF of capacitance on this pin.
17	17	GND	Power	Device ground. Connect this pin to the system ground.
18	18	GH1	Output	High-side gate. Connect this pin to the high-side FET gate.
19	19	SH1	Input	High-side source. Connect this pin to the high-side FET source.
20	20	GL1	Output	Low-side gate. Connect this pin to the low-side FET gate.
21	21	SP	Input	Shunt amplifier positive input. Connect this pin to the current-sense resistor.
22	22	SN	Input	Shunt amplifier negative input. Connect this pin to the current-sense resistor.
23	23	SL2	Input	Low-side source. Connect this pin to the low-side FET source.
24	24	GL2	Output	Low-side gate. Connect this pin to the low-side FET gate.
25	25	SH2	Input	High-side source. Connect this pin to the high-side FET source
26	26	GH2	Output	High-side gate. Connect this pin to the high-side FET gate.
27	27	VDRAIN	Input	High-side FET drain connection. This pin is common for the two H-bridges.
28	28	VM	Power	Power supply. Connect this pin to the motor supply voltage. Bypass this pin to ground with a 0.1µF ceramic plus a 10µF (minimum) capacitor.
29	29	VCP	Power	Charge-pump output. Connect a 16V, 1µF ceramic capacitor between this pin and the VM pin.
30	30	CPH	Power	Charge-pump switching node. Connect a 0.1µF X7R capacitor rated for the supply voltage (VM) between the CPH and CPL pins.
31	31	CPL	Power	Charge-pump switching node. Connect a 0.1µF X7R capacitor rated for the supply voltage (VM) between the CPH and CPL pins.
32	32	NC	No Connect	No connect. No internal connection.
—	7	SCLK	Input	SPI clock. This pin is for the SPI clock signal. This pin is connected to an internal pulldown resistor.
—	6	SDI	Input	SPI input. This pin is for the SPI input signal. This pin is connected to an internal pulldown resistor.
—	4	SDO	Open-Drain Output	SPI output. This pin is for the SPI output signal. This pin is an open-drain output that requires an external pullup resistor.
—	9	nWDFLT	Open-Drain Output	Watchdog fault indication pin. This pin is pulled logic low when a watchdog fault condition occurs. This pin is an open-drain output that requires an external pullup resistor.
—	5	nSCS	Input	SPI chip select. This pin is the select and enable for SPI. This pin is active low.

5. SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS

Table 4 lists the absolute maximum ratings of the DR702Q/703Q.

Table 4. Absolute Maximum Ratings

PARAMETER	DESCRIPTION		MIN	MAX	UNITS
Voltage	Power supply	VM	–0.3	55	V
	Charge pump	VCP, CPH	–0.3	V_{VM} + 12	
	Charge pump negative switching pin	CPL	–0.3	V_{VM}	
	Internal logic regulator	DVDD	–0.3	3.8	
	Internal analog regulator	AVDD	–0.3	5.75	
	Drain pin	VDRAIN	–0.3	55	
	Difference between supply and VDRAIN	VM – VDRAIN	–10	10	
	Control pin	IN1, IN2, nSLEEP, nFAULT, VREF, IDRIVE, VDS, MODE, nSCS, SCLK, SDI, SDO, nWDFLT	–0.3	5.75	
	High-side gate pin	GH1, GH2	–0.3	V_{VM} + 12	
	Low-side gate pin	GL1, GL2	–0.3	12	
	Continuous phase-node pin	SH1, SH2	–1.2	V_{VM} + 1.2	
	Pulsed 10µs phase-node pin	SH1, SH2	–2	V_{VM} + 2	
	Continuous shunt amplifier input pin	SP, SL2	–0.5	1.2	
		SN	–0.3	0.3	
	Pulsed 10µs shunt amplifier input pin	SP, SL2	–1	1.2	
	Shunt amplifier output pin voltage	SO	–0.3	5.75	
Current	Shunt amplifier output pin	SO	0	5	mA
	Maximum, limit with external series resistor	VDRAIN	–2	2	
	Open-drain output	nFAULT, SDO, nWDFLT	0	10	
	Gate pin source	GH1, GL1, GH2, GL2	0	250	
	Gate pin sink	GH1, GL1, GH2, GL2	0	500	
Temperature	Junction, T_J		–40	150	°C
	Storage, T_{stg}		–65	150	

Note: Stresses beyond those listed under Table 4 may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Table 6. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD RATINGS

Table 5 lists the ESD ratings of the DR702Q/703Q.

Table 5. ESD Ratings

PARAMETER	SYMBOL	DESCRIPTION	VALUE	UNITS
Electrostatic Discharge	$V_{(ESD)}$	Human-body model (HBM), per AEC Q100-002	±5000	V
		Charged-device model (CDM), per AEC Q100-011	±2000	

5.3 RECOMMENDED OPERATING CONDITIONS

Table 6 lists the recommended operating conditions for the DR702Q/703Q.

Table 6. Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Power Supply Voltage, VM	V_{VM}	5.5	45	V
Logic-Level Input Voltage	V_{CC}	0	5.25	V
Current Shunt Amplifier Reference Voltage, VREF	V_{VREF}	0.3(1)	3.6	V
Applied PWM Signal (IN1/IN2), IN1, IN2	$f_{(PWM)}$		100	kHz
AVDD External Load Current	I_{AVDD}		30(2)	mA
DVDD External Load Current	I_{DVDD}		30(2)	mA
Shunt Amplifier Output-Current Loading, SO	I_{SO}		5	mA
Operating Ambient Temperature	T_A	–40	125	°C

Note 1: Operational at V_{VREF} = 0 to approximately 0.3V, but accuracy is degraded.
Note 2: Power dissipation and thermal limits must be observed.

5.4 THERMAL INFORMATION

Table 7 lists the thermal information for the DR702Q/703Q.

Table 7. Thermal Information

PARAMETER	SYMBOL	QFN-32	UNITS
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	29.7	°C/W
Junction-to-Board Thermal Resistance	$R_{\theta JB}$	7.3	°C/W
Junction-to-Top Characterization Parameter	ψ_{JT}	0.3	°C/W
Junction-to-Board Characterization Parameter	ψ_{JB}	7.3	°C/W
Junction-to-Case (Top) Thermal Resistance	$R_{\theta JC(top)}$	28.7	°C/W
Junction-to-Case (Bottom) Thermal Resistance	$R_{\theta JC(bot)}$	—	°C/W

5.5 ELECTRICAL CHARACTERISTICS

Table 8 lists the electrical characteristics of the DR702Q/703Q. Over recommended operating conditions unless otherwise noted. Typical limits apply for T_A = 25°C and V_{VM} = 13.5V.

Table 8. Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES (VM, AVDD, DVDD)						
VM Operating Voltage	V_{VM}	Gate drivers functional	5.5		45	V
		Logic functional	4.5		45	
VM Operating Supply Current	I_{VM}	V_{VM} = 13.5V; nSLEEP = 1	5	6	7	mA
VM Sleep Mode Supply Current	$I_{(SLEEP)}$	nSLEEP = 0, V_{VM} = 13.5V, T_A = 25°C		3.4	4.6	µA
		nSLEEP = 0, V_{VM} = 13.5V, T_A = 125°C(1)			7	
Internal Logic Regulator Voltage	V_{DVDD}	2mA load	3	3.3	3.5	V
		30mA load, V_{VM} = 13.5V	2.9	3.2	3.5	
Internal Logic Regulator Voltage	V_{AVDD}	2mA load	4.7	5	5.3	V
		30mA load, V_{VM} = 13.5V	4.6	5	5.3	
CHARGE PUMP (VCP, CPH, CPL)						
VCP Operating Voltage	V_{VCP}	V_{VM} = 13.5V; I_{VCP} = 0mA to 12mA	22.5	23.6	25	V
		V_{VM} = 8V; I_{VCP} = 0mA to 10mA	13.4	13.7	15	
		V_{VM} = 5.5V; I_{VCP} = 0mA to 8mA	8.7	8.8	10.5	
Charge-Pump Current Capacity	I_{VCP}	V_{VM} > 13.5V	12			mA
		8V < V_{VM} < 13.5V	10			
		5.5V < V_{VM} < 8V	8			
CONTROL INPUTS (IN1/PH, IN2/EN, nSLEEP, MODE, nSCS, SCLK, SDI)						
Input Logic-Low Voltage	V_{IL}		0		0.8	V
Input Logic-High Voltage	V_{IH}		1.5		5.25	V
Input Logic Hysteresis	V_{hys}			100		mV
Input Logic-Low Current	I_{IL}	V_{IN} = 0V	–1		1	µA
Input Logic-High Current	I_{IH}	V_{IN} = 5V			65	µA
Pulldown Resistance	R_{PD}	IN1/PH, IN2/EN, nSLEEP, nSCS, SCLK, SDI	64	100	173	kΩ
Pulldown Resistance	R_{PD}	MODE		65		kΩ
Pullup Resistance	R_{PU}	MODE		26		kΩ
CONTROL OUTPUTS (nFAULT, WDFAULT, SDO)						
Output Logic-Low Voltage	V_{OL}	I_O = 2mA			0.15	V
Output High-Impedance Leakage	I_{OZ}	5V pullup voltage	–1		1	µA
FET GATE DRIVERS (GH1, GH2, SH1, SH2, GL1, GL2)						
High-Side V_{GS} Gate Drive (Gate-to-Source)	V_{GSH}	V_{VM} > 13.5V; V_{GSH} with respect to SHx		10.2	11	V
		V_{VM} = 8V; V_{GSH} with respect to SHx	5.7	6.5	6.8	
		V_{VM} = 5.5V; V_{GSH} with respect to SHx	3.4	4	4.5	
Low-Side V_{GS} Gate Drive (Gate-to-Source)	V_{GSL}	V_{VM} > 10.5V		10.2		V
		V_{VM} < 10.5V	V_{VM} – 2			

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High-Side Peak Source Current (V_{VM} = 5.5V)	$I_{DRIVE(SRC_HS)}$	$R_{(IDRIVE)}$ < 1kΩ to GND (DR702Q) or IDRIVE = 3'b000 (DR703Q)		6		mA
		$R_{(IDRIVE)}$ = 33kΩ to GND (DR702Q) or IDRIVE = 3'b001 (DR703Q)		12		
		$R_{(IDRIVE)}$ = 200kΩ to GND (DR702Q) or IDRIVE = 3'b010 (DR703Q)		30		
		IDRIVE = 3'b011 (DR703Q)		42		
		IDRIVE = 3'b100 (DR703Q)		60		
		$R_{(IDRIVE)}$ > 2MΩ to GND (DR702Q) or IDRIVE = 3'b101 (DR703Q)		100		
		$R_{(IDRIVE)}$ = 68kΩ to AVDD (DR702Q) or IDRIVE = 3'b110 (DR703Q)		130		
		$R_{(IDRIVE)}$ = 1kΩ to AVDD (DR702Q) or IDRIVE = 3'b111 (DR703Q)		160		
High-Side Peak Sink Current (V_{VM} = 5.5V)	$I_{DRIVE(SNK_HS)}$	$R_{(IDRIVE)}$ < 1kΩ to GND (DR702Q) or IDRIVE = 3'b000 (DR703Q)		14		mA
		$R_{(IDRIVE)}$ = 33kΩ to GND (DR702Q) or IDRIVE = 3'b001 (DR703Q)		28		
		$R_{(IDRIVE)}$ = 200kΩ to GND (DR702Q) or IDRIVE = 3'b010 (DR703Q)		72		
		IDRIVE = 3'b011 (DR703Q)		100		
		IDRIVE = 3'b100 (DR703Q)		140		
		$R_{(IDRIVE)}$ > 2MΩ to GND (DR702Q) or IDRIVE = 3'b101 (DR703Q)		180		
		$R_{(IDRIVE)}$ = 68kΩ to AVDD (DR702Q) or IDRIVE = 3'b110 (DR703Q)		250		
		$R_{(IDRIVE)}$ = 1kΩ to AVDD (DR702Q) or IDRIVE = 3'b111 (DR703Q)		320		
Low-Side Peak Source Current (V_{VM} = 5.5V)	$I_{DRIVE(SRC_LS)}$	$R_{(IDRIVE)}$ < 1kΩ to GND (DR702Q) or IDRIVE = 3'b000 (DR703Q)		8		mA
		$R_{(IDRIVE)}$ = 33kΩ to GND (DR702Q) or IDRIVE = 3'b001 (DR703Q)		16		
		$R_{(IDRIVE)}$ = 200kΩ to GND (DR702Q) or IDRIVE = 3'b010 (DR703Q)		39		
		IDRIVE = 3'b011 (DR703Q)		54		
		IDRIVE = 3'b100 (DR703Q)		77		
		$R_{(IDRIVE)}$ > 2MΩ to GND (DR702Q) or IDRIVE = 3'b101 (DR703Q)		100		
		$R_{(IDRIVE)}$ = 68kΩ to AVDD (DR702Q) or IDRIVE = 3'b110 (DR703Q)		139		
		$R_{(IDRIVE)}$ = 1kΩ to AVDD (DR702Q) or IDRIVE = 3'b111 (DR703Q)		178		
Low-Side Peak Sink Current (V_{VM} = 5.5V)	$I_{DRIVE(SNK_LS)}$	$R_{(IDRIVE)}$ < 1kΩ to GND (DR702Q) or IDRIVE = 3'b000 (DR703Q)		17		mA
		$R_{(IDRIVE)}$ = 33kΩ to GND (DR702Q) or IDRIVE = 3'b001 (DR703Q)		35		
		$R_{(IDRIVE)}$ = 200kΩ to GND (DR702Q) or IDRIVE = 3'b010 (DR703Q)		75		
		IDRIVE = 3'b011 (DR703Q)		108		
		IDRIVE = 3'b100 (DR703Q)		158		
		$R_{(IDRIVE)}$ > 2MΩ to GND (DR702Q) or IDRIVE = 3'b101 (DR703Q)		204		
		$R_{(IDRIVE)}$ = 68kΩ to AVDD (DR702Q) or IDRIVE = 3'b110 (DR703Q)		280		
		$R_{(IDRIVE)}$ = 1kΩ to AVDD (DR702Q) or IDRIVE = 3'b111 (DR703Q)		360		

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High-Side Peak Source Current (V_{VM} = 13.5V)	$I_{DRIVE(SRC_HS)}$	$R_{(IDRIVE)}$ < 1kΩ to GND (DR702Q) or IDRIVE = 3'b000 (DR703Q)		10		mA
		$R_{(IDRIVE)}$ = 33kΩ to GND (DR702Q) or IDRIVE = 3'b001 (DR703Q)		20		
		$R_{(IDRIVE)}$ = 200kΩ to GND (DR702Q) or IDRIVE = 3'b010 (DR703Q)		48		
		IDRIVE = 3'b011 (DR703Q)		67		
		IDRIVE = 3'b100 (DR703Q)		95		
		$R_{(IDRIVE)}$ > 2MΩ to GND (DR702Q) or IDRIVE = 3'b101 (DR703Q)		152		
		$R_{(IDRIVE)}$ = 68kΩ to AVDD (DR702Q) or IDRIVE = 3'b110 (DR703Q)		199		
		$R_{(IDRIVE)}$ = 1kΩ to AVDD (DR702Q) or IDRIVE = 3'b111 (DR703Q)		245		
High-Side Peak Sink Current (V_{VM} = 13.5V)	$I_{DRIVE(SNK_HS)}$	$R_{(IDRIVE)}$ < 1kΩ to GND (DR702Q) or IDRIVE = 3'b000 (DR703Q)		20		mA
		$R_{(IDRIVE)}$ = 33kΩ to GND (DR702Q) or IDRIVE = 3'b001 (DR703Q)		40		
		$R_{(IDRIVE)}$ = 200kΩ to GND (DR702Q) or IDRIVE = 3'b010 (DR703Q)		100		
		IDRIVE = 3'b011 (DR703Q)		140		
		IDRIVE = 3'b100 (DR703Q)		200		
		$R_{(IDRIVE)}$ > 2MΩ to GND (DR702Q) or IDRIVE = 3'b101 (DR703Q)		253		
		$R_{(IDRIVE)}$ = 68kΩ to AVDD (DR702Q) or IDRIVE = 3'b110 (DR703Q)		354		
		$R_{(IDRIVE)}$ = 1kΩ to AVDD (DR702Q) or IDRIVE = 3'b111 (DR703Q)		454		
Low-Side Peak Source Current (V_{VM} = 13.5V)	$I_{DRIVE(SRC_LS)}$	$R_{(IDRIVE)}$ < 1kΩ to GND (DR702Q) or IDRIVE = 3'b000 (DR703Q)		10		mA
		$R_{(IDRIVE)}$ = 33kΩ to GND (DR702Q) or IDRIVE = 3'b001 (DR703Q)		20		
		$R_{(IDRIVE)}$ = 200kΩ to GND (DR702Q) or IDRIVE = 3'b010 (DR703Q)		50		
		IDRIVE = 3'b011 (DR703Q)		70		
		IDRIVE = 3'b100 (DR703Q)		100		
		$R_{(IDRIVE)}$ > 2MΩ to GND (DR702Q) or IDRIVE = 3'b101 (DR703Q)		120		
		$R_{(IDRIVE)}$ = 68kΩ to AVDD (DR702Q) or IDRIVE = 3'b110 (DR703Q)		170		
		$R_{(IDRIVE)}$ = 1kΩ to AVDD (DR702Q) or IDRIVE = 3'b111 (DR703Q)		220		
Low-Side Peak Sink Current (V_{VM} = 13.5V)	$I_{DRIVE(SNK_LS)}$	$R_{(IDRIVE)}$ < 1kΩ to GND (DR702Q) or IDRIVE = 3'b000 (DR703Q)		20		mA
		$R_{(IDRIVE)}$ = 33kΩ to GND (DR702Q) or IDRIVE = 3'b001 (DR703Q)		40		
		$R_{(IDRIVE)}$ = 200kΩ to GND (DR702Q) or IDRIVE = 3'b010 (DR703Q)		87		
		IDRIVE = 3'b011 (DR703Q)		125		
		IDRIVE = 3'b100 (DR703Q)		184		
		$R_{(IDRIVE)}$ > 2MΩ to GND (DR702Q) or IDRIVE = 3'b101 (DR703Q)		240		
		$R_{(IDRIVE)}$ = 68kΩ to AVDD (DR702Q) or IDRIVE = 3'b110 (DR703Q)		325		
		$R_{(IDRIVE)}$ = 1kΩ to AVDD (DR702Q) or IDRIVE = 3'b111 (DR703Q)		422		

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FET Holding Current	I_{HOLD}	Source current after t_{DRIVE}		10		mA
		Sink current after t_{DRIVE}		40		
FET Holdoff Strong Pulldown	I_{STRONG}	GHx		750		mA
		GLx		1000		
FET Gate Holdoff Resistor	$R_{(OFF)}$	Pulldown GHx to SHx		200		kΩ
		Pulldown GLx to GND		150		
CURRENT SHUNT AMPLIFIER AND PWM CURRENT CONTROL (SP, SN, SO, VREF)						
VREF Input rms Voltage	V_{VREF}	For current internal chopping	0.3(2)		3.6	V
VREF Input Impedance	R_{VREF}	DR702Q and DR703Q VREF_SCL = 00 (100%)	1			MΩ
		DR703Q VREF_SCL = 2'b01, 2'b10 or 2'b11		200		kΩ
Amplifier Gain (DR702Q)	A_V	60mV < V_{SP} < 225mV; V_{SN} = GND	19.3	19.8	20.3	V/V
Amplifier Gain (DR703Q)	A_V	GAIN_CS = 00; 10mV < V_{SP} < 450mV; V_{SN} = GND	9.75	10	10.25	V/V
		GAIN_CS = 01; 60mV < V_{SP} < 225mV; V_{SN} = GND	19.3	19.8	20.3	
		GAIN_CS = 10; 10mV < V_{SP} < 112mV; V_{SN} = GND	38.4	39.4	40.4	
		GAIN_CS = 11; 10mV < V_{SP} < 56mV; V_{SN} = GND	74	78	81	
Input-Referred Offset	V_{IO}	V_{SP} = V_{SN} = GND		3.7	7	mV
Drift Offset(2)	$V_{IO(DRIFT)}$	V_{SP} = V_{SN} = GND		3.8		µV/°C
SP Input Current	I_{SP}	V_{SP} = 100mV; V_{SN} = GND, VDS = 0.96V		–20		µA
SO Pin Output Voltage Range	V_{SO}		A_V × V_{IO}		4.5	V
Allowable SO Pin Capacitance	$C_{(SO)}$				1	nF
PROTECTION CIRCUITS						
VM Undervoltage Lockout	$V_{(UVLO2)}$	VM falling; UVLO2 report		5.25		V
		VM rising; UVLO2 recovery		5.4	5.65	
Logic Undervoltage Lockout	$V_{(UVLO1)}$				4.5	V
VM Undervoltage Hysteresis	$V_{hys(UVLO)}$	Rising to falling threshold	100			mV
Charge Pump Undervoltage	$V_{(CP_UV)}$	VCP falling; CPUV report	V_{VM} + 1.5			V
		VCP rising; CPUV recovery	V_{VM} + 1.55			
CP Undervoltage Hysteresis	$V_{hys(CP_UV)}$	Rising to falling threshold		50		mV
Overcurrent Protection Trip Level, V_{DS} of Each External FET (DR702Q) High side FETs: VDRAIN SHx Low Side FETs: SHx SP/SL2	$V_{DS(OCP)}$	$R_{(VDS)}$ < 1kΩ to GND		0.06		V
		$R_{(VDS)}$ = 33kΩ to GND		0.12		
		$R_{(VDS)}$ = 200kΩ to GND		0.24		
		$R_{(VDS)}$ > 2MΩ to GND		0.48		
		$R_{(VDS)}$ = 68kΩ to AVDD		0.96		
		$R_{(VDS)}$ < 1kΩ to AVDD	Disabled			
Overcurrent Protection Trip Level, V_{DS} of Each External FET (DR703Q) High-Side FETs: VDRAIN SHx Low-Side FETs: SHx SP/SL2	$V_{DS(OCP)}$	VDS_LEVEL = 3'b000		0.06		V
		VDS_LEVEL = 3'b001		0.145		
		VDS_LEVEL = 3'b010		0.17		
		VDS_LEVEL = 3'b011		0.2		
		VDS_LEVEL = 3'b100		0.12		
		VDS_LEVEL = 3'b101		0.24		
		VDS_LEVEL = 3'b110		0.48		
		VDS_LEVEL = 3'b111		0.96		
Overcurrent Protection Trip Level, Measured by Sense Amplifier	$V_{SP(OCP)}$	V_{SP} with respect to GND	0.7	1	1.4	V
Thermal Warning Temperature(1)	$T_{(OTW)}$	Die temperature T_J		135		°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Shutdown Temperature(1)	T_{SD}	Die temperature T_J		153		°C
Thermal Shutdown Hysteresis(1)	T_{hys}	Die temperature T_J		20		°C
Gate-Drive Clamping Voltage	$V_{C(GS)}$	Positive clamping voltage	14	14.7	16	V
		Negative clamping voltage	–1.1	–0.85	–0.6	

Note 1: Ensured by design and characterization data.
Note 2: Operational at V_{VREF} = 0 to approximately 0.3V, but accuracy is degraded.

5.6 SPI TIMING REQUIREMENTS

Table 9 lists the SPI timing.

Table 9. SPI Timing

PARAMETER	SYMBOL	MIN	NOM	MAX	UNITS
Minimum SPI Clock Period	$t_{(CLK)}$	125			ns
Clock High Time	$t_{(CLKH)}$	62.5			ns
Clock Low Time	$t_{(CLKL)}$	62.5			ns
SDI Input Data Setup Time	$t_{(SU_SDI)}$	20			ns
SDI Input Data Hold Time	$t_{(HD_SDI)}$	30			ns
SDO Output Hold Time	$t_{(HD_SDO)}$	50			ns
SCS Setup Time	$t_{(SU_SCS)}$	50			ns
SCS Hold Time	$t_{(HD_SCS)}$	50			ns
SCS Minimum High Time Before SCS Active Low	$t_{(HI_SCS)}$	400			ns

5.7 SWITCHING CHARACTERISTICS

Table 10 lists the switching characteristics.

Table 10. Switching Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES (VM, AVDD, DVDD)						
Sleep Time	$t_{(SLEEP)}$	nSLEEP = low to sleep mode			100	µs
Wake-Up Time	$t_{(wu)}$	nSLEEP = high to output change			1	ms
Turn On Time	t_{on}	VM > UVLO2 to output transition			1	ms
CHARGE PUMP (VCP, CPH, CPL)						
Charge-Pump Switching Frequency	$f_{S(VCP)}$	VM > UVLO2	250	400	550	kHz
CONTROL INPUTS (IN1, IN2, nSLEEP, MODE, nSCS, SCLK, SDI, PH, EN)						
Propagation Delay	t_{PD}	IN1, IN2 to GHx or GLx		300		ns
FET GATE DRIVERS (GH1, GH2, SH1, SH2, GL1, GL2)						
Output Dead Time (DR702Q)	$t_{(DEAD)}$	Observed $t_{(DEAD)}$ depends on IDRIVE setting		240		ns
Output Dead Time (DR703Q)	$t_{(DEAD)}$	TDEAD = 2'b00; Observed $t_{(DEAD)}$ depends on IDRIVE setting		120		ns
		TDEAD = 2'b01; Observed $t_{(DEAD)}$ depends on IDRIVE setting		240		
		TDEAD = 2'b10; Observed $t_{(DEAD)}$ depends on IDRIVE setting		480		
		TDEAD = 2'b11; Observed $t_{(DEAD)}$ depends on IDRIVE setting		960		
Gate Drive Time	$t_{(DRIVE)}$			2.5		µs
CURRENT SHUNT AMPLIFIER AND PWM CURRENT CONTROL (SP, SN, SO, VREF)						
Settling Time to ±1%(1)	t_S	V_{SP} = V_{SN} = GND to V_{SP} = 240mV, V_{SN} = GND, A_V = 10; $C_{(SO)}$ = 200pF			0.5	µs
		V_{SP} = V_{SN} = GND to V_{SP} = 120mV, V_{SN} = GND, A_V = 20; $C_{(SO)}$ = 200pF			1	
		V_{SP} = V_{SN} = GND to V_{SP} = 60mV, V_{SN} = GND, A_V = 40; $C_{(SO)}$ = 200pF			2	
		V_{SP} = V_{SN} = GND to V_{SP} = 30mV, V_{SN} = GND, A_V = 80; $C_{(SO)}$ = 200pF			4	

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWM Off-Time (DR702Q)	t_{off}			25		μs
PWM Off-Time (DR703Q)	t_{off}	t_{off} = 00		25		μs
		t_{off} = 01		50		
		t_{off} = 10		100		
		t_{off} = 11		200		
PWM Blanking Time	$t_{(BLANK)}$			2		μs
PROTECTION CIRCUITS						
VM UVLO Falling Deglitch Time	$t_{(UVLO)}$	VM falling; UVLO report		10		μs
Overcurrent Deglitch Time	$t_{(OCP)}$			4		μs
Overcurrent Retry Time	$t_{(RETRY)}$		2.8	3	3.2	ms
Watchdog Time Out (DR703Q)	$t_{(WD)}$	WD_DLY = 2'b00		10		ms
		WD_DLY = 2'b01		20		
		WD_DLY = 2'b10		50		
		WD_DLY = 2'b11		100		
Watchdog Timer Reset Period	$t_{(RESET)}$			64		μs
SPI						
SPI Read After Power On	$t_{(SPI_READY)}$	VM > VUVLO1			10	ms
SDO Output Data Delay Time, CLK High to SDO Valid	$t_{d(SDO)}$	C_L = 20pF		50		ns
SCS Access Time, SCS Low to SDO Out of High Impedance	t_a			100		ns
SCS Disable Time, SCS High to SDO High Impedance	t_{dis}			50		ns

Note: Ensured by design.

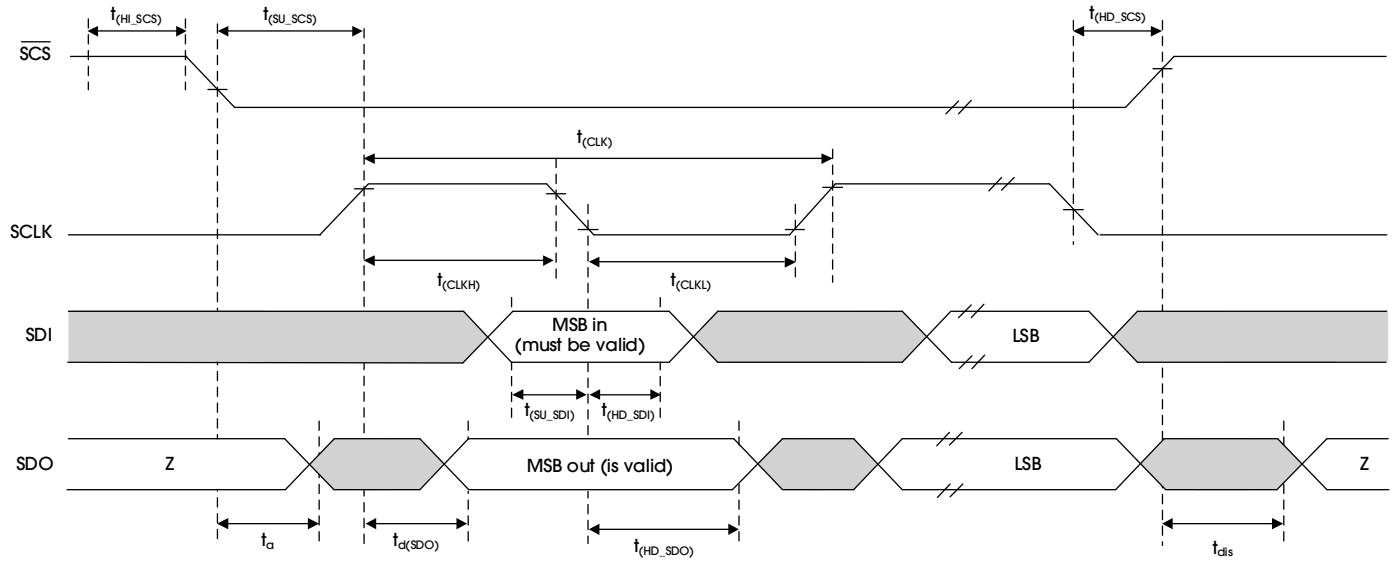


Figure 2. SPI Slave Mode Timing Diagram

6. TYPICAL CHARACTERISTICS

V_{VM} = 13.5V and T_A = 25°C, unless otherwise noted.

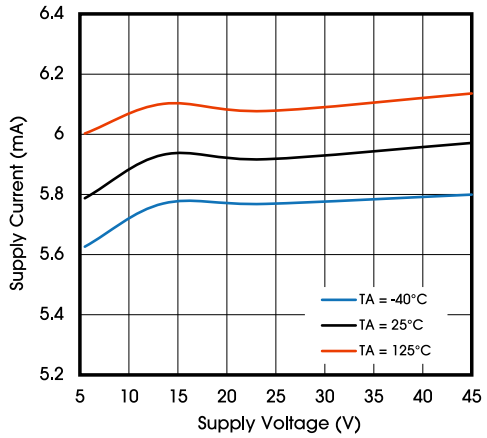


Figure 3. Supply Current vs. Supply Voltage (VM)

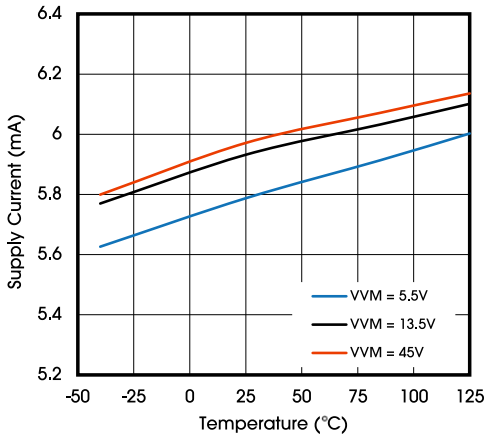


Figure 4. Supply Current vs. Temperature

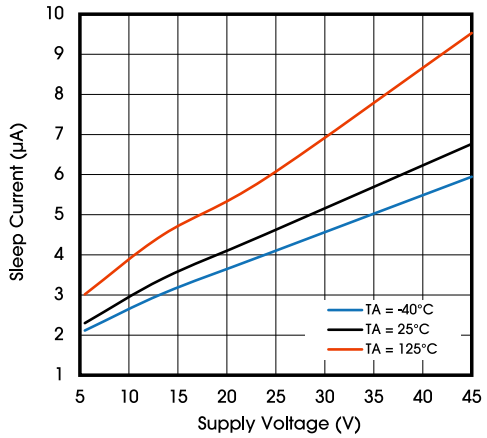


Figure 5. Sleep Current vs. Supply Voltage (VM)

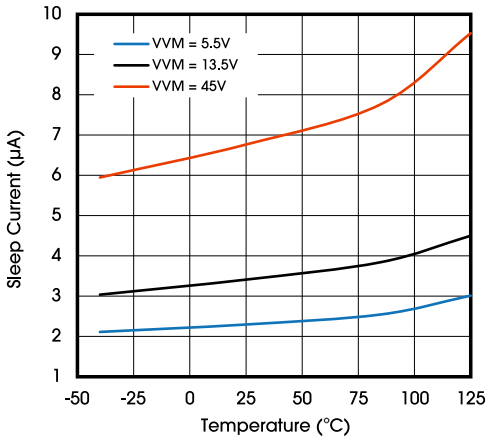


Figure 6. Sleep Current vs. Temperature

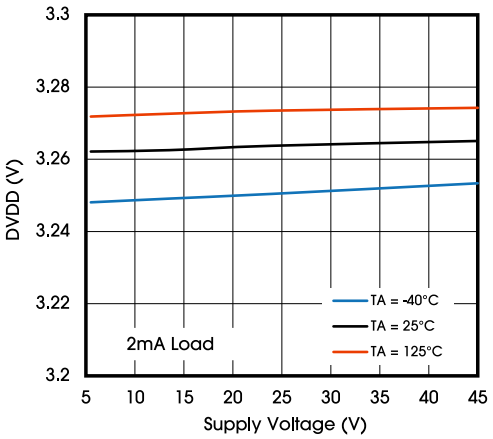


Figure 7. DVDD Regulator (2mA Load)

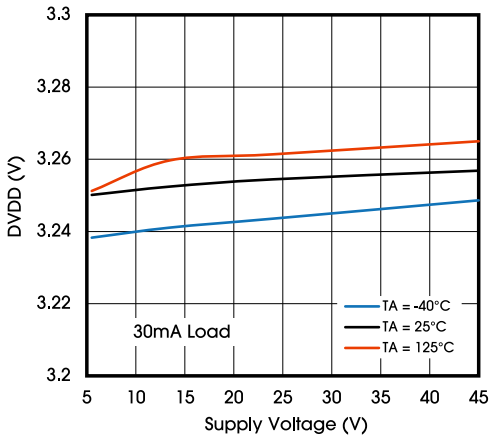


Figure 8. DVDD Regulator (30mA Load)

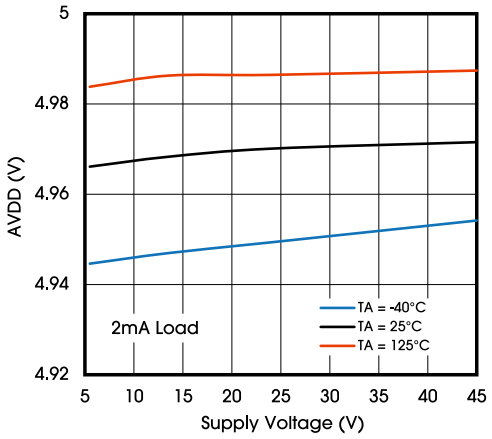


Figure 9. AVDD Regulator (2mA Load)

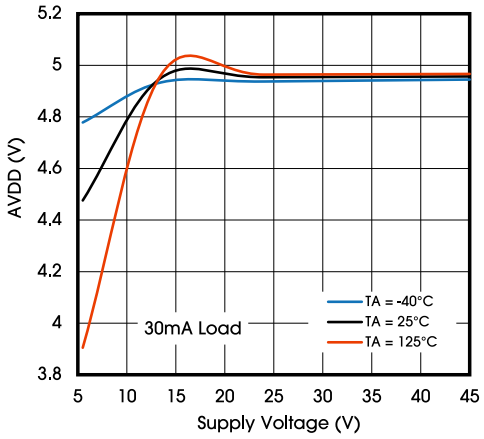


Figure 10. AVDD Regulator (30mA Load)

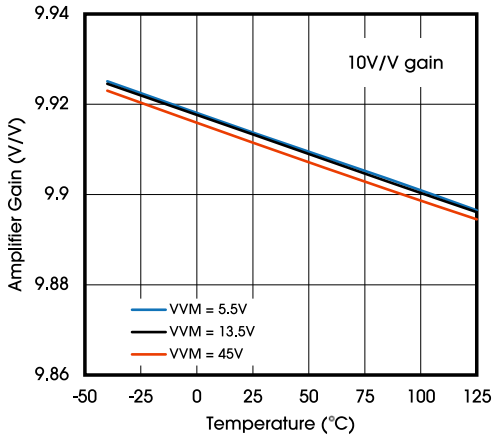


Figure 11. Amplifier Gain vs. Temperature, 10V/V Gain

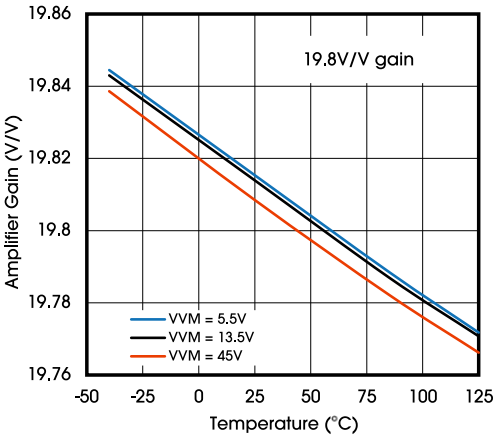


Figure 12. Amplifier Gain vs. Temperature, 19.8V/V Gain

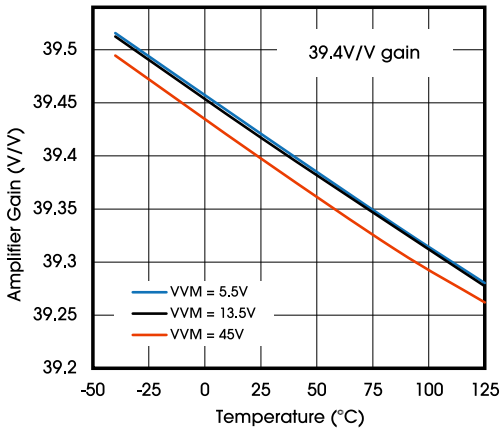


Figure 13. Amplifier Gain vs. Temperature, 39.4V/V Gain

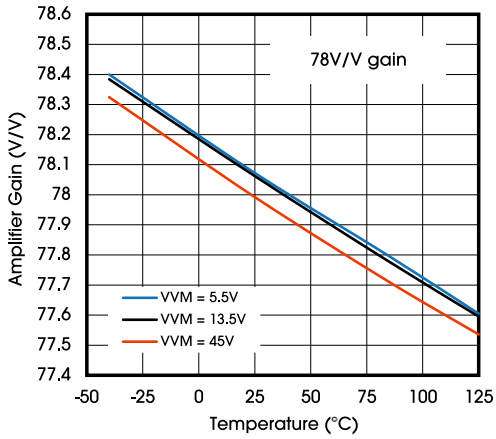


Figure 14. Amplifier Gain vs. Temperature, 78V/V Gain

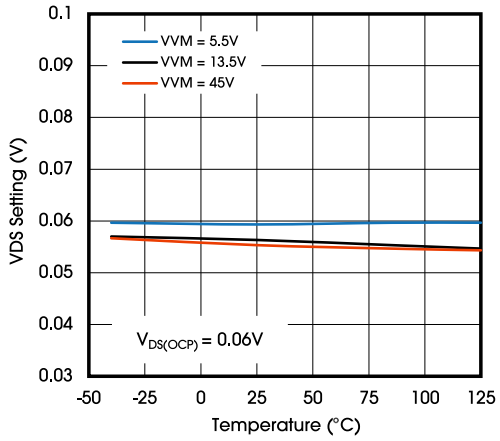


Figure 15. OCP Threshold Voltage vs. Temperature, $V_{DS(OCP)}$ = 0.06V

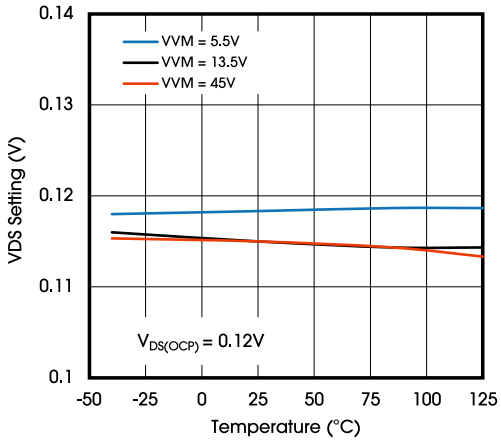


Figure 16. OCP Threshold Voltage vs. Temperature, $V_{DS(OCP)}$ = 0.12V

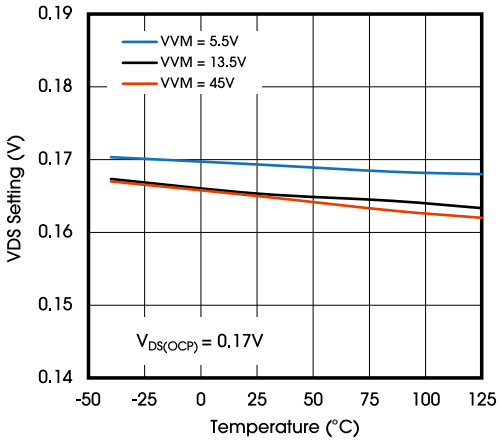


Figure 17. OCP Threshold Voltage vs. Temperature, $V_{DS(OCP)}$ = 0.17V

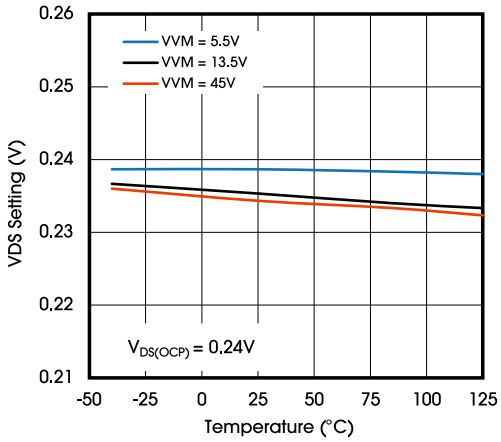


Figure 18. OCP Threshold Voltage vs. Temperature, $V_{DS(OCP)}$ = 0.24V

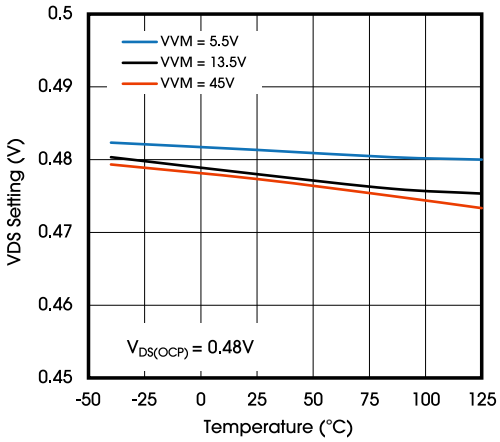


Figure 19. OCP Threshold Voltage vs. Temperature, $V_{DS(OCP)}$ = 0.48V

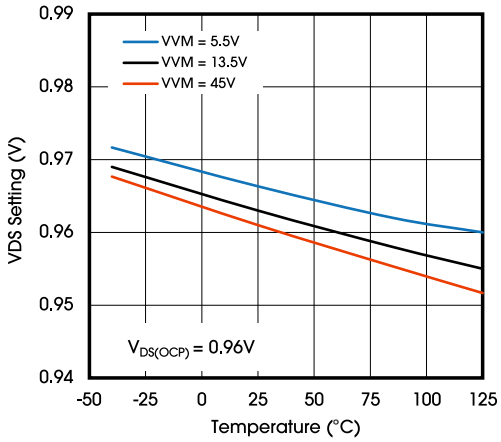


Figure 20. OCP Threshold Voltage vs. Temperature, $V_{DS(OCP)}$ = 0.96V

7. 详细说明

7.1 概述

DR702Q 和 DR703Q 是用于汽车应用的智能单 H 桥驱动器，可驱动四个外部 N 沟道 MOSFET 以实现双向有刷直流电机。DR702Q 支持硬件配置接口，DR703Q 支持 SPI 配置接口。两款器件均支持 PH/EN、独立 H-Bridge 或标准 PWM 接口，可实现正向、反向、滑行、慢衰减等多种电机控制。DR702Q/703Q 可以通过独立半桥模式以经济高效的方式顺序控制两个单向有刷直流电机。这些器件可支持 5.5V 至 45V 的电源电压，最大电源电压高达 55V。此外，这些器件具有通过 nSLEEP 引脚启用的低功耗睡眠模式，并且集成的电荷泵来支持 100%的占空比输出。

DR702Q 和 DR703Q 提供保护功能和栅极驱动可配置性的组合，以提高设计的简单性并将电机系统的智能化程度提升到一个新的水平。栅极驱动能力或栅极驱动电流可以通过驱动器本身进行调整，这样可以方便针对不同的 FET 和应用进行选择和优化，省去了外部电阻器等元件。驱动峰值电流可通过 IDRIVE 引脚(DR702Q)或 SPI (DR703Q)进行多个挡位调整。当 VM 电压超过 13.5V 时，高侧和低侧 FET 均由 10.2V(标称值)的栅极源极电压(VGS)驱动。在较低的 VM 电压下，VGS 会降低。高侧栅极驱动电压是使用调节至 VM + 10.2V 的双倍架构电荷泵生成的。

为了限制启动浪涌电流和堵转电流，器件内置了固定时间关断电流斩波方案。通过设置 VREF 引脚上的电压，通过检测电阻器设置斩波电流电平。有关更多信息，请参见 CURRENT REGULATION 部分。DR702Q/703Q 中还集成有电流采样放大器，可为系统控制器提供准确的电流测量。DR702Q 固定增益为 20 而 DR703Q 支持 10/19.8/39.4/78 四档增益。

DR702Q/703Q 还具有超越传统分立实现的保护功能，包括欠压锁定(UVLO)、过流保护(OCP)、栅极驱动器故障和热关断(TSD)等。

DR702Q/703Q 还为内部数字振荡器和内部电荷泵集成了扩频时钟功能以应对系统 EMC 挑战。

7.2 功能模块框图

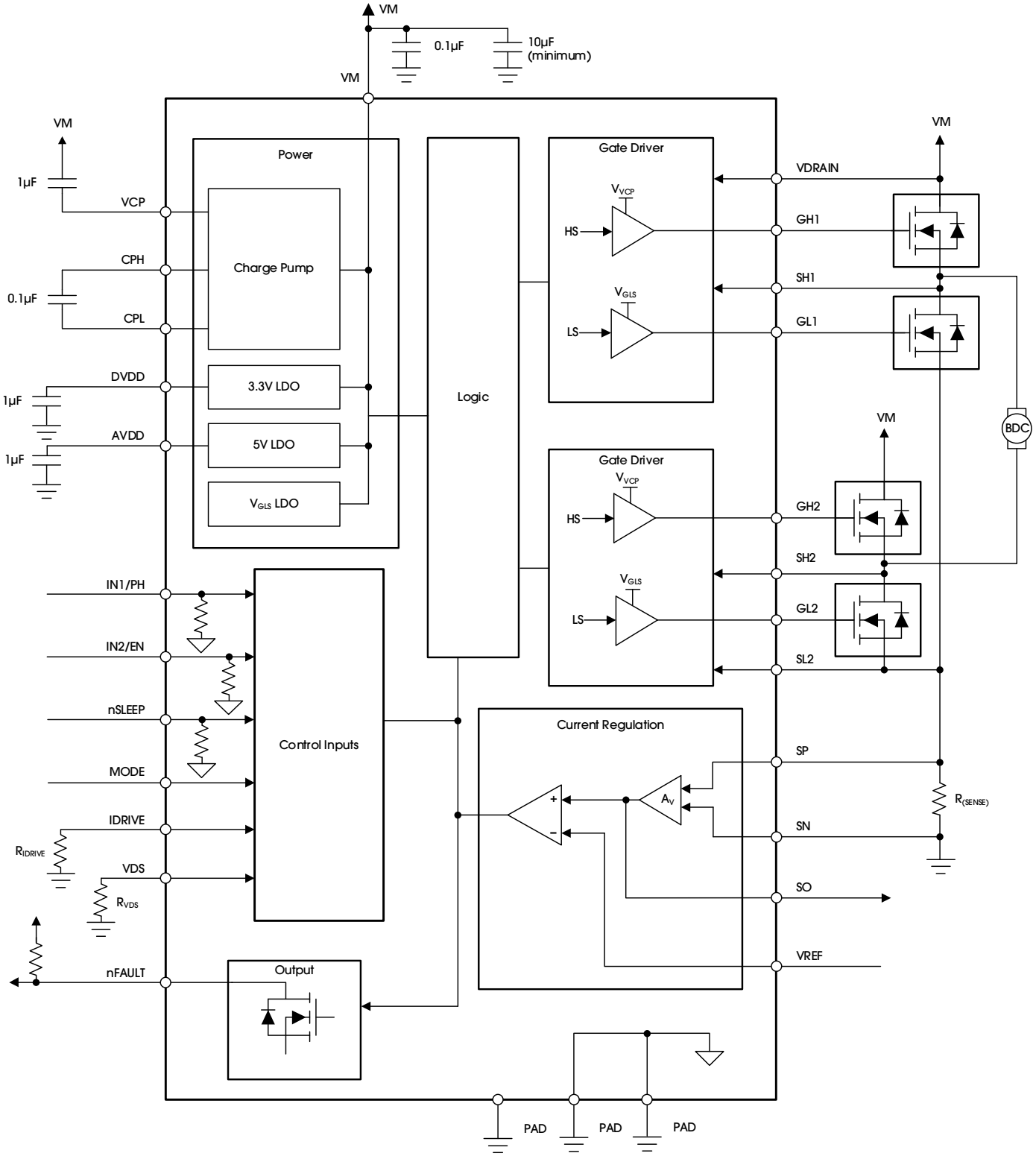


Figure 21. DR702Q Functional Block Diagram

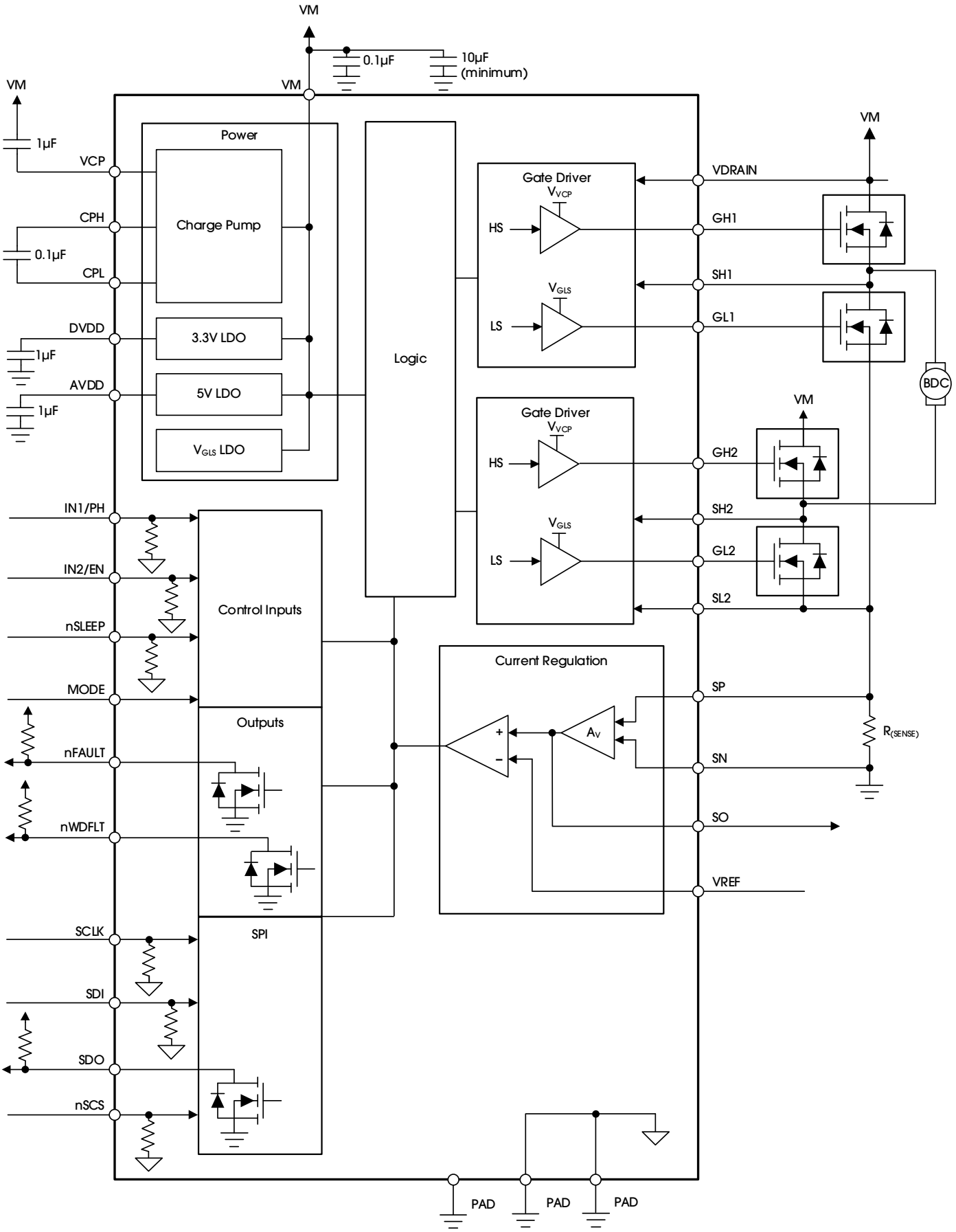


Figure 22. DR703Q Functional Block Diagram

7.3 特性说明

Table 11 和 Table 12 为推荐外部器件。

Table 11. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
$C_{(VM1)}$	VM	GND	0.1µF ceramic capacitor rated for VM
$C_{(VM2)}$	VM	GND	≥ 10µF electrolytic capacitor rated for VM
$C_{(VCP)}$	VCP	VM	16V, 1µF ceramic capacitor
$C_{(SW)}$	CPH	CPL	0.1µF X7R capacitor rated for VM
$C_{(DVDD)}$	DVDD	GND	6.3V, 1µF ceramic capacitor
$C_{(AVDD)}$	AVDD	GND	6.3V, 1µF ceramic capacitor
$R_{(IDRIVE)}$	IDRIVE	GND	For resistor sizing, see the TYPICAL APPLICATION section.
$R_{(VDS)}$	VDS	GND	For resistor sizing, see the TYPICAL APPLICATION section.
$R_{(nFAULT)}$	V_{CC}(1)	nFAULT	≥ 10kΩ
$R_{(nWDFLT)}$	V_{CC}(1)	nWDFLT	≥ 10kΩ
$R_{(SENSE)}$	SP	SN or GND	Optional low-side sense resistor
$R_{(VDRAIN)}$(2)	VDRAIN	VM	100Ω series resistor

注 1：V_{CC} 引脚不是 DR702Q/703Q 上的引脚，但开漏输出 nFAULT 需要 V_{CC} 电源电压上拉。这些引脚可以上拉至 AVDD 或 DVDD。

注 2：如果没有在 VDRAIN 引脚上实施外部电池反接保护，则应在 VDRAIN 和 VM 引脚之间使用 $R_{(VDRAIN)}$电阻，以最大限度地减少流向 VDRAIN 引脚的电流。

Table 12. External Gates

COMPONENT	GATE	DRAIN	SOURCE	RECOMMENDED
$Q_{(HS1)}$	GH1	VM	SH1	Supports FETs up to 200nC at 40kHz PWM For more information, see the APPLICATION AND IMPLEMENTATION section.
$Q_{(LS1)}$	GL1	SH1	SP or GND	
$Q_{(HS2)}$	GH2	VM	SH2	
$Q_{(LS2)}$	GL2	SH2	SP or GND	

7.3.1 H 桥控制

DR702Q/703Q 使用可配置的输入接口进行控制。LOGIC TABLES 部分提供了完整的 H 桥状态。该表未考虑 DR702Q/703Q 中内置的电流控制。正电流定义为 SH1 到 SH2 的方向。MODE 引脚设置的逻辑操作在上电或退出睡眠模式时被锁存。

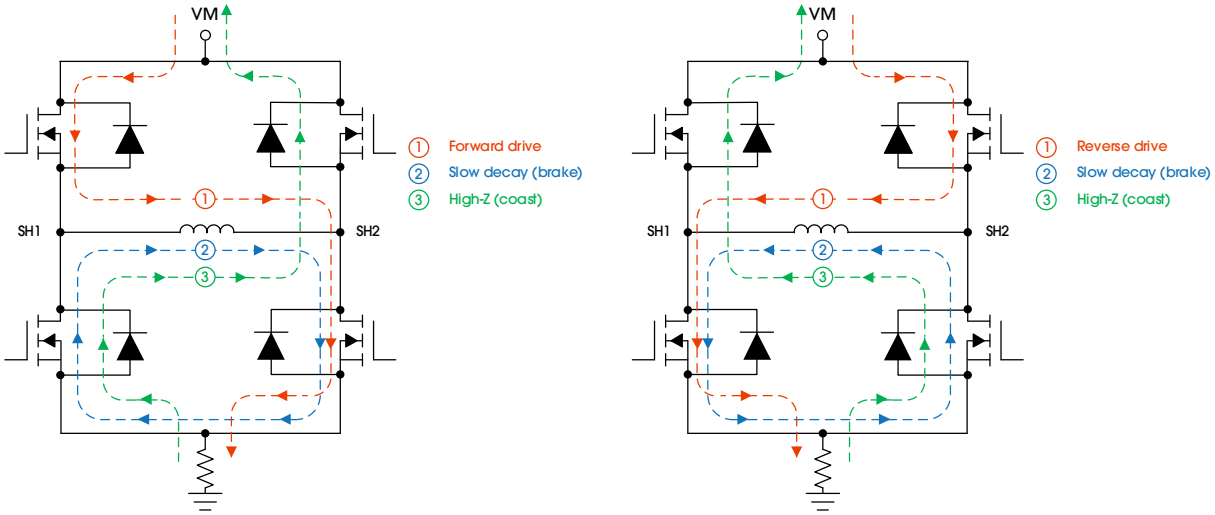


Figure 23. Bridge Control

7.3.1.1 LOGIC TABLES

Table 13、Table 14 和 Table 15 为芯片逻辑表，其中 *X* 代表无关输入或者输出。

Table 13. DR702Q/703Q PH and EN Control Interface (MODE = 0)

nSLEEP	IN1/PH	IN2/EN	GH1	GL1	SH1	GH2	GL2	SH2	AVDD/DVDD	DESCRIPTION
0	X	X	X	X	Hi-Z	X	X	Hi-Z	Disabled	Sleep mode H-bridge disabled Hi-Z
1	X	0	0	1	L	0	1	L	Enabled	Brake low-side slow decay
1	0	1	0	1	L	1	0	H	Enabled	Reverse (current SH2 to SH1)
1	1	1	1	0	H	0	1	L	Enabled	Forward (current SH1 to SH2)

Table 14. DR702Q/703Q Independent PWM Control Interface (MODE = 1)

nSLEEP	IN1/PH	IN2/EN	GH1	GL1	SH1	GH2	GL2	SH2	AVDD/DVDD	DESCRIPTION
0	X	X	X	X	Hi-Z	X	X	Hi-Z	Disabled	Sleep mode H-bridge disabled Hi-Z
1	X	0	X	X	X	0	1	L	Enabled	Half-bridge 2 low side on
1	X	1	X	X	X	1	0	H	Enabled	Half-bridge 2 high side on
1	0	X	0	1	L	X	X	X	Enabled	Half-bridge 1 low side on
1	1	X	1	0	H	X	X	X	Enabled	Half-bridge 1 high side on

Table 15. DR702Q/703Q Standard PWM Control Interface (MODE = Hi-Z)

nSLEEP	IN1/PH	IN2/EN	GH1	GL1	SH1	GH2	GL2	SH2	AVDD/DVDD	DESCRIPTION
0	X	X	X	X	Hi-Z	X	X	Hi-Z	Disabled	Sleep mode H-bridge disabled Hi-Z
1	0	0	0	0	Hi-Z	0	0	Hi-Z	Enabled	Coast H-bridge disabled Hi-Z
1	0	1	0	1	L	1	0	H	Enabled	Reverse (current SH2 to SH1)
1	1	0	1	0	H	0	1	L	Enabled	Forward (current SH1 to SH2)
1	1	1	0	1	L	0	1	L	Enabled	Brake low-side slow decay

7.3.2 模式引脚

器件的 MODE 引脚决定控制接口并在上电或退出睡眠模式时锁存。Figure 24 显示了 MODE 引脚的内部电路概览。

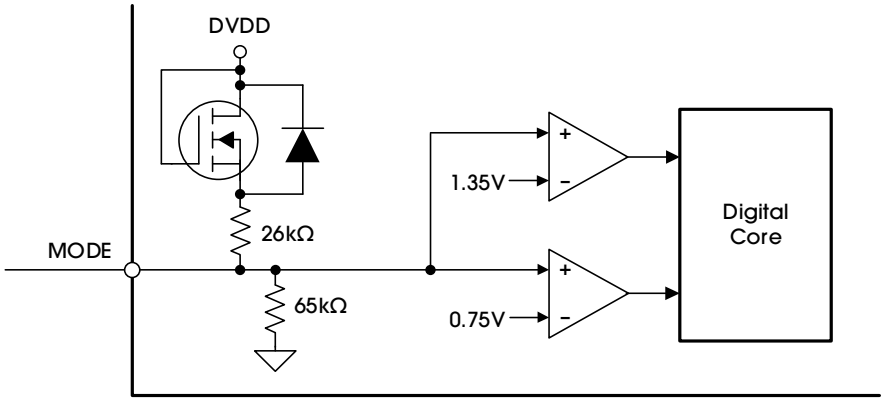


Figure 24. MODE Pin Block Diagram

Table 16 列出了可在上电或退出睡眠模式时通过 MODE 引脚设置的不同控制接口。

Table 16. MODE Pin Configuration

MODE	CONTROL INTERFACE
0	PH or EN
1	Independent half-bridge
Hi-Z	PWM

在器件上电期间，首先启用 DVDD 引脚。然后 MODE 引脚锁存。最后启用 AVDD 引脚。设置 PWM 控制接口时，不建议将 MODE 引脚连接到 AVDD 引脚。如果不是由外部微控制器(MCU)驱动，MODE 引脚应连接到外部 5V 或 3.3V 电源或 DVDD 引脚。

7.3.3 nFAULT 引脚

nFAULT 引脚为漏极开路输出，应上拉至 5V 或 3.3V 电源。当检测到故障时，nFAULT 为逻辑低电平。对于 3.3V 上拉，nFAULT 引脚可以通过电阻器连接到 DVDD 引脚。对于 5V 上拉，应使用外部 5V 电源。不建议将 nFAULT 引脚连接到 AVDD 引脚。

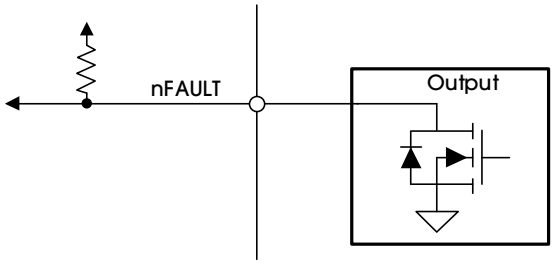


Figure 25. nFAULT Block Diagram

7.3.4 电流调节

通过电机绕组的最大电流可由固定关断时间 PWM 通过电流斩波进行调节。当 H 桥在正向或反向驱动中启用时，电流通过绕组上升的速率取决于绕组的直流电压和电感。当电流达到电流斩波阈值时，电桥进入制动(低侧 slow decay)模式，直到 t_{off} 时间到期。

需要注意的是，电流启用后，SP 引脚上的电压立即被忽略一段时间($t_{(BLANK)}$)，然后启用电流检测电路。

PWM 斩波电流由比较器设置，该比较器将连接到 SP 引脚的电流检测电阻器两端的电压乘以 A_V 因子与来自 VREF 引脚的参考电压进行比较。系数 A_V 是电流检测放大器增益，对于 DR702Q 器件为 19.8V/V，对于 DR703Q 器件可配置为 10、19.8、39.4 或 78V/V。请使用 Equation 1 计算斩波电流(I_{CHOP})。

$$I_{(CHOP)} = \frac{V_{REF} - V_{IO} \times A_V}{A_V \times R_{SENSE}} \quad (1)$$

例如，如果选择 50mΩ 检测电阻和 3.3V 的 VREF 值，则满量程斩波电流为 3.28A。在本例中，A_V 为 19.8V/V，V_{IO} 假定为 3.7mV。

对于直流电机，电流调节用于限制电机的启动和停止电流。如果不需要电流调节功能，可以通过将 VREF 引脚直接连接到 AVDD 引脚来禁用它。如果选择独立 PWM 控制接口模式(MODE 引脚为 1)进行操作，则该器件不执行 PWM 电流调节或电流斩波。

7.3.5 放大器输出(SO)

DR702Q/703Q 器件上的 SO 引脚输出的模拟电压等于 SP 和 SN 引脚上的电压乘以 A_V。SO 电压仅对正向或反向驱动有效。使用 Equation 2 计算 H 桥的近似电流。

$$I = \frac{V_{SO} - V_{IO} \times A_V}{A_V \times R_{SENSE}} \quad (2)$$

当 SP 和 SN 电压为 0V 时，SO 引脚输出放大器失调电压乘以放大器增益 $V_{IO} \times A_V$。当 SP 减去 SN 大于 0V 时，SO 引脚输出放大器失调电压与检测电阻或电压之和，乘以放大器增益，$(V_{IO} + V_{RSENSE}) \times A_V$。SO 引脚上不需要电容器。

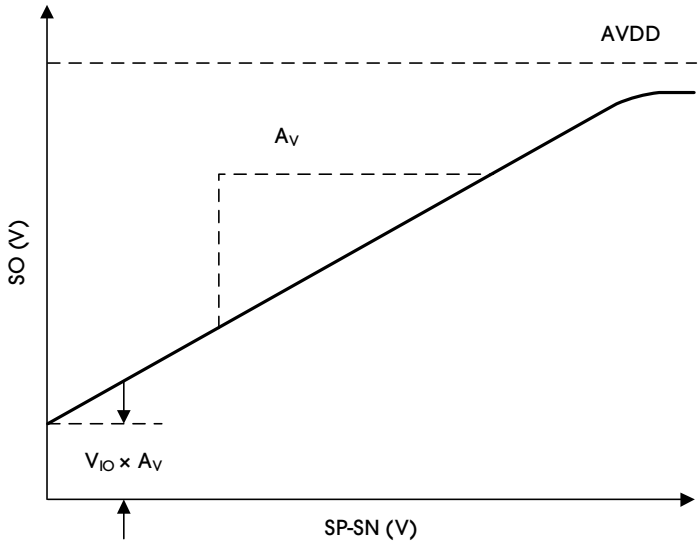


Figure 26. Current Sense Amplifier Output

如果 SP 和 SN 引脚上的电压超过 1V，则 DR702Q/703Q 会触发过流保护。

如果 SO 引脚接地短路，或者如果该引脚驱动高的电流负载，则 SO 输出将用作恒流源。输出电压不代表该状态下的 H 桥电流。

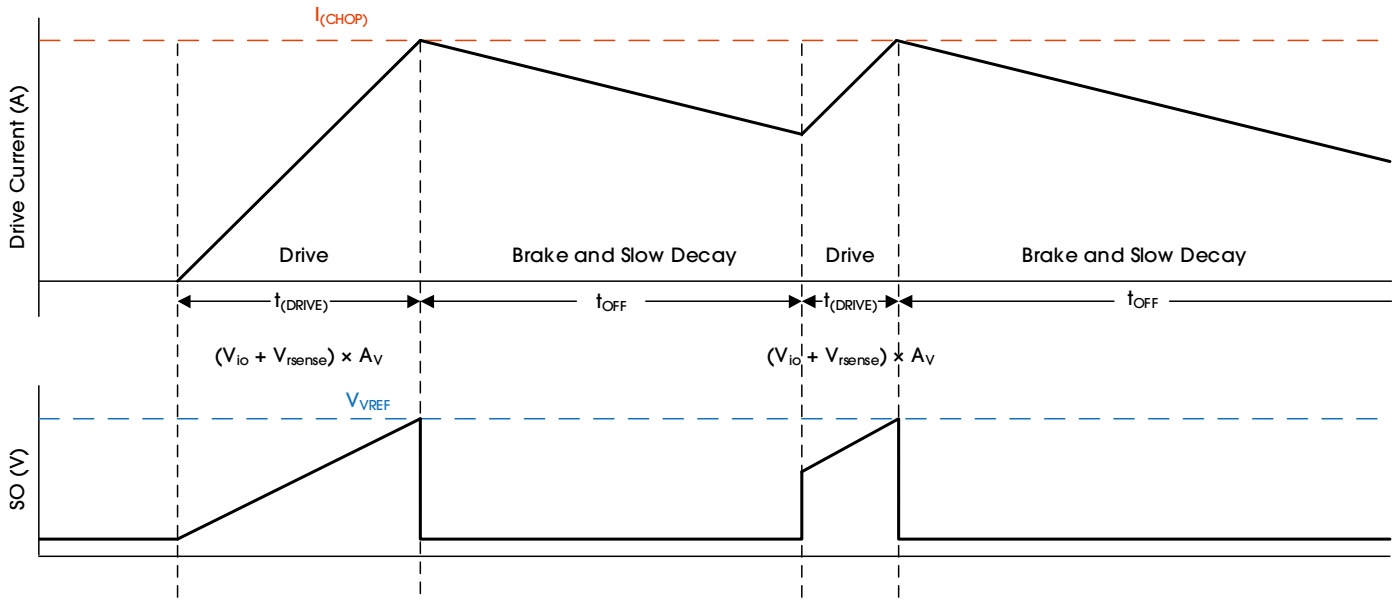


Figure 27. Current Sense Amplifier and Current Chopping Operation

在制动模式(slow decay)期间，电流通过低侧 FET 循环。因为电流没有流过检测电阻，所以 SO 引脚不代表电机电流。

7.3.5.1 SO 采样保持

DR703Q 支持电流采样放大器采样保持功能。要启用此模式，请通过 SPI 将 SH_EN 位设置为高电平。在这种模式下，只要驱动器处于制动模式，分流放大器输出就会被禁用为 Hi-Z 状态。建议在此引脚上放置一个外部电容。

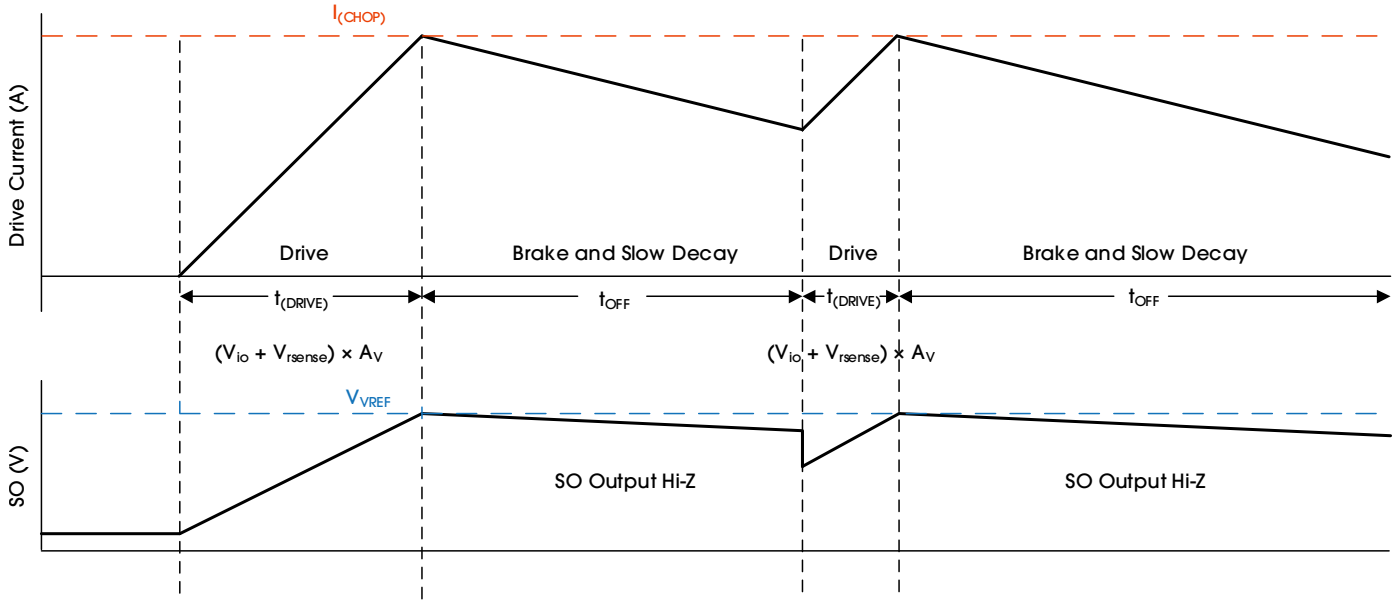


Figure 28. Sample and Hold Operation

7.3.6 PWM 电机栅极驱动器

Figure 29 显示了 DR702Q/703Q 预驱动电路的框图。

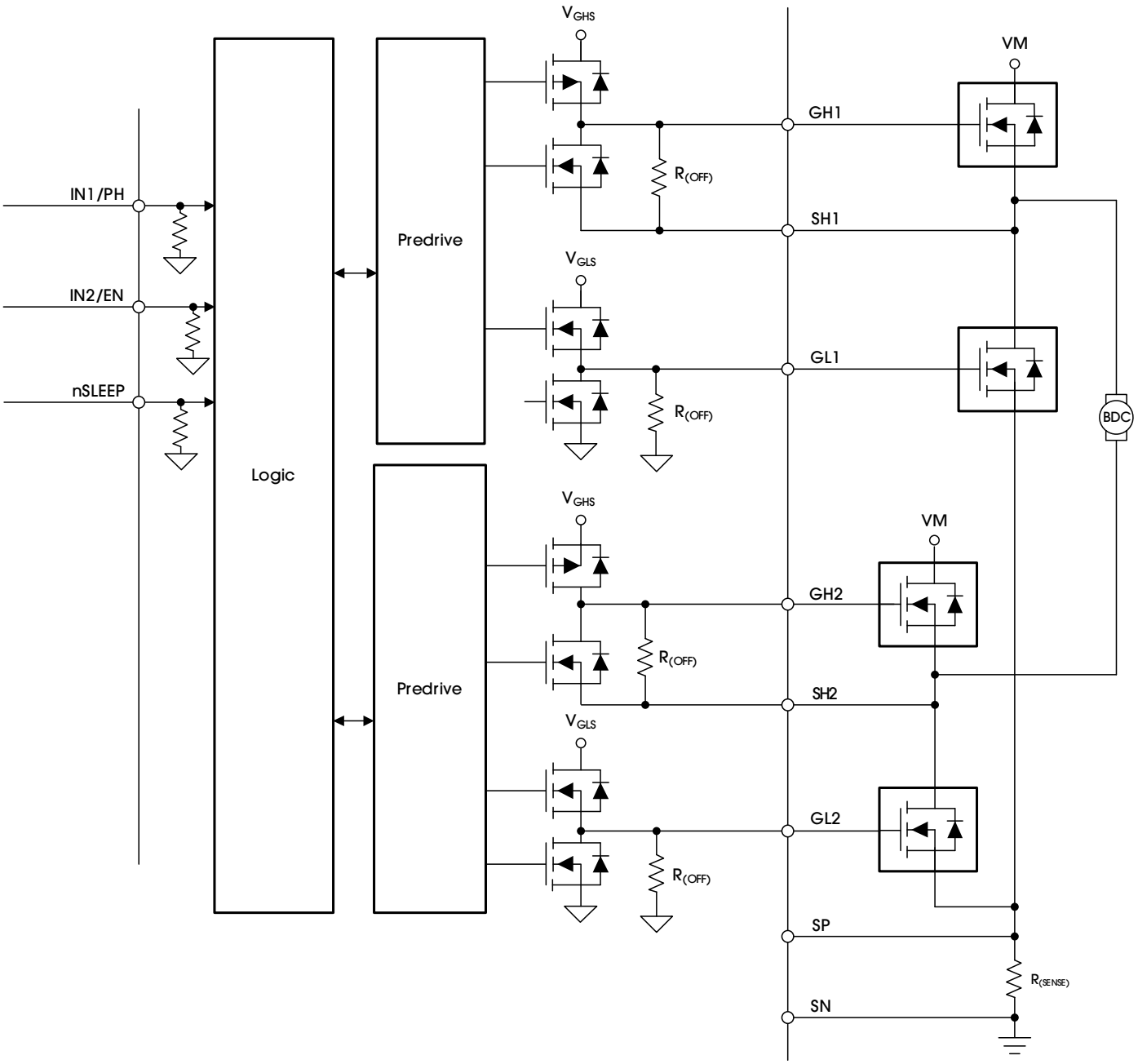


Figure 29. Predrive Block Diagram

DR702Q/703Q 内部的栅极驱动器直接驱动驱动电机电流的 N 沟道 MOSFET。高侧栅极驱动由电荷泵提供，而内部稳压器产生低侧栅极驱动。

栅极驱动器的峰值驱动电流可通过 DR702Q 器件的 IDRIVE 引脚或 DR703Q 器件的 IDRIVE 寄存器进行调节。详情请参考 ELECTRICAL CHARACTERISTICS 表中列出的值。峰值灌电流大约是峰值拉电流的两倍。调整峰值电流会改变输出转换率，这也取决于 FET 输入电容和栅极电荷。

快速切换会在 VM 和 GND 引脚上产生额外的噪声。当体二极管瞬时反向偏置时，这种额外的噪声可能是因为低侧体二极管的反向恢复时间相对较慢，类似于直通。开关时间慢则会导致功耗过大，因为外部 FET 的开启和关闭时间较长。

当改变输出状态时，峰值电流(I_{DRIVE})会在(t_{DRIVE})时间内施加，以对栅极电容充电。在此时间之后，使用弱电流源(I_{HOLD})将栅极保持在所需状态。为给定的外部 FET 选择栅极驱动强度时，所选电流必须足够高，以便在 $t_{(DRIVE)}$期间对栅极进行完全充电和放电，否则 FET 中会耗散过多的功率。

在高侧导通期间，低侧栅极通过强下拉(I_{STRONG})被拉低。此下拉可防止低侧 FET Q_{GS} 充电并使 FET 保持关闭状态，即使在输出端发生快速切换时也是如此。

栅极驱动器电路包括在模拟电路中强制执行死区时间，以防止高侧和低侧 FET 同时导通。当开关 FET 导通时，这种握手可防止高侧或低侧 FET 导通，直到相反的 FET 关闭。

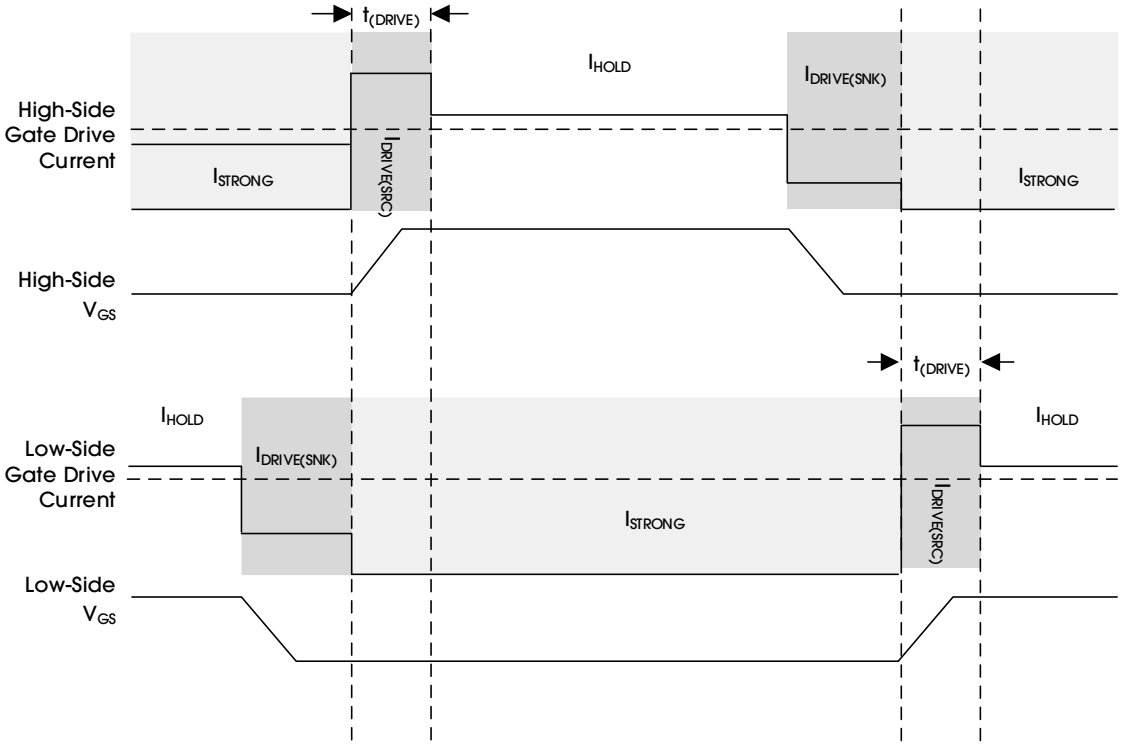


Figure 30. Gate Driver Output to Control External FETs

7.3.6.1 米勒电荷(Q_{GD})

当 FET 栅极导通时，必须对以下电容充电：

- 门源电荷，Q_{GS}
- 栅漏电荷，Q_{GD} (米勒电荷)
- 剩余 Q_G

FET 输出主要在 Q_{GD} 充电期间转换。

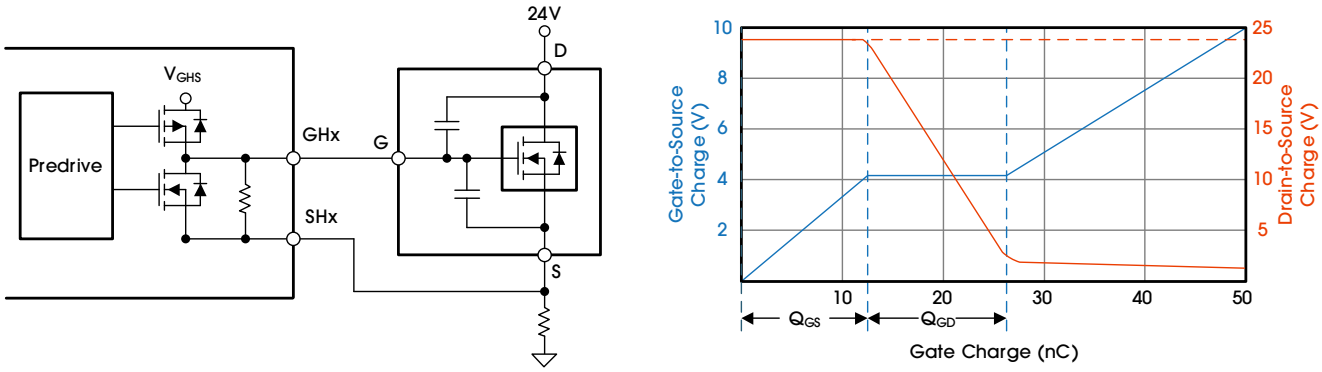


Figure 31. FET Gate Charging Profile

7.3.7 IDRIVE 引脚(仅限 DR702Q)

H 桥输出(SHx 引脚)的上升和下降时间可以通过设置 IDRIVE 电阻值或在 IDRIVE 引脚上施加电压来调整。如果选择了更高的 IDRIVE 设置，FET 栅极电压上升得更快。FET 栅极的斜坡直接影响 H 桥输出的上升和下降时间。

将 IDRIVE 引脚接地可选择 10mA 拉电流和 20mA 灌电流的最低驱动设置。保持此引脚开路选择 155mA 高压侧和 130mA 低压侧的源电流驱动设置，以及 265mA 高压侧和 260mA 低压侧灌电流，VM 电压为 13.5V。有关 IDRIVE 配置的详细列表，请参见 Table 17。

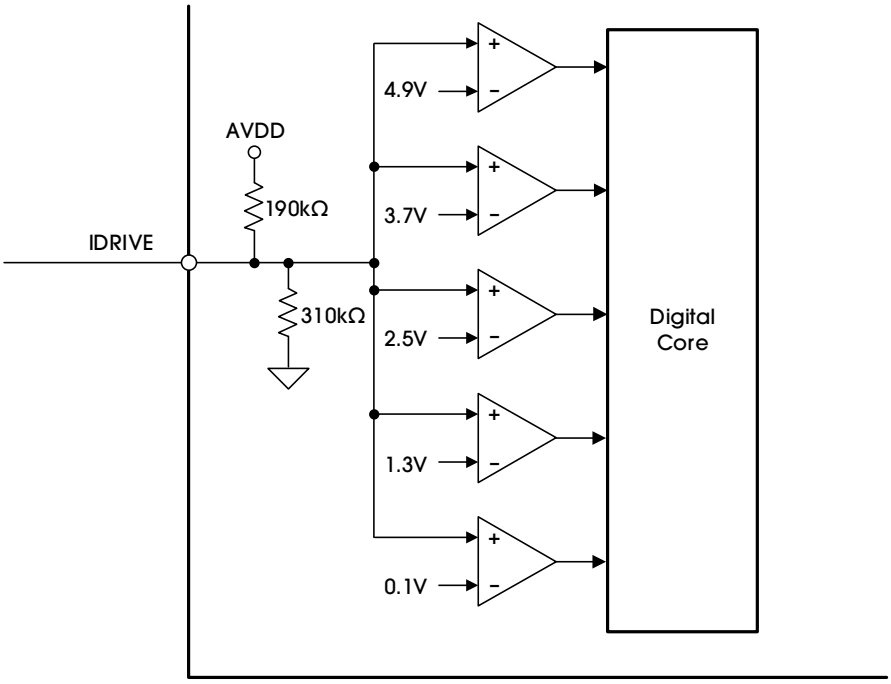
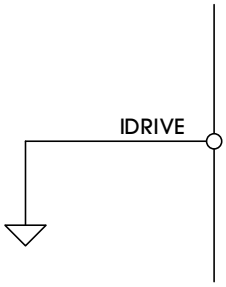
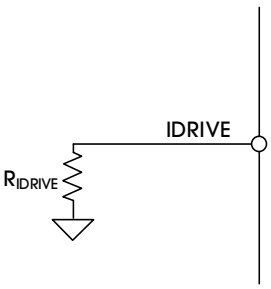
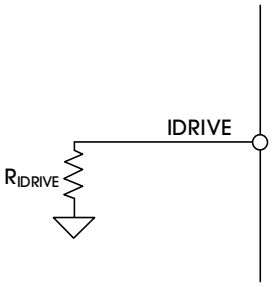
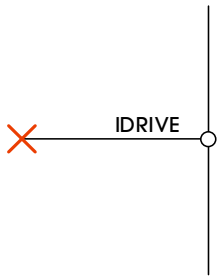
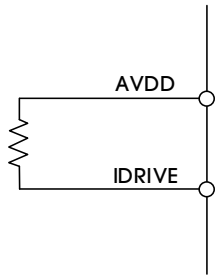
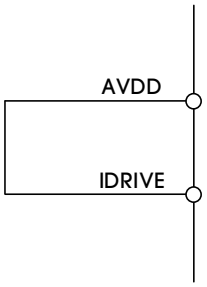


Figure 32. IDRIVE Pin Internal Circuitry

Table 17. DR702Q IDRIVE Settings

IDRIVE RESISTANCE	IDRIVE VOLTAGE	SOURCE CURRENT		SINK CURRENT		CIRCUIT
		V_{VM} = 5.5V	V_{VM} = 13.5V	V_{VM} = 5.5V	V_{VM} = 13.5V	
< 1kΩ to GND	GND	High-side: 6mA Low-side: 8mA	High-side: 10mA Low-side: 10mA	High-side: 14mA Low-side: 17mA	High-side: 20mA Low-side: 20mA	
33kΩ ± 5% to GND	0.7V ± 5%	High-side: 12mA Low-side: 16mA	High-side: 20mA Low-side: 20mA	High-side: 28mA Low-side: 35mA	High-side: 40mA Low-side: 40mA	

IDRIVE RESISTANCE	IDRIVE VOLTAGE	SOURCE CURRENT		SINK CURRENT		CIRCUIT
		V_{VM} = 5.5V	V_{VM} = 13.5V	V_{VM} = 5.5V	V_{VM} = 13.5V	
200kΩ ± 5% to GND	2V ± 5%	High-side: 30mA Low-side: 39mA	High-side: 48mA Low-side: 50mA	High-side: 72mA Low-side: 75mA	High-side: 100mA Low-side: 87mA	
> 2MΩ to GND, Hi-Z	3V ± 5%	High-side: 100mA Low-side: 100mA	High-side: 152mA Low-side: 120mA	High-side: 180mA Low-side: 204mA	High-side: 253mA Low-side: 240mA	
68kΩ ± 5% to AVDD	4V ± 5%	High-side: 130mA Low-side: 139mA	High-side: 199mA Low-side: 170mA	High-side: 250mA Low-side: 280mA	High-side: 354mA Low-side: 325mA	
< 1kΩ to AVDD	AVDD	High-side: 160mA Low-side: 178mA	High-side: 245mA Low-side: 220mA	High-side: 320mA Low-side: 360mA	High-side: 454mA Low-side: 422mA	

7.3.8 死区时间

死区时间由插入的数字死区时间和 FET 栅极转换组成。DR702Q 器件的数字死区时间约为 240ns。DR703Q 器件具有 120ns、240ns、480ns 和 960ns 的可编程死区时间选项。除了这个数字死区时间，只要 GLx 引脚到地或 GHx 引脚到 SHx 引脚的电压小于 FET 阈值电压，输出就是 Hi-Z。

总死区时间取决于 IDRIVE 电阻设置，因为 FET 栅极斜坡(GHx 和 GLx 引脚)的一部分包括可观察到的死区时间。

7.3.9 传播延迟

传播延迟时间(t_{PD})测量为输入边沿与输出变化之间的时间。该时间由两部分组成：输入去毛刺脉冲发生器和输出转换延迟。输入去毛刺抑制器可防止输入引脚上的噪声影响输出状态。

栅极驱动转换速率也会影响延迟时间。为了在正常操作期间改变输出状态，必须首先关闭一个 FET。FET 栅极根据 IDRIVE 电阻器选择斜坡下降，当 FET 栅极降至阈值电压以下时，观察到的传播延迟结束。

7.3.10 过流 VDS 监控器

栅极驱动电路在驱动电流时监控每个外部 FET 的 VDS 电压。当 OCP 抗尖峰脉冲时间结束后监测到的电压大于 OCP 阈值电压($V_{DS(OCP)}$)时，将检测到 OCP 条件。可以通过改变 DR702Q 器件 VDS 引脚上的电阻器(R_{VDS})来调整 $V_{DS(OCP)}$电压。DR703Q 器件通过设置 VDS 寄存器提供 $V_{DS(OCP)}$电压电平。

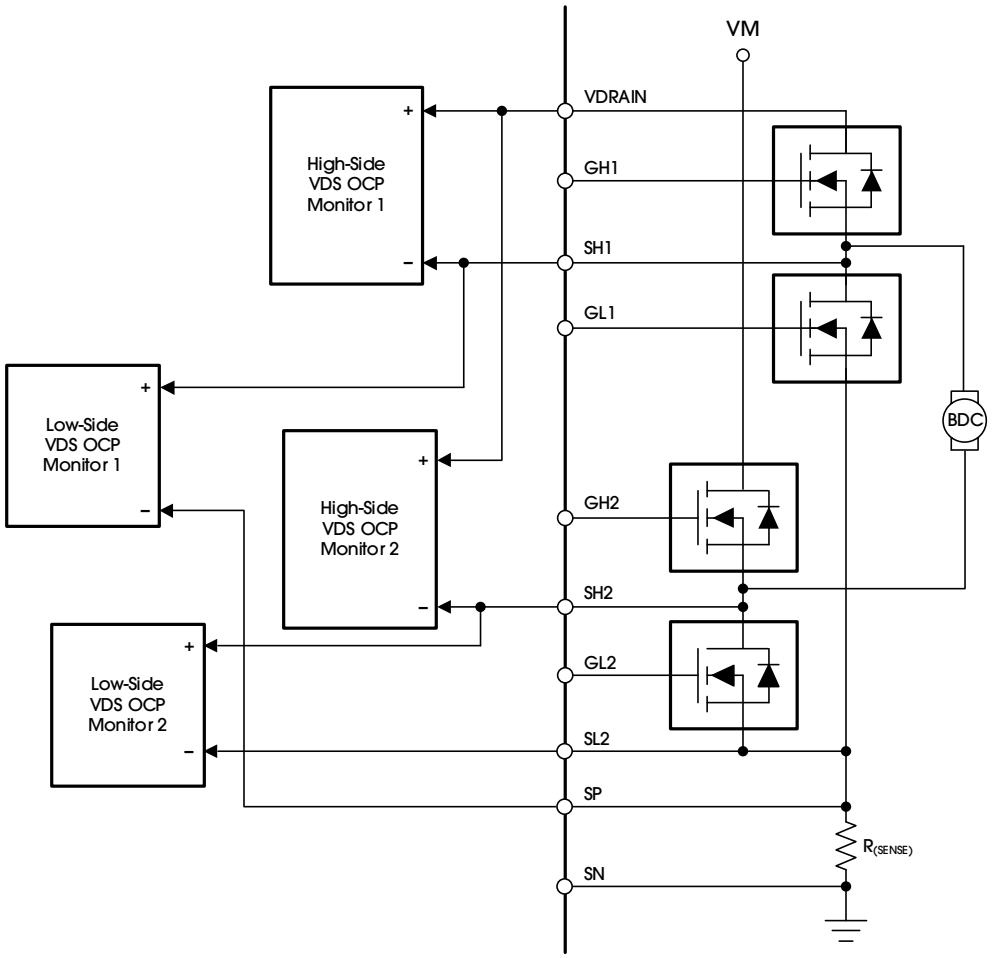


Figure 33. $V_{DS(OCP)}$ Block Diagram

高侧 FET 上的 VDS 电压通过 VDRAIN 至 SHx 引脚测量。半桥 1 上的低侧 VDS 监视器测量 SH1 到 SP 引脚的 VDS 电压。半桥 2 上的低侧 VDS 监视器测量 SH2 至 SL2 引脚上的 VDS 电压。即使未使用采样放大器，也请确保 SP 引脚始终连接到半桥 1 的低侧 FET 的源极。

7.3.11 VDS 引脚（仅限 DR702Q）

DR702Q 器件上的 VDS 引脚用于选择过流检测的 VDS 阈值电压。

将 VDS 引脚接地可选择 0.06V 的最低设置。保持此引脚开路可选择 0.48V 的设置。将 VDS 引脚连接到 AVDD 引脚可禁用 VDS 监视器。有关 VDS 配置的详细列表，请参见 Table 18。

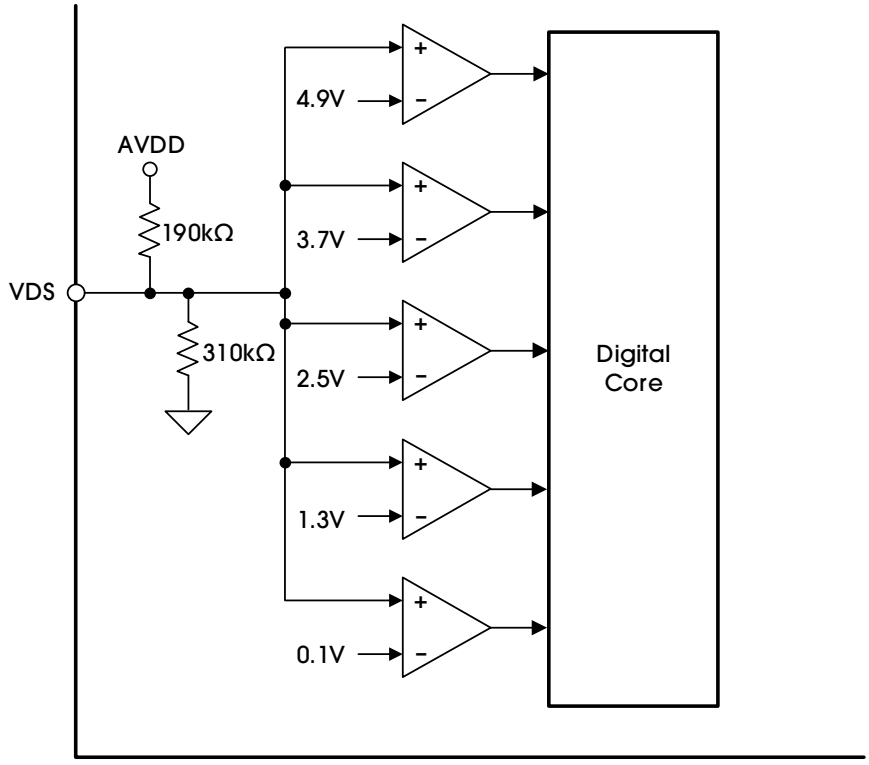
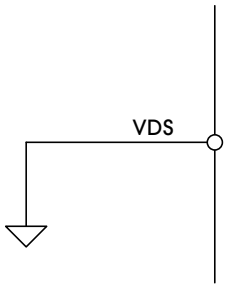
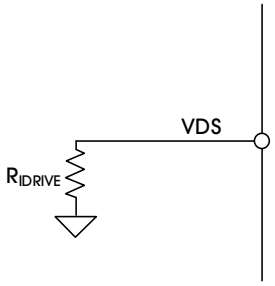
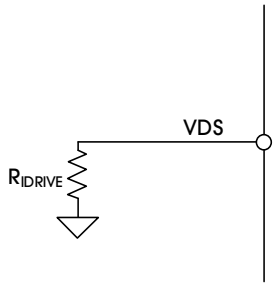
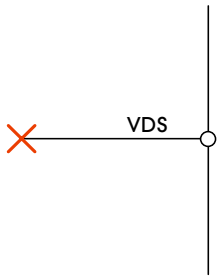
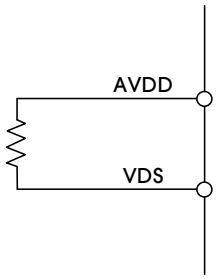
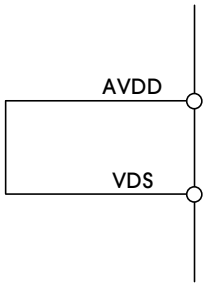


Figure 34. VDS Block Diagram

Table 18. VDS Pin Resistor Setting

VDS RESISTANCE	VDS VOLTAGE	OVERCURRENT TRIP LEVEL ($V_{DS(OCP)}$)	CIRCUIT
< 1kΩ to GND	GND	0.06V	
33kΩ ± 5% to GND	0.7V ± 5%	0.12V	

VDS RESISTANCE	VDS VOLTAGE	OVERCURRENT TRIP LEVEL ($V_{DS(OCP)}$)	CIRCUIT
200kΩ ± 5% to GND	2V ± 5%	0.24V	
> 2MΩ to GND, Hi-Z	3V ± 5%	0.48V	
68kΩ ± 5% to AVDD	4V ± 5%	0.96V	
< 1kΩ to AVDD	AVDD	Disabled	

7.3.12 电荷泵

集成电荷泵以提供高侧 NMOS (V_{GSH})的栅极驱动电压。电荷泵需要在 VM 和 VCP 引脚之间连接一个电容器。此外，在 CPH 和 CPL 引脚之间需要一个低 ESR 陶瓷电容器。当 VM 电压低于 13.5V 时，此电荷泵用作倍增器，并在空载时产生等于 2 × V_{VM} – 1.5V 的 V_{VCP}。当 VM 电压超过 13.5V 时，电荷泵调节 V_{VCP} 使其等于 V_{VM} + 10.2V。

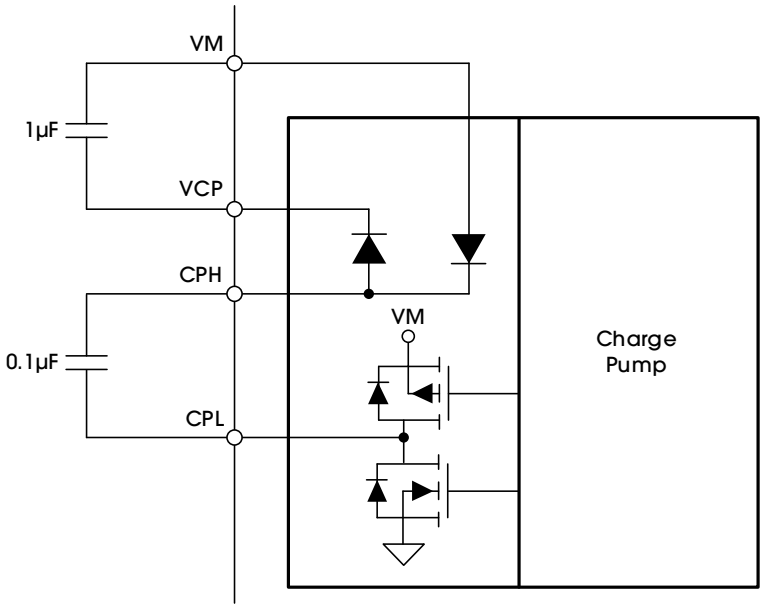


Figure 35. Charge Pump Block Diagram

7.3.13 栅极驱动钳位

钳位电路将栅极驱动输出电压限制为 $V_{C(GS)}$电压，以保护功率 FET 免受损坏。正电压钳位是使用一系列二极管实现的。负电压钳位使用内部预驱动器 FET 的体二极管。

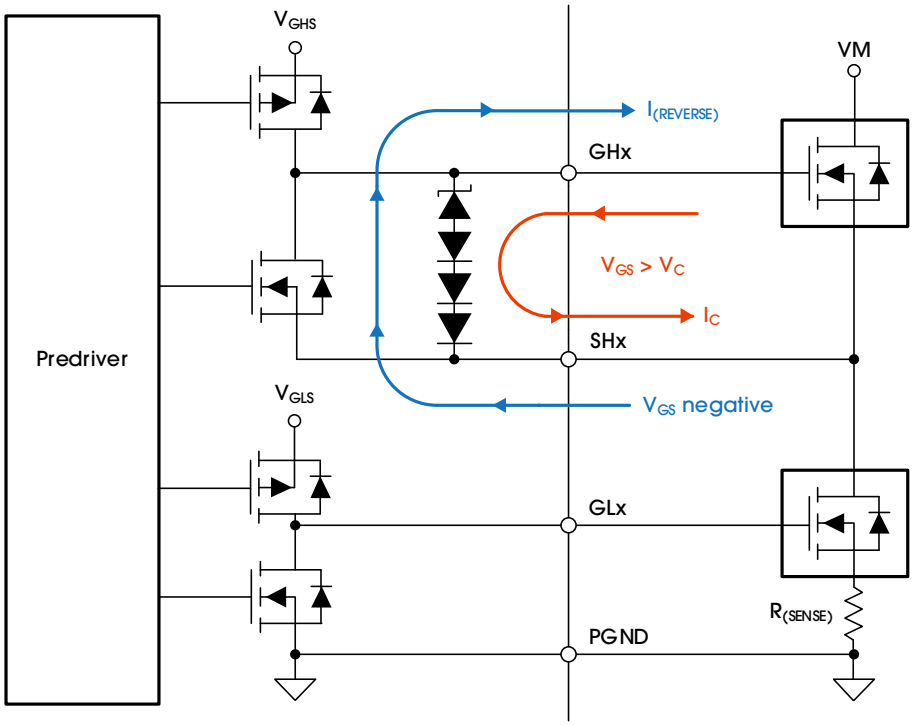


Figure 36. Gate Drive Clamp

7.3.14 保护电路

DR702Q/703Q 器件可防止 VM 欠压、电荷泵欠压、过流、栅极驱动器短路和过热事件。

7.3.14.1 VM 欠压闭锁(UVLO2)

如果 VM 引脚上的电压低于 VM 欠压锁定阈值电压(V_{UVLO2})，H 桥中的所有 FET 将被禁用，电荷泵将被禁用，nFAULT 引脚将被驱动为低电平，DR703Q 器件的 VM_UVFL 位被置位。当 VM 电压升至 UVLO2 阈值以上时，操作恢复。nFAULT 引脚在操作恢复后释放，但 DR703Q 设备上的 VM_UVFL 位保持设置状态，直到通过写入 CLR_FLT 位来清除。

即使输出驱动器被禁用，DR703Q 设备上的 SPI 设置也不会因此故障而复位。在 VM 电压低于逻辑欠压阈值(V_{UVLO1})之前，设置将保持不变且内部逻辑保持活动状态。DR703Q 第一次上电，寄存器 0x00 的第 2 位会提示 VM 欠压故障，建议第一次上电后清除故障。

7.3.14.2 逻辑欠压(UVLO1)

如果 VM 引脚上的电压低于逻辑欠压阈值电压(V_{UVLO1})，则内部逻辑将复位。当 VM 电压上升到 UVLO1 阈值以上时，操作恢复。nFAULT 引脚在此状态期间为逻辑低电平，因为当发生 VM 欠压情况时它被拉低。将 VM 电压降低到该欠压阈值以下会重置 SPI 设置。

7.3.14.3 VCP 欠压闭锁(CPUV)

如果 VCP 引脚上的电压低于电荷泵欠压(CPUV)锁定的阈值电压，H 桥中的所有 FET 将被禁用并且 nFAULT 引脚被驱动为低电平。DR703Q 器件上的 VCP_UVFL 位被置位。当 VCP 电压上升到 CPUV 阈值以上时，操作恢复。nFAULT 引脚在操作恢复后释放，但 DR703Q 器件上的 VCP_UVFL 位保持设置状态，直到通过写入 CLR_FLT 位来清除。DR703Q 第一次上电，寄存器 0x00 的第 3 位会提示 VCP 欠压故障，建议第一次上电后清除故障。

7.3.14.4 过流保护(OCP)

通过监视外部 FET 上的 VDS 压降来检测过流。如果驱动 FET 两端的电压超过 $V_{DS(OCP)}$电平的时间长于 OCP 抗尖峰脉冲时间，则识别为 OCP 事件，然后 H 桥中的所有 FET 都被禁用，nFAULT 引脚被驱动为低电平。DR703Q 器件的 OCP 位被置位。驱动器在 $t_{(RETRY)}$时间过后重新启用。nFAULT 引脚在重试时间后再次变为高电平。

如果故障条件仍然存在，则循环重复。如果故障不再存在，则恢复正常操作并且 nFAULT 引脚变为高电平。DR703Q 上的 OCP 位保持设置状态，直到通过写入 CLR_FLT 位来清除。除了此 FET VDS 监视器之外，如果 SP 引脚上的电压超过 $V_{SP(OCP)}$ 并且 nFAULT 引脚被驱动为低电平，则会检测到过流情况。DR703Q 器件中的 OCP 位已设置。

7.3.14.5 栅极驱动器故障(GDF)

GHx 和 GLx 引脚受到监控，如果外部 FET 栅极上的电压在 $t_{(DRIVE)}$时间后没有升高或降低，则检测到栅极驱动器故障。例如 GHx 或 GLx 引脚与 GND、SHx 或 VM 引脚短路，则会发生此故障。此外，如果所选的 IDRIVE 设置不足以开启外部 FET，则会发生栅极驱动器故障。H 桥中的所有 FET 都被禁用，nFAULT 引脚被驱动为低电平。DR703Q 器件的 GDF 位会被置位。在 OCP 重试周期($t_{(RETRY)}$)过后，驱动程序重新启用。nFAULT 引脚在操作恢复后释放，但 DR703Q 器件上的 GDF 位保持设置状态，直到通过写入 CLR_FLT 位来清除。

7.3.14.6 热关断(TSD)

如果芯片内部温度超过 T_{SD} 温度，则 H 桥中的所有 FET 都被禁用，电荷泵关闭，AVDD 稳压器被禁用，nFAULT 引脚被驱动为低电平。DR703Q 器件的 OTSD 位也被置位。在管芯温度低于 $T_{SD} – T_{hys}$ 温度后，器件会自动恢复运行。nFAULT 引脚在操作恢复后释放，但 DR703Q 器件上的 OTSD 位保持置位状态，直到通过写入 CLR_FLT 位来清除。

7.3.14.7 看门狗故障(仅限 WDFLT、DR703Q)

可以启用 MCU 看门狗功能，以确保指示 DR703Q 设备的外部控制器处于活动状态并处于已知状态。SPI 看门狗必须通过 SPI 向 WD_EN 位写入 1 来启用(默认情况下禁用，WD_EN 位为 0)。当看门狗使能时，内部定时器开始倒计时到 WD_DLY 位设置的时间间隔。MCU 必须在 WD_DLY 位设置的时间间隔内读取寄存器地址 0x00 以重置看门狗。如果允许定时器到期，则启用 nWDFLT 引脚。当启用 nWDFLT 引脚时，会发生以下情况：

- nWDFLT 引脚变低 64µs。
- nFAULT 引脚有效。
- WD_EN 位被清除。
- H 桥中的所有 FET 被禁用。

WDFLT 位保持有效，并且操作停止，直到 CLR_FLT 位被写入 1。Table 19 列出了器件在故障条件下的故障响应。

Table 19. Fault Response

FAULT	CONDITION	H-BRIDGE	CHARGE PUMP	AVDD	DVDD	RECOVERY
VM Undervoltage (UVLO)	$V_{VM} \le V_{(UVLOx)}$ (5.45V, max)	Disabled	Disabled	Disabled	Operating	$V_{VM} \ge V_{(UVLOx)}$ (5.65V, max)
VCP Undervoltage (CPUV)	$V_{VCP} \le V_{(CP_UV)}$ (V_{VM} + 1.5, typ)	Disabled	Operating	Operating	Operating	$V_{VCP} \ge V_{(CP_UV)}$ (V_{VM} + 1.5, typ)
External FET Overload (OCP)	$V_{DS} \ge V_{DS(OCP)}$ V_{SP} V_{SN} > 1V	Disabled	Operating	Operating	Operating	$t_{(RETRY)}$
Gate Driver Fault (GDF)	Gate voltage unchanged after $t_{(DRIVE)}$	Disabled	Operating	Operating	Operating	$t_{(RETRY)}$
Watchdog Fault (WDFLT)	Watchdog timer expires	Disabled	Operating	Operating	Operating	CLR_FLT bit
Thermal Shutdown (TSD)	$T_J \ge T_{SD}$ (150°C, min)	Disabled	Disabled	Disabled	Operating	$T_J \le T_{SD}$ T_{hys} (Thys is typically 20°C.)

7.3.14.8 电源反接保护

可以实施 Figure 37 中的电路来帮助保护系统免受反向电源条件的影响。该电路需要以下附加组件：

- NMOS 场效应管
- NPN BJT
- 二极管
- 10kΩ 电阻
- 43kΩ 电阻

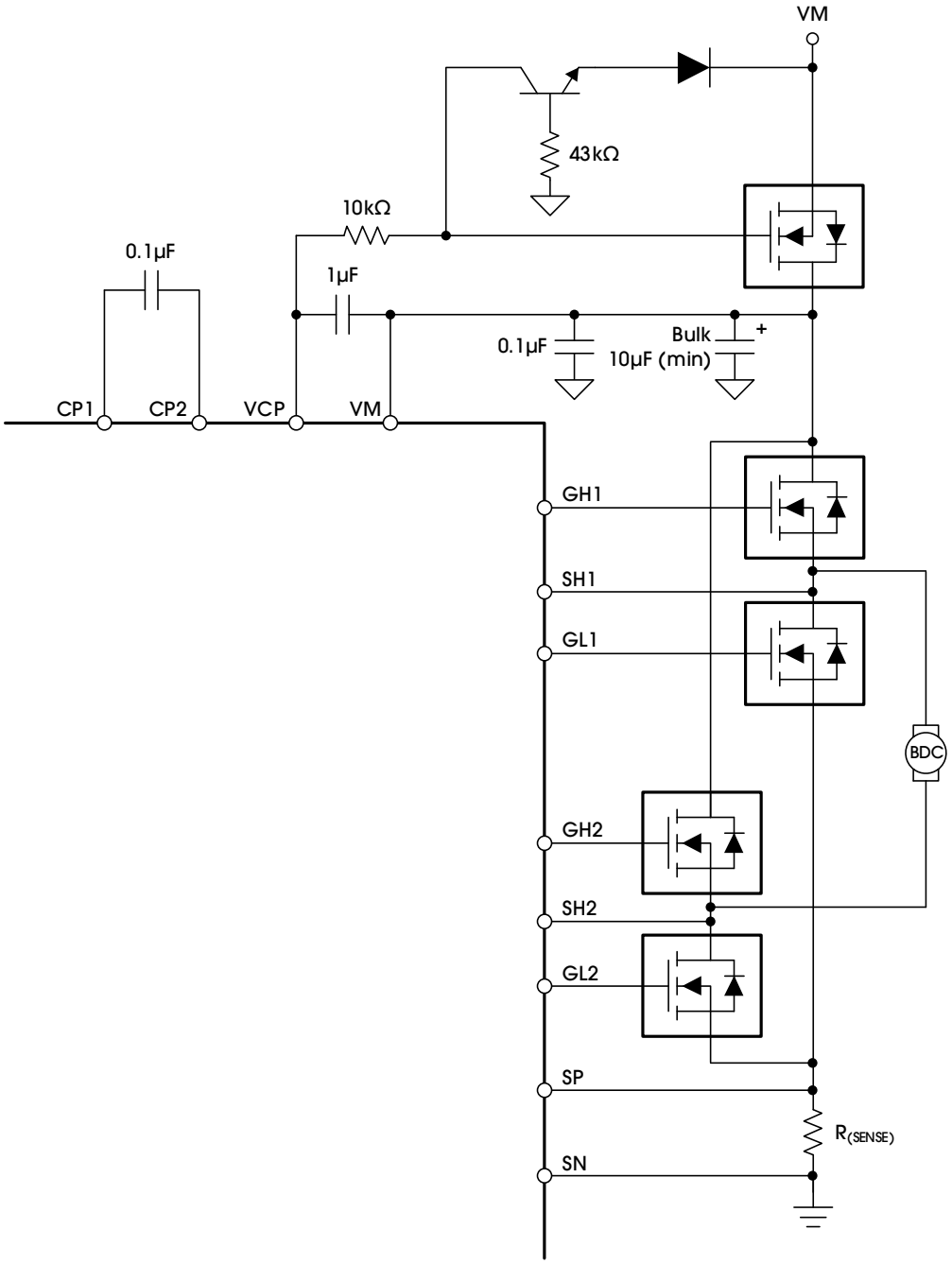


Figure 37. Reverse Supply Protection

7.3.15 硬件接口

DR702Q 硬件接口允许在没有 SPI 的情况下配置设备，但并非所有功能都像 DR703Q 设备一样可配置。硬件接口设备选项的以下配置设置是固定的：

- t_{off} 值设置为 25µs。
- 启用电流调节。
- VREF 引脚电压未在内部调整(100%)。
- 电流检测放大器具有 19.8V/V 的固定增益。

7.3.15.1 IDRIVE (6-LEVEL INPUT)

IDRIVE 引脚上的电压或电阻设置峰值拉电流和峰值灌电流 IDRIVE 配置，如 Table 20 中所列。

Table 20. DR702Q IDRIVE Settings

IDRIVE RESISTANCE	IDRIVE VOLTAGE	SOURCE CURRENT		SINK CURRENT	
		V_{VM} = 5.5V	V_{VM} = 13.5V	V_{VM} = 5.5V	V_{VM} = 13.5V
< 1kΩ to GND	GND	High-side: 6mA Low-side: 8mA	High-side: 10mA Low-side: 10mA	High-side: 14mA Low-side: 17mA	High-side: 20mA Low-side: 20mA
33kΩ ± 5% to GND	0.7V ± 5%	High-side: 12mA Low-side: 16mA	High-side: 20mA Low-side: 20mA	High-side: 28mA Low-side: 35mA	High-side: 40mA Low-side: 40mA
200kΩ ± 5% to GND	2V ± 5%	High-side: 30mA Low-side: 39mA	High-side: 48mA Low-side: 50mA	High-side: 72mA Low-side: 75mA	High-side: 100mA Low-side: 87mA
> 2MΩ to GND, Hi-Z	3V ± 5%	High-side: 100mA Low-side: 100mA	High-side: 152mA Low-side: 120mA	High-side: 180mA Low-side: 204mA	High-side: 253mA Low-side: 240mA
68kΩ ± 5% to AVDD	4V ± 5%	High-side: 130mA Low-side: 139mA	High-side:199mA Low-side: 170mA	High-side: 250mA Low-side: 280mA	High-side: 354mA Low-side: 325mA
< 1kΩ to AVDD	AVDD	High-side: 160mA Low-side: 178mA	High-side: 245mA Low-side: 220mA	High-side: 320mA Low-side: 360mA	High-side: 454mA Low-side: 422mA

7.3.15.2 VDS (6-LEVEL INPUT)

This input controls the VDS monitor trip voltage as listed in Table 21.

Table 21. DR702Q VDS Settings

VDS RESISTANCE	VDS VOLTAGE	OVERCURRENT TRIP LEVEL ($V_{DS(OCP)}$)
< 1kΩ to GND	GND	0.06V
33kΩ ± 5% to GND	0.7V ± 5%	0.12V
200kΩ ± 5% to GND	2V ± 5%	0.24V
> 2MΩ to GND, Hi-Z	3V ± 5%	0.48V
68kΩ ± 5% to AVDD	4V ± 5%	0.96V
< 1kΩ to AVDD	AVDD	Disabled

7.4 器件功能模式

DR702Q/703Q 器件处于活动状态除非 nSLEEP 引脚变低。在睡眠模式下，电荷泵被禁用，H 桥 FET 被禁用到 Hi-Z 状态，AVDD 和 DVDD 稳压器被禁用。在器件进入睡眠模式之前，nSLEEP 引脚上的下降沿之后必须经过 $t_{(SLEEP)}$时间。如果 nSLEEP 引脚变高，DR702Q/703Q 器件会自动退出睡眠模式。在唤醒后输出改变状态之前必须经过 $t_{(WAKE)}$时间。

在 DR703Q 设备上，SPI 设置在退出 UVLO 或退出睡眠模式时重置。当 nSLEEP 引脚变低时，所有外部 H 桥 FET 都被禁用。高侧栅极引脚 GHx 被内部电阻拉至输出节点 SHx，而低侧栅极引脚 GLx 被拉至地。当未施加 VM 电压时以及在上电时间(t_{on})期间，使用 GHx 和 SHx 引脚以及 GLx 和 GND 引脚之间的弱下拉电阻禁用输出。此外，MODE 引脚控制相位和使能、独立半桥或 PWM 输入模式的器件逻辑操作。该操作在上电或退出睡眠模式时被锁存。

7.5 编程

7.5.1 串行外设接口(SPI)

SPI(仅限 DR703Q)用于设置设备配置、运行参数和读出诊断信息。DR703Q SPI 在从机模式下运行。SPI 输入数据(SDI)字由一个 16 位字、一个 5 位命令、3 个无关位和 8 位数据组成。SPI 输出数据(SDO)字由 8 位寄存器数据组成，前 8 位无关。

一个有效的框架必须满足以下条件：

- 时钟极性(CPOL)必须设置为 0。
- 时钟相位(CPHA)必须设置为 1。
- 当 nSCS 引脚变为低电平和 nSCS 引脚变为高电平时，SCLK 引脚必须为低电平。
- 当 nSCS 信号处于转换状态时，不会出现 SCLK 信号。
- 当 nSCS 引脚变为高电平时，SCLK 引脚必须为低电平。
- nSCS 引脚应在帧之间保持至少 500ns 的高电平。
- 当 nSCS 引脚置为高电平时，SCLK 和 SDI 引脚上的任何信号都将被忽略，并且 SDO 引脚处于高阻抗状态。
- 必须出现完整的 16 个 SCLK 周期。
- 数据在时钟的下降沿被捕获，数据在时钟的上升沿被驱动。
- 最高有效位(MSB)先移入移出。
- 对于写命令，如果发送到 SDI 引脚的数据字少于或多于 16 位，则会发生帧错误并且忽略该数据字。
- 对于写命令，正在写入的寄存器中的现有数据在 5 位命令数据之后从 SDO 引脚移出。

7.5.2 SPI 格式

SDI 输入数据字长 16 位，格式如下：

- 1 个读取或写入位，W (第 15 位)
- 4 个地址位，A (位 14 到 11)
- 3 个无关位，X (10 到 8)
- 8 个数据位，D (7:0)

SDO 输出数据字长 16 位，前 8 位为无关位。数据字是被访问的寄存器的内容。

对于写入命令(W0 = 0)，SDO 引脚上的响应字是当前正在写入的寄存器中的数据。

对于读取命令(W0 = 1)，响应字是当前正在读取的寄存器中的数据。

Table 22. SDI Input Data Word Format

R/W	ADDRESS				DON'T CARE			DATA							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
W0	A3	A2	A1	A0	X	X	X	D7	D6	D5	D4	D3	D2	D1	D0

Table 23. SDO Output Data Word Format

DON'T CARE								DATA							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
X	X	X	X	X	X	X	X	D7	D6	D5	D4	D3	D2	D1	D0

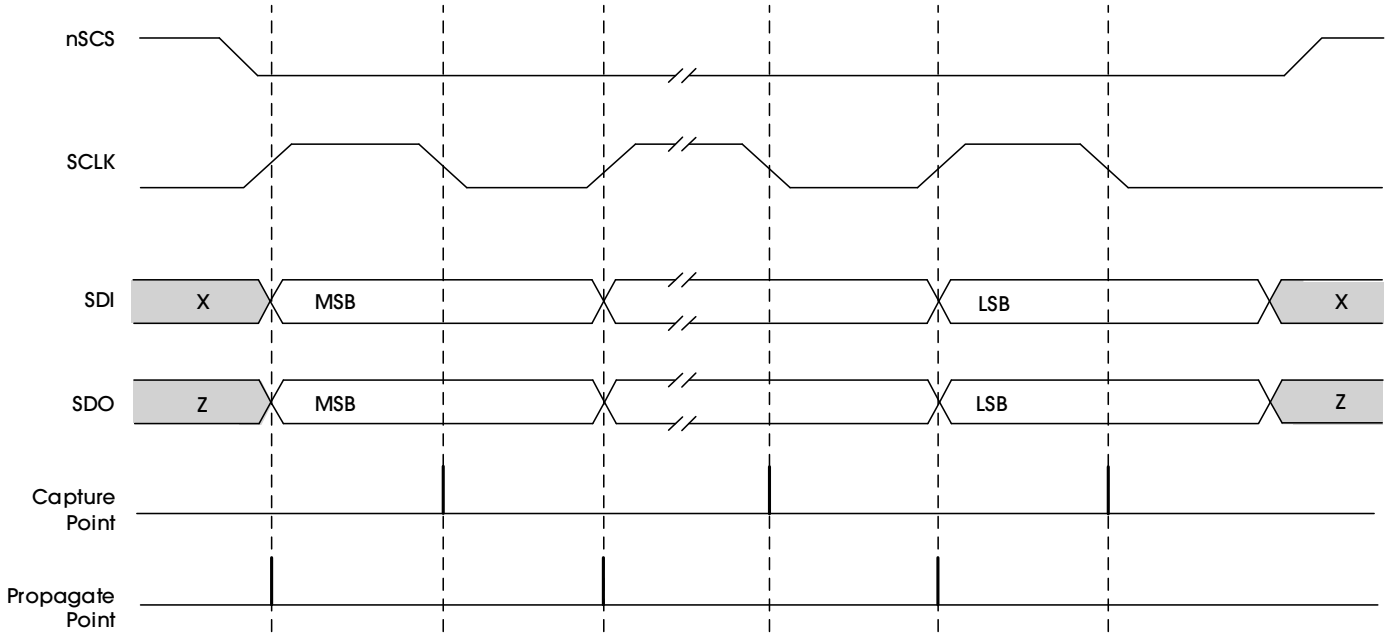


Figure 38. SPI Transaction

SCLK 引脚在器件上电时应为低电平，以实现可靠的 SPI 事务。如果 SCLK 引脚不能保证在加电时为低电平，建议在加电后执行虚拟 SPI 读取事务(任何寄存器的)以确保可靠的后续事务。从这个虚拟读取事务中读取的数据应该被丢弃。

7.6 REGISTER MAPS

Table 24. DR703Q Memory Map

REGISTER NAME	7	6	5	4	3	2	1	0	ACCESS TYPE	ADDRESS (HEX)
FAULT Status	FAULT	WDFLT	GDF	OCP	VM_UVFL	VCP_UVFL	OTSD	OTW	R	0
VDS and GDF	H2_GDF	L2_GDF	H1_GDF	L1_GDF	H2_VDS	L2_VDS	H1_VDS	L1_VDS	R	1
Main	Chip ID		LOCK			IN1/PH	IN2/EN	CLR_FLT	R/W	2
IDRIVE and WD	TDEAD		WD_EN	WD_DLY		IDRIVE			R/W	3
VDS	SO_LIM	VDS			DIS_H2_VDS	DIS_L2_VDS	DIS_H1_VDS	DIS_L1_VDS	R/W	4
Config	TOFF		CHOP_IDS	VREF_SCL		SH_EN	GAIN_CS		R/W	5

Table 25. Access Type Codes

ACCESS TYPE	CODE	DESCRIPTION
READ TYPE		
R	R	Read
WRITE TYPE		
W	W	Write

7.6.1 STATUS REGISTERS

The status registers are used to report warning and fault conditions. Status registers are read only registers. Table 26 lists the memory-mapped registers for the status registers. All register offset addresses not listed in Table 26 should be considered as reserved locations and the register contents should not be modified.

Table 26. Status Registers

ADDRESS	REGISTER NAME
0x00h	FAULT status
0x01h	VDS and GDF status

7.6.2 FAULT STATUS REGISTER (ADDRESS = 0X00H)

FAULT status is shown in Table 27 and described in Table 28. Return to Summary Table.

Read only. For the first power-on, the register is read out to be 0x8C. It is normal as both VM and VCP will go through undervoltage threshold when digital is active. Hence, clear faults just after the power-on.

Table 27. FAULT Status Register

7	6	5	4	3	2	1	0
FAULT	WDFLT	GDF	OCP	VM_UVFL	VCP_UVFL	OTSD	OTW
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 28. FAULT Status Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	FAULT	R	1b	Logic OR of the FAULT status register, excluding the OTW bit
6	WDFLT	R	0b	Watchdog time-out fault
5	GDF	R	0b	Indicate gate drive fault condition
4	OCP	R	0b	Indicate VDS monitor overcurrent fault condition
3	VM_UVFL	R	1b	Indicate VM undervoltage lockout fault condition
2	VCP_UVFL	R	1b	Indicate charge-pump undervoltage fault condition
1	OTSD	R	0b	Indicate overtemperature shutdown
0	OTW	R	0b	Indicate overtemperature warning

7.6.3 VDS AND GDF STATUS REGISTER NAME (ADDRESS = 0X01H)

VDS and GDF status is shown in Table 29 and described in Table 30. Return to Summary Table.

Read only

Table 29. VDS and GDF Status Register

7	6	5	4	3	2	1	0
H2_GDF	L2_GDF	H1_GDF	L1_GDF	H2_VDS	L2_VDS	H1_VDS	L1_VDS
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 30. VDS and GDF Status Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	H2_GDF	R	0b	Indicate gate drive fault on the high-side FET of half-bridge 2
6	L2_GDF	R	0b	Indicate gate drive fault on the low-side FET of half-bridge 2
5	H1_GDF	R	0b	Indicate gate drive fault on the high-side FET of half-bridge 1
4	L1_GDF	R	0b	Indicate gate drive fault on the low-side FET of half-bridge 1
3	H2_VDS	R	0b	Indicate VDS monitor overcurrent fault on the high-side FET of half-bridge 2
2	L2_VDS	R	0b	Indicate VDS monitor overcurrent fault on the low-side FET of half-bridge 2
1	H1_VDS	R	0b	Indicate VDS monitor overcurrent fault on the high-side FET of half-bridge 1
0	L1_VDS	R	0b	Indicate VDS monitor overcurrent fault on the low-side FET of half-bridge 1

7.6.4 CONTROL REGISTERS

The control registers are used to configure the device. Control registers are read and write capable. Table 31 lists the memory-mapped registers for the status registers. All register offset addresses not listed in Table 31 should be considered as reserved locations and the register contents should not be modified.

Table 31. Control Registers

ADDRESS	REGISTER NAME
0x02h	Main control
0x03h	IDRIVE and WD control
0x04h	VDS control
0x05h	Config control

7.6.5 MAIN CONTROL REGISTER NAME (ADDRESS = 0X02H)

Main control is shown in Table 32 and described in Table 33. Return to Summary Table.

Read and write

Table 32. Main Control Register

7	6	5	4	3	2	1	0
Chip ID		LOCK			IN1/PH	IN2/EN	CLR_FLT
R-01b		R/W-011b			R/W-0b	R/W-0b	R/W-0b

Table 33. Main Control Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7-6	Chip ID	R	01b	Chip ID and read only.
5-3	LOCK	R/W	011b	Write 110b to lock the settings by ignoring further register changes except to address 0x02h. Writing any sequence other than 110b has no effect when unlocked. Write 011b to this register to unlock all registers. Writing any sequence other than 011b has no effect when locked.
2	IN1/PH	R/W	0b	This bit is ORed with the IN1/PH pin.
1	IN2/EN	R/W	0b	This bit is ORed with the IN2/EN pin
0	CLR_FLT	R/W	0b	Write a 1 to this bit to clear the fault bits.

7.6.6 IDRIVE AND WD CONTROL REGISTER NAME (ADDRESS = 0X03H)

IDRIVE and WD control is shown in Table 34 and described in Table 35. Return to Summary Table.

Read and write

Table 34. IDRIVE and WD Register

7	6	5	4	3	2	1	0
TDEAD		WD_EN	WD_DLY		IDRIVE		
R/W-00b		R/W-0b	R/W-00b		R/W-111b		

Table 35. IDRIVE and WD Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7-6	TDEAD	R/W	00b	Dead time 00b = 120ns 01b = 240ns 10b = 480ns 11b = 960ns
5	WD_EN	R/W	0b	Enable or disable the watchdog time (disabled by default)
4-3	WD_DLY	R/W	00b	Watchdog timeout delay (if WD_EN = 1) 00b = 10ms 01b = 20ms 10b = 50ms 11b = 100ms
2-0	IDRIVE	R/W	111b	Set the peak source current and peak sink current of the gate drive. Table 36 lists the bit settings.

Table 36. IDRIVE Bit Settings

BIT VALUE	SOURCE CURRENT		SINK CURRENT	
	V_{VM} = 5.5V	V_{VM} = 13.5V	V_{VM} = 5.5V	V_{VM} = 13.5V
000b	High-side: 6mA Low-side: 8mA	High-side: 10mA Low-side: 10mA	High-side: 14mA Low-side: 17mA	High-side: 20mA Low-side: 20mA
001b	High-side: 12mA Low-side: 16mA	High-side: 20mA Low-side: 20mA	High-side: 28mA Low-side: 35mA	High-side: 40mA Low-side: 40mA
010b	High-side: 30mA Low-side: 39mA	High-side: 48mA Low-side: 50mA	High-side: 72mA Low-side: 75mA	High-side: 100mA Low-side: 87mA
011b	High-side: 42mA Low-side: 54mA	High-side:67 mA Low-side:70 mA	High-side: 100mA Low-side:108 mA	High-side: 140mA Low-side:125 mA
100b	High-side: 60mA Low-side: 77mA	High-side:95 mA Low-side:100 mA	High-side: 140mA Low-side: 158mA	High-side: 200mA Low-side: 184mA
101b	High-side: 100mA Low-side: 100mA	High-side: 152mA Low-side: 120mA	High-side: 180mA Low-side: 204mA	High-side: 253mA Low-side: 240mA
110b	High-side: 130mA Low-side: 139mA	High-side: 199mA Low-side: 170mA	High-side: 250mA Low-side: 280mA	High-side: 354mA Low-side: 325mA
111b	High-side: 160mA Low-side: 178mA	High-side: 245mA Low-side: 220mA	High-side: 320mA Low-side: 360mA	High-side: 454mA Low-side: 422mA

7.6.7 VDS CONTROL REGISTER NAME (ADDRESS = 0X04H)

VDS control is shown in Table 37 and described in Table 38. Return to Summary Table.

Read and write

Table 37. VDS Control Register

7	6	5	4	3	2	1	0
SO_LIM	VDS			DIS_H2_VDS	DIS_L2_VDS	DIS_H1_VDS	DIS_L1_VDS
R/W-0b	R/W-111b			R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 38. VDS Control Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	SO_LIM	R/W	0b	0b = Default operation 1b = SO output is voltage-limited to 3.6V
6-4	VDS	R/W	111b	Set the $V_{DS(OCP)}$ monitor for each FET 000b = 0.06V 001b = 0.145V 010b = 0.17V 011b = 0.2V 100b = 0.12V 101b = 0.24V 110b = 0.48V 111b = 0.96V
3	DIS_H2_VDS	R/W	0b	Disable the VDS monitor on the high-side FET of half-bridge 2 (enabled by default)
2	DIS_L2_VDS	R/W	0b	Disable the VDS monitor on the low-side FET of half-bridge 2 (enabled by default)
1	DIS_H1_VDS	R/W	0b	Disable the VDS monitor on the high-side FET of half-bridge 1 (enabled by default)
0	DIS_L1_VDS	R/W	0b	Disable the VDS monitor on the low-side FET of half-bridge 1 (enabled by default)

7.6.8 CONFIG CONTROL REGISTER NAME (ADDRESS = 0X05H)

Config control is shown in Table 39 and described in Table 40. Return to Summary Table.

Read and write

Table 39. Config Control Register

7	6	5	4	3	2	1	0
TOFF		CHOP_IDS	VREF_SCL		SH_EN	GAIN_CS	
R/W-00b		R/W-0b	R/W-00b		R/W-0b	R/W-01b	

Table 40. Config Control Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7-6	TOFF	R/W	00b	Off time for PWM current chopping 00b = 25µs 01b = 50µs 10b = 100µs 11b = 200µs
5	CHOP_IDS	R/W	0b	Disable current regulation (enabled by default)
4-3	VREF_SCL	R/W	00b	Scale factor for the VREF input 00b = 100% 01b = 75% 10b = 50% 11b = 25%
2	SH_EN	R/W	0b	Enable sample and hold operation of the shunt amplifier (disabled by default)
1-0	GAIN_CS	R/W	01b	Shunt amplifier gain setting 00b = 10V/V 01b = 19.8V/V 10b = 39.4V/V 11b = 78V/V

8. 应用和实现

注

以下应用部分中的信息不是 AnalogySemi 器件规范的一部分，AnalogySemi 不保证其准确性或完整性。AnalogySemi 的客户有责任确定器件是否适合他们的应用。客户应验证和测试他们的设计实施以确认系统功能。

8.1 典型应用

DR702Q 典型应用如下图：

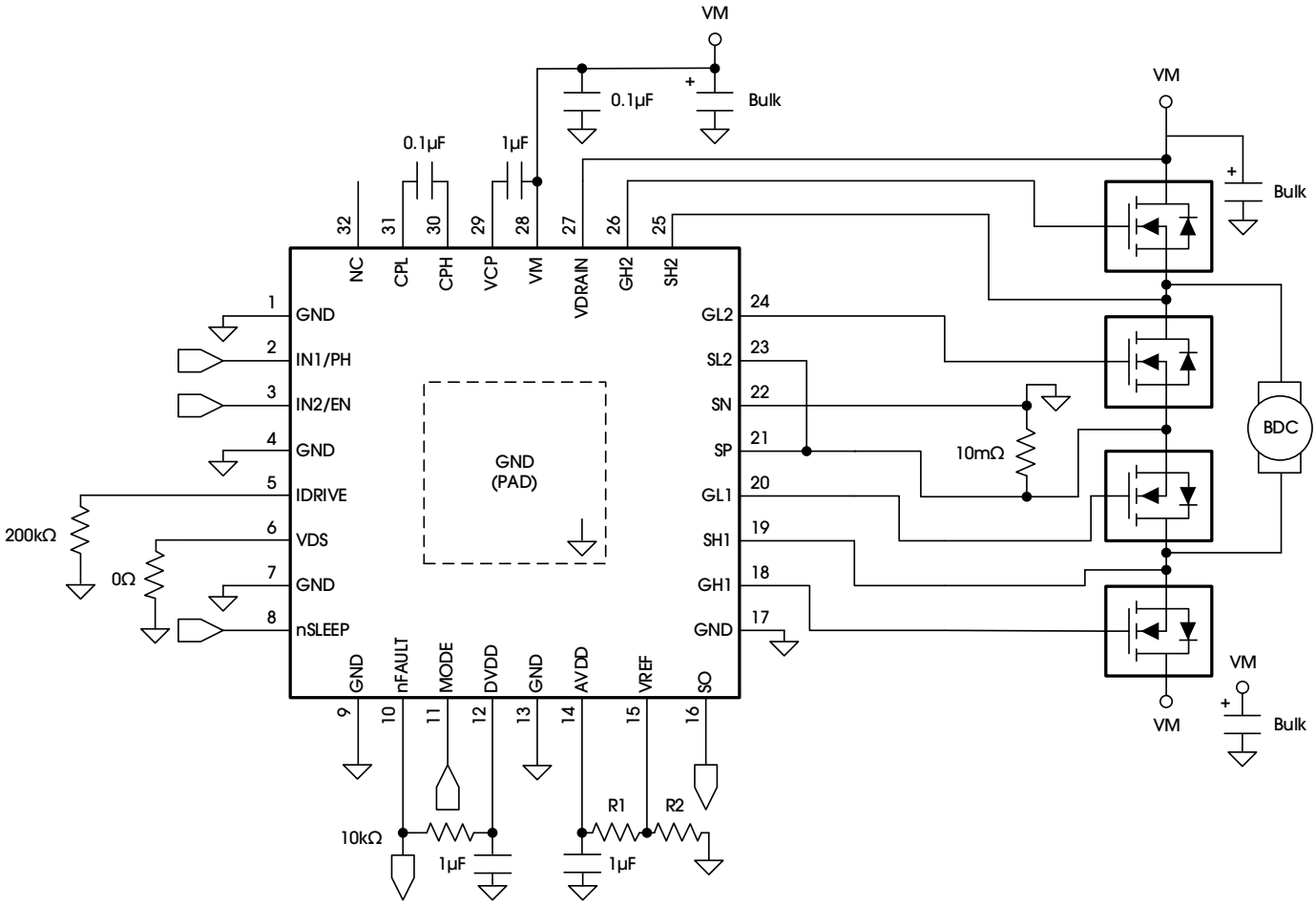


Figure 39. DR702Q Typical Application Schematic

8.1.1 详细设计步骤

8.1.1.1 外部 FET 选择

DR702Q FET 的选择是基于电荷泵容量和 PWM 输出频率。要快速计算 FET 驱动能力，驱动和慢刹(slow decay)是主要操作模式时使用 Equation 3。

$$Q_g < \frac{I_{VCP}}{t_{(PWM)}} \tag{3}$$

其中：

- f_{PWM} 是应用于 DR702Q 输入的最大所需 PWM 频率或当前斩波频率，以较大者为准。
- I_{VCP} 是电荷泵容量，取决于 VM 电压。

内部电流斩波频率不高于 PWM 频率，如 Equation 4 所示。

$$f_{(PWM)} < \frac{1}{t_{off} + t_{(BLANK)}} \tag{4}$$

例如，如果系统的 VM 电压为 7V (I_{VCP} = 8mA)并使用 40kHz 的最大 PWM 频率，则 DR702Q 器件将支持 Q_g 高达 200nC 的 FET。

如果应用需要强制快速衰减(或在驱动和反向驱动之间交替)，请使用 Equation 5 计算最大 FET 驱动能力。

$$Q_g < \frac{I_{VCP}}{2 \times f_{(PWM)}} \tag{5}$$

8.1.1.2 IDRIVE 配置

IDRIVE 电流是根据 FET 的栅极电荷来选择的。必须配置 IDRIVE 引脚，以便 FET 栅极在 $t_{(DRIVE)}$时间内完全充电。如果所选的 IDRIVE 电流对于给定的 FET 来说太低，则 FET 可能无法完全导通。建议使用所需的外部 FET 和电机在系统内调整这些值，以获得和应用相匹配的最佳配置。

对于具有已知栅漏电荷(Q_{gd})和所需上升时间(t_r)的 FET，可以根据 Equation 6 选择 IDRIVE 电流。

$$I_{DRIVE} > \frac{Q_{gd}}{t_r} \tag{6}$$

如果栅极至漏极电荷为 8.4nC 并且所需的上升时间约为 100ns 至 300ns，则使用 Equation 7 计算最小 IDRIVE (I_{DRIVE1})，使用 Equation 8 计算最大 IDRIVE (I_{DRIVE2})。

$$I_{DRIVE1} = 8.4nC / 100ns = 84mA \tag{7}$$

$$I_{DRIVE2} = 8.4nC / 300ns = 28mA \tag{8}$$

为 IDRIVE 选择一个介于 28mA 和 84mA 之间的值。针对这种情况，建议选择大约 50mA 的源电流 IDRIVE 值(大约 100mA 的灌电流)。该值的配置只需要一个 200kΩ 的电阻从 IDRIVE 引脚接地。

8.1.1.3 VDS 配置

VDS 监控阈值电压 $V_{DS(OCP)}$根据 FET 的最大电流 I_{VDS} 和 $R_{DS(on)}$配置。漏源电压 V_{DSFET} 是最大电流 I_{VDS} 乘以 FET 的 $R_{DS(on)}$。DR702Q 的 VDS 引脚选择 VDS 监视器触发阈值 $V_{DS(OCP)}$。DR703Q 的 VDS 寄存器中的 VDS 位选择 $V_{DS(OCP)}$电压。使用 Equation 9 计算跳闸电流。

$$I_{VDS} > \frac{V_{DSFET}}{R_{DS(on)}} \tag{9}$$

如果 FET 的 $R_{DS(on)}$为 1.8mΩ 并且所需的最大电流小于 100A，则 V_{DSFET} 电压等于 180mV，如 Equation 10 所示。

对于此示例，为 $V_{DS(OCP)}$选择一个小于 180mV 的值。为此应用选择了 0.12V 的 $V_{DS(OCP)}$值。要将 $V_{DS(OCP)}$设置为 0.12V，请使用 SPI (仅限 DR703Q)或在 VDS 引脚处放置一个 33k 电阻接地(仅限 DR702Q)。VDS 引脚可以配置为选择其他 $V_{DS(OCP)}$阈值电压。有关 VDS 操作的更多信息，请参见 VDS PIN 部分。

$$V_{DSFET} = I_{VDS} \times R_{DS(on)} = 100A \times 1.8m\Omega = 180mV \tag{10}$$

8.1.1.4 电流斩波配置

斩波电流根据检测电阻值和 VREF 引脚上的模拟电压设置。使用 Equation 11 计算电流($I_{(CHOP)}$)。DR702Q 的放大器增益 A_V 为 19.8V/V，V_{IO} 通常为 3.7mV (参考输入)。

$$I_{(CHOP)} = \frac{V_{VREF} - V_{IO} \times A_V}{A_V \times R_{(SENSE)}} \quad (11)$$

例如，如果所需的斩波电流为 15A，则为 $R_{(SENSE)}$选择 10mΩ 的值。因此，V_{VREF} 的值必须为 2.975V。从 AVDD (5V)引脚添加一个电阻分压器，将 V_{VREF} 设置为大约 2.975V。为 R1 (VREF 电阻器)选择 13kΩ 的值，为 R2 选择 19.1kΩ 的值。如果不需要电流斩波，则可以移除检测电阻器并将低侧 FET 的源极接地。SN 和 SP 应连接到低侧 FET 的源极，VREF 应连接到 AVDD。

9. 电源供电推荐

DR702Q 器件设计用于在 5.5V 至 45V 的输入电压电源(VM)范围内运行。额定值为 VM 的 0.1µF 陶瓷电容器必须尽可能靠近 DR702Q 器件放置。此外，必须在 VM 引脚上放置一个值至少为 10µF 的大容量电容器，考虑到外部的 H 桥 FET，还需要额外的大电容进行旁路去耦。

9.1 去耦电容

去耦电容大小是电机驱动系统设计中的一个重要因素。使用更多的大电容是有益的，但是缺点是增加了成本和物理尺寸。

所需局部电容的大小取决于多种因素，包括：

- 电机系统所需的最大电流
- 电源的电容和电源提供电流的能力
- 电源和电机系统之间的寄生电感量
- 可接受的电压纹波
- 使用的电机类型(有刷直流、无刷直流和步进电机)
- 电机制动方式

电源和电机驱动系统之间的寄生电感限制了电源电流变化的速率。如果局部大电容太小，系统为了响应瞬时大电流，此时电压会变低。当使用足够的大容量电容时，电机电压保持稳定，可以正常快速提供大电流。数据表提供了推荐值，但需要进行系统级测试以确定合适大小的大容量电容器。

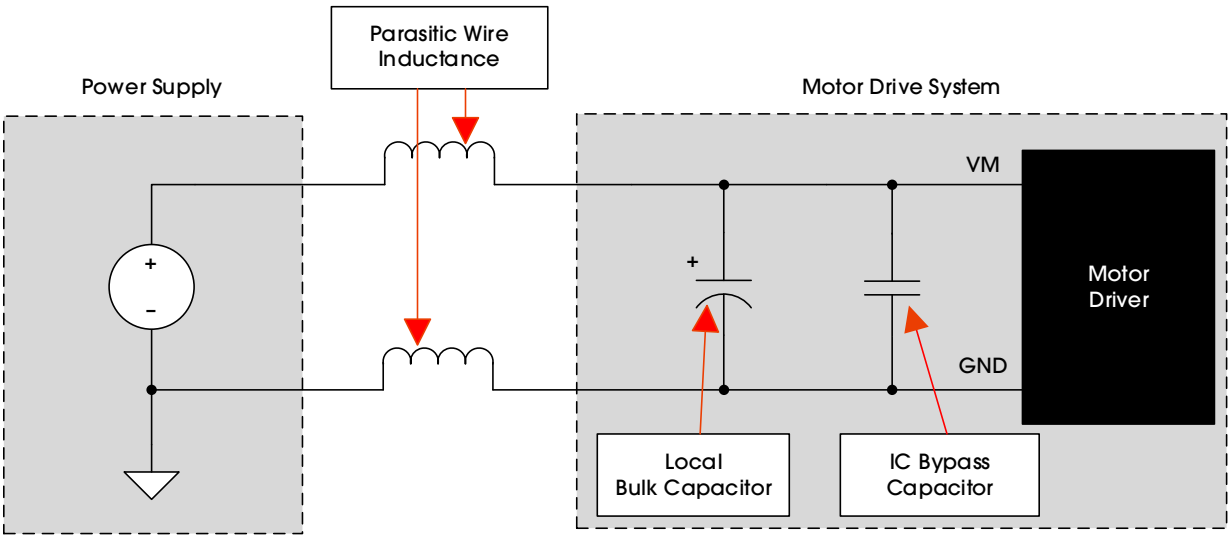


Figure 40. Example Setup of Motor Drive System With External Power Supply

大容量电容器的额定电压应高于工作电压，以便有足够的余量应付电机能量向电源转移的情况。

10. 布局

10.1 布局建议

应使用低 ESR 陶瓷旁路电容器将 VM 引脚旁路至地，建议 VM 额定值为 0.1μF。该电容器应放置在尽可能靠近 VM 引脚的位置，并通过粗走线或接地平面连接到器件的 GND 引脚。VM 引脚还必须使用额定为 VM 的大容量电容器旁路接地。该电容器可以是电解电容器，并且必须至少为 10μF。

必须在 CPL 和 CPH 引脚之间放置一个低 ESR 陶瓷电容器。建议 VM 的额定值为 0.1μF。将此电容器放置在尽可能靠近引脚的位置。必须在 VM 和 VCP 引脚之间放置一个低 ESR 陶瓷电容器。推荐 16V 额定值 1μF。将该组件放置在尽可能靠近引脚的位置。

使用额定电压为 6.3V 的陶瓷电容器将 AVDD 和 DVDD 引脚旁路到地。将这些旁路电容器尽可能靠近引脚放置。

使用独立走线将 SP 和 SN 引脚连接到 $R_{(SENSE)}$电阻器。

10.2 布局示例

请参考 EVM 或者咨询 AnalogySemi 销售支持。

11. PACKAGE INFORMATION

The DR702Q/703Q is available in the QFN-32 package. Figure 41 shows the package view.

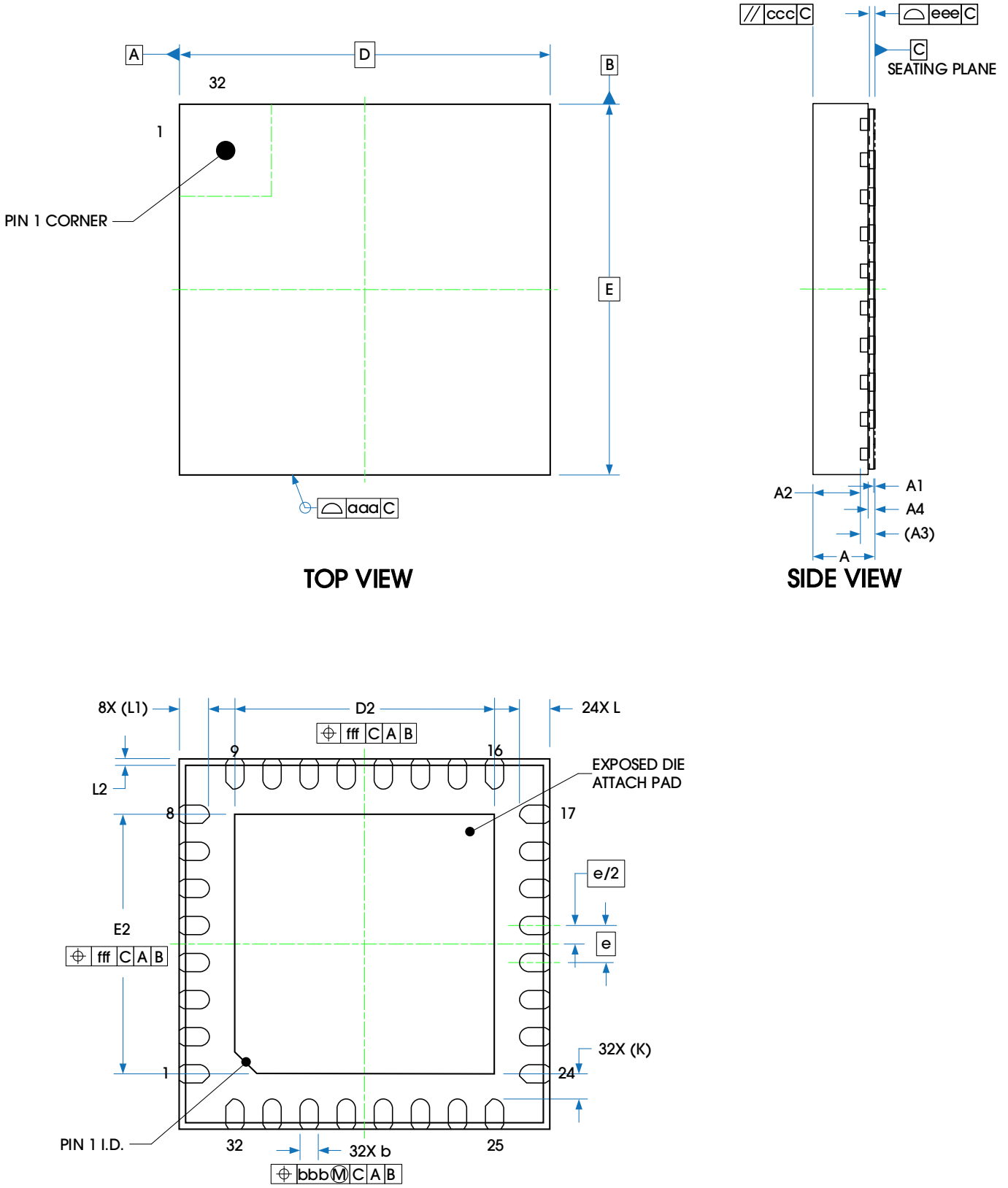


Figure 41. Package View

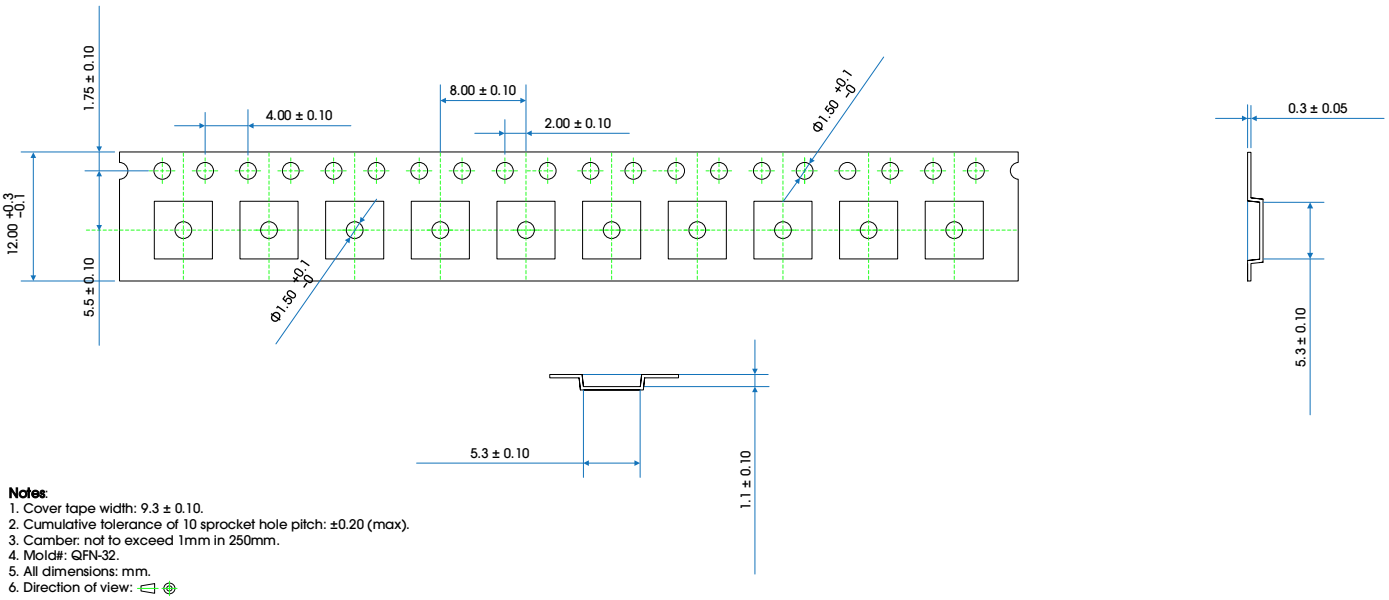
Table 41 provides detailed information about the dimensions.

Table 41. Dimensions

PARAMETER		SYMBOL	DIMENSIONS IN MILLIMETERS		
			MIN	NOM	MAX
Total Thickness		A	0.8	0.85	0.9
Stand Off		A1	0	0.02	0.05
Mold Thickness		A2	—	0.65	—
L/F Thickness		A3		0.203 REF	
Side Wettable Depth		A4	0.075	—	0.2
Lead Width		b	0.2	0.25	0.3
Body Size	X	D		5 BSC	
	Y	E		5 BSC	
Lead Pitch		e		0.5 BSC	
EP Size	X	D2	3.4	3.5	3.6
	Y	E2	3.4	3.5	3.6
Lead Length		L	0.3	0.4	0.5
		L1		0.4 REF	
Side Wettable Width		L2	0	—	0.075
Lead Tip to Exposed Pad Edge		K		0.35 REF	
Package Edge Tolerance		aaa		0.1	
Mold Flatness		ccc		0.1	
Coplanarity		eee		0.08	
Lead Offset		bbb		0.1	
Exposed Pad Offset		fff		0.1	

12. TAPE AND REEL INFORMATION

Figure 42 illustrates the carrier tape.



Notes:
1. Cover tape width: 9.3 ± 0.10.
2. Cumulative tolerance of 10 sprocket hole pitch: ±0.20 (max).
3. Camber: not to exceed 1mm in 250mm.
4. Mold#: QFN-32.
5. All dimensions: mm.
6. Direction of view:

Figure 42. Carrier Tape Drawing

Table 42 provides information about tape and reel.

Table 42. Tape and Reel Information

PACKAGE TYPE	REEL	QTY/REEL	REEL/ INNER BOX	INNER BOX/ CARTON	QTY/CARTON	INNER BOX SIZE (mm)	CARTON SIZE (mm)
QFN-32 5*5	13''	4000	1	8	32000	336*336*448	420*355*365

Figure 43 shows the product loading orientation—pin 1 is assigned at Q2.

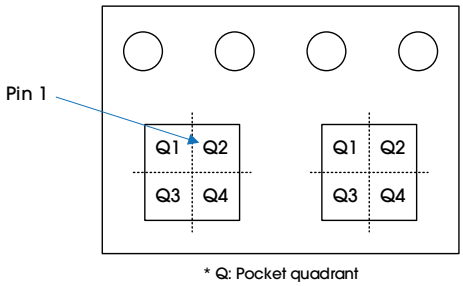


Figure 43. Product Loading Orientation

REVISION HISTORY

REVISION	DATE	DESCRIPTION
Rev A	04 April 2023	Rev A release.
Rev B	16 June 2023	Updated the ESD test standard description.
Rev C	16 October 2025	Added TPSEMI logo, updated the order information and the TYP for I_{VM}.
Rev D	11 August 2026	Updated the order information, Table 3, and Section 8.1.1.4. Added Figure 2.