TMI8140-Q1 40V 7A H-Bridge DC Motor Driver

FEATURES

- H-Bridge DC Motor Driver
- 8V to 40V Operating Supply Voltage Range
- Low Power Standby Mode
- High Output Current Capability
  -DFN5*6_15:7A DC
- PWM Control Interface
- Rdson(HS+LS): 45~50 mΩ
- Protection Features
  -VCC Undervoltage Lockout (UVLO)
  -Overcurrent Protection (OCP)
  -Thermal Shutdown (TSD)
  -Short Protection (short to VM or short to GND)
  -Integrated Fast Stop Function
- Package and Footprint:
  -DFN5*6_15

APPLICATIONS

- Brushed DC motors
- Body control module (BCM)
- Door lock
- Inner / Outer door handle
- Massager
- Robots

GENERAL DESCRIPTION

The TMI8140-Q1 is a DC bidirectional motor driver, suitable for medium and large current motors.

The two logic input terminals(IN1/IN2) are used as the input of PWM control mode to control the direction of current flow through the H-bridge, and hence the direction of rotation of a DC motor.

This circuit has good anti-interference, tiny standby current, ultra-low output internal resistance, using BCD process, strong withstand voltage, and strong reverse surge current capability to release inductive load.

The package form of TMI8140-Q1 is DFN5*6_15, and is comply with ROHS specifications, and the lead frame is 100% lead-free.

TYPICAL APPILCATION

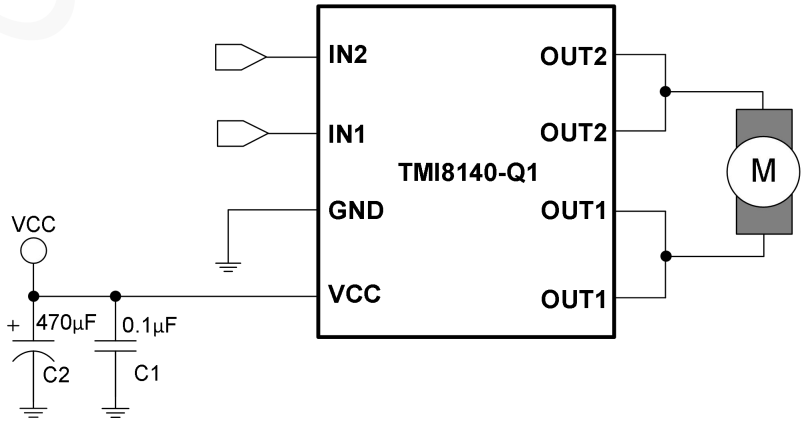


Figure 1. Basic Application Circuit

Block Diagram

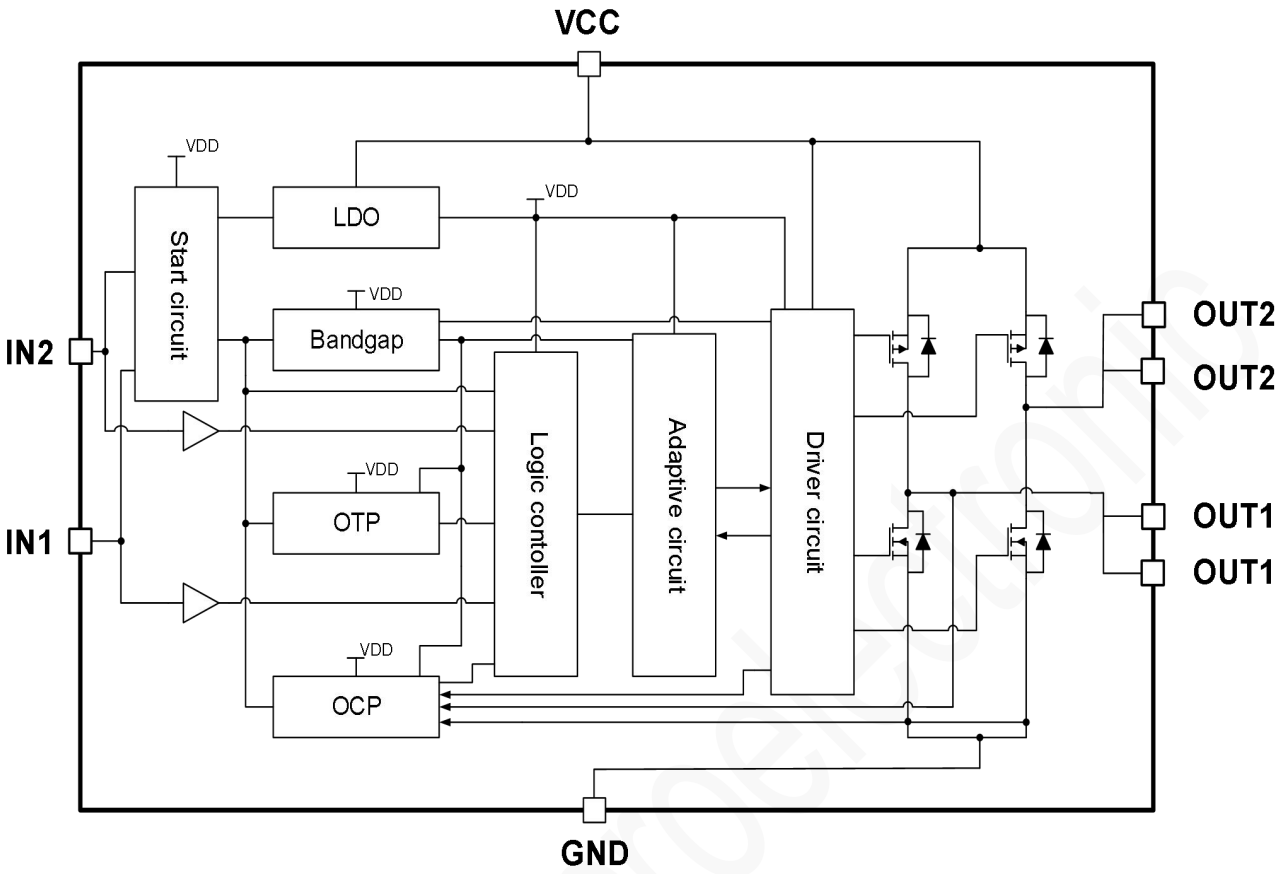


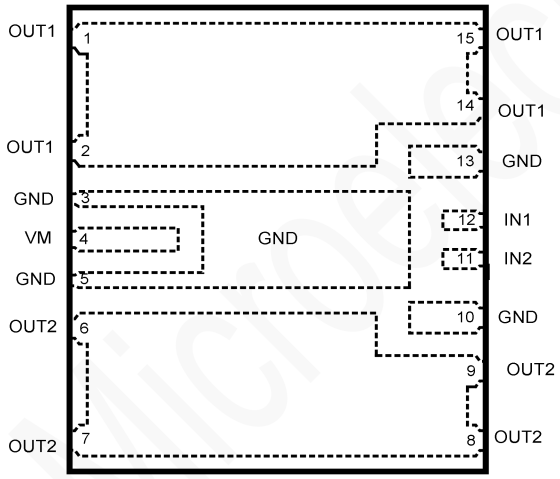
Figure 2. TMI8140-Q1 Block Diagram

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ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Min	Max	Unit
Power supply voltage (VCC)	-0.3	40	V
Logic input voltage (IN2, IN1)	-0.3	VCC	V
Output continuous current (IOUT) (Note 2)	0	7.0	A
Operating ambient temperature	-40	125	°C
Power consumption (PD)	0	2.5	W
Operating junction temperature (Note 3)	-40	150	°C
Storage temperature	-55	150	°C

PACKAGE/ORDER INFORMATION



TMI8140-Q1 (Top View)
DFN5*6_15

Part Number	Package	Top mark	Quantity/ Reel
TMI8140-Q1	DFN5*6_15	TMI8140-Q1 XXXXXX	5000

TMI8140-Q1 device is Pb-free and RoHS compliant.

PIN FUNCTIONS

Pin	Name	I/O	Description
1、2、14、15	OUT1	Output	Forward output.
3、5、10、13	GND	Ground	Device ground.
4	VCC	Power	Power supply.
6、7、8、9	OUT2	Output	Reverse output.
11	IN2	Input	Reverse logic control.
12	IN1	Input	Forward logic control.

ESD RATING

Items	Description	Value	Unit
V_{ESD}	Human body model for all pins	±2000	V

JEDEC specification JS-001

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Units
Power supply voltage range	VCC	8	40	V
Logic input voltage range	V_{IN_X}	-0.3	6	V
Output continuous current (DFN5*6_15)	I_{OUT_X}	0	7.0	A
Logic input frequency	F_{IN_X}	0	50	kHz

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ELECTRICAL CHARACTERISTICS

(T_A = 25°C, over recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Power supply (VCC)						
Operation voltage	V_{VCC}		8		40	V
Shutdown current	I_{SDT}	VCC=24V, IN1=IN2=0V, no load			1	μA
Standby current	I_{BRAKE}	VCC=24V, IN1=IN2=5V or IN1=5V & IN2=0V or IN1=0V & IN2=5V, no load	0.3	0.6	1	mA
PWM current	I_{PWM}	VCC=24V, IN1=5V, IN2=50kHz, no load	1	1.5	3	mA
Turn-on time	t_{WAKE}	Sleep mode to active mode delay	10	15	20	us
Auto-sleep Turn-off time	$t_{AUTOSLEEP}$	Active mode to autosleep mode delay	0.8	1	1.5	ms
Undervoltage lockout	UVLO	VCC rising	4.6	4.7	4.9	V
Logic inputs						
Input logic high voltage	V_{INH}	VCC = 24V, no load	1.5		6	V
Input logic low voltage	V_{INL}	VCC = 24V, no load			1.2	V
Input logic high current	I_{INH}	VCC = 24V, V_{IN} = 5V		50	100	μA
Input logic low current	I_{INL}	VCC = 24V, V_{IN}= 0V			1	μA
H-bridge FETs						
FETs on resistance	$R_{ds(on)}$	I_{LOAD}=1A, HS+LS		45		mΩ
FETs on resistance	$R_{ds(on)}$	I_{LOAD}=3A, HS+LS		50		mΩ
Delay time during output voltage rise	t_{pd_on}	VCC = 24V, Load = 50Ω+1mH		150		ns
Rise time	t_{rise}		18		50	ns
Dead time during output voltage rise	t_{dead_on}			310		ns
Delay time during output voltage fall	t_{pd_off}			110		ns
Fall time	t_{fall}		15		40	ns
Dead time during output voltage fall	t_{dead_off}			200		ns

ELECTRICAL CHARACTERISTICS (Continued)

T_A = 25°C, (unless otherwise noted.)

Over temperature protection						
Thermal shutdown temperature (Note4)	T_{SD}	VCC = 24V, V_{IN} = 1Hz		170		°C
Thermal shutdown hysteresis (Note4)	T_{HYS}			40		°C
Over current protection						
Overcurrent protection trip current	I_{OCP}	VCC = 24V		13.0		A
Overcurrent deglitch time	t_{OCP}			2.5		μs

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Power dissipation and thermal limits must be observed.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula: $T_J = T_A + P_D \times \theta_{JA}$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_{D\,(MAX)} = (T_{J(MAX)}-T_A)/\theta_{JA}$.

Note 4: Thermal shutdown threshold and hysteresis are guaranteed by design.

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OPERATION

Bridge Control

The TMI8140-Q1 output consists of 4 internal P+N channel MOSFETs that are designed to drive high current. These outputs are controlled by the two logic inputs IN1 and IN2 as listed in Table 1.

Table 1. H-Bridge Control

IN1	IN2	OUT1	OUT2	DESCRIPTION
L	L	High-Z	High-Z	Coast; H-bridge disabled to High-Z
L	H	L	H	Reverse (Current OUT2 →OUT1)
H	L	H	L	Forward (Current OUT1 →OUT2)
H	H	L	L	Brake; low-side slow decay

Output Timing Diagram

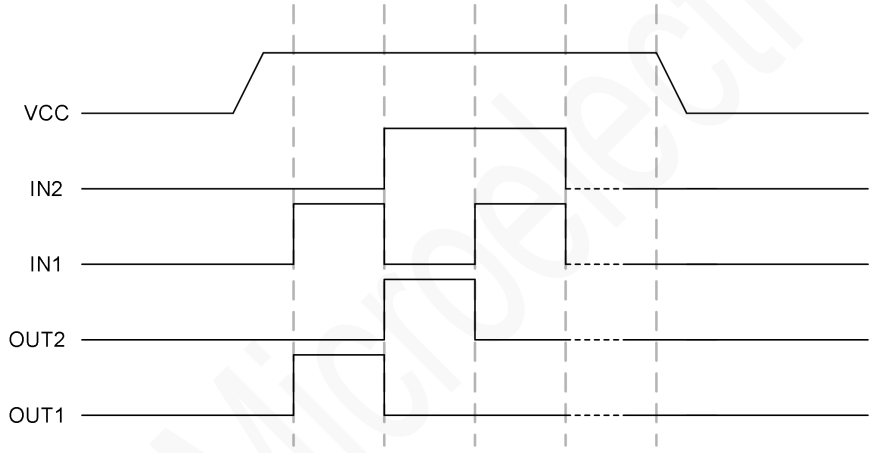


Figure 3. TMI8140-Q1 Output Timing Diagram

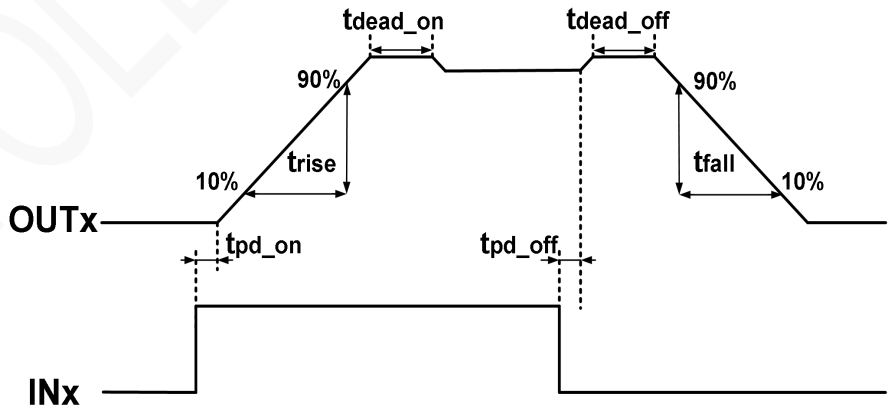


Figure 4. TMI8140-Q1 Input Output Logic

Application Directions

The peripheral components on the typical application circuit as shown in Figure 1 are described as follows:

C1 and C2 are VCC input capacitors, the main functions are as follows:

1. Absorb the energy released by the motor to the power supply, stabilize the VCC power supply voltage, prevent the IC from being directly broken down due to the high surge voltage, and have the function of filtering ripple and interference noise.
2. At the moment when the motor starts, it can release current to help the motor start quickly.
3. The selection of the VCC input capacitor C2 needs to be based on the voltage stability of the VCC and the motor load current. If the VCC voltage wave is large or the motor load current is large, a larger capacitor value must be selected.It is recommended that the C2 capacitance is greater than 100uF.
4. C1 and C2 capacitors need to be as close to VCC as possible on the PCB configuration.

Work Mode Directions

Basic working mode:

1. Forward mode, defined as: IN2=L, IN1=H, then OUT2=L, OUT1=H;
2. Reverse mode, defined as: IN2=H, IN1=L, then OUT2=H, OUT1=L;
3. Brake mode, defined as: IN2=H, IN1=H, then OUT2=L, OUT1=L;
4. Coast mode, defined as: IN2=L, IN1=L, at this time OUT2=Open, OUT1=Open.

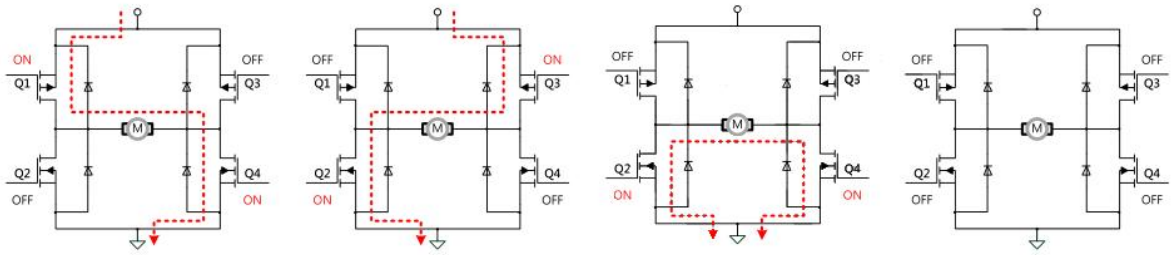


Figure 5. TMI8140-Q1 Work Modes

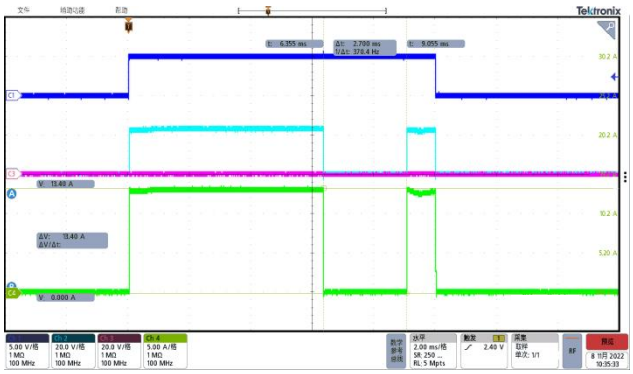
Thermal Shutdown (TSD) and Over Current Protection (OCP)

When the IC temperature exceeds 170°C (typical value), the overheating protection circuit of the built-in IC will forcibly turn off part of the driving MOS transistors to ensure the safety of customer products.

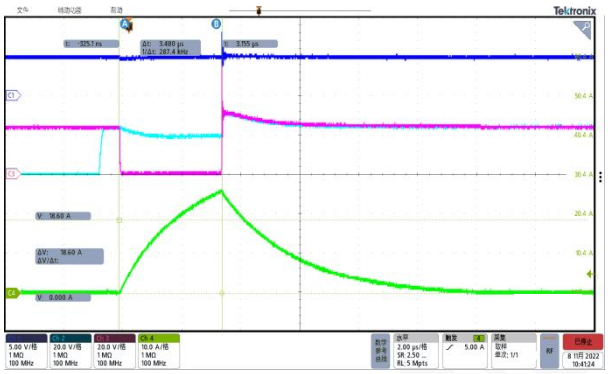
When the temperature of the IC drops to 130°C (typical), the IC will automatically resume to work quickly.

An analog current limit circuit on each MOSFET limits the peak current out of the device even in hard short circuit events. If the output current exceeds the overcurrent threshold IOCP for longer than tOCP, all MOSFETs in the H-bridge will be disabled, until VDD power is removed, the MOSFETs will be re-enabled again.

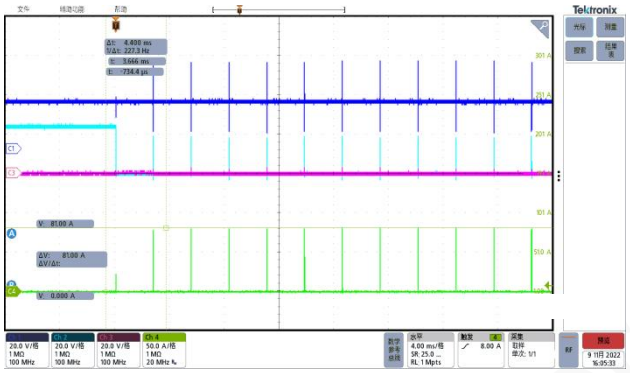
Application Curves



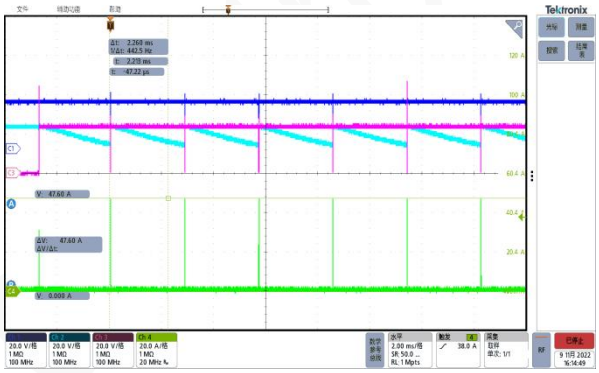
TMI8140-Q1 Over Current waveform (Iocp)



TMI8140-Q1 Over Current waveform (tocp)



TMI8140-Q1 short waveform(OUTx to GND)



TMI8140-Q1 short waveform(OUTx to VM)

Suggested PCB layout

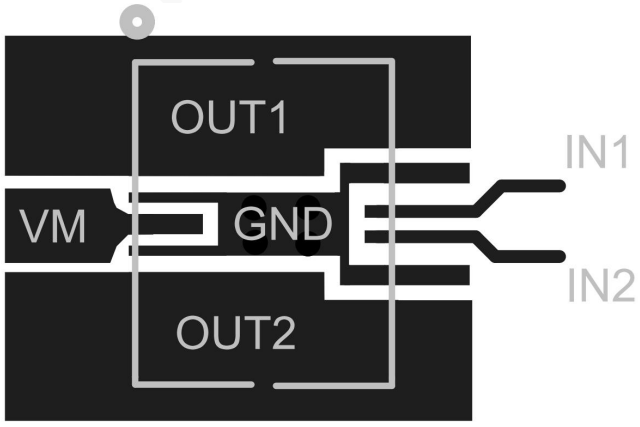


Figure 6. TMI8140-Q1 Simplified Layout Example

PCB Layout Guidelines

1. The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.
2. Small-value capacitors should be ceramic, and placed closely to device pins.
3. The high-current device outputs should use wide metal traces.
4. The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias help dissipate the I^2 x RDS(on) heat that is generated in the device.
5. The pin pad extends more than 0.4mm outwards as far as possible according to the POD size, which helps to connect the chip and pad during welding.

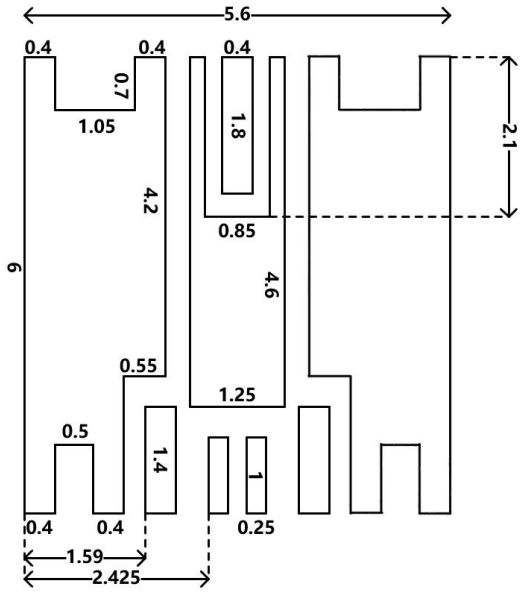
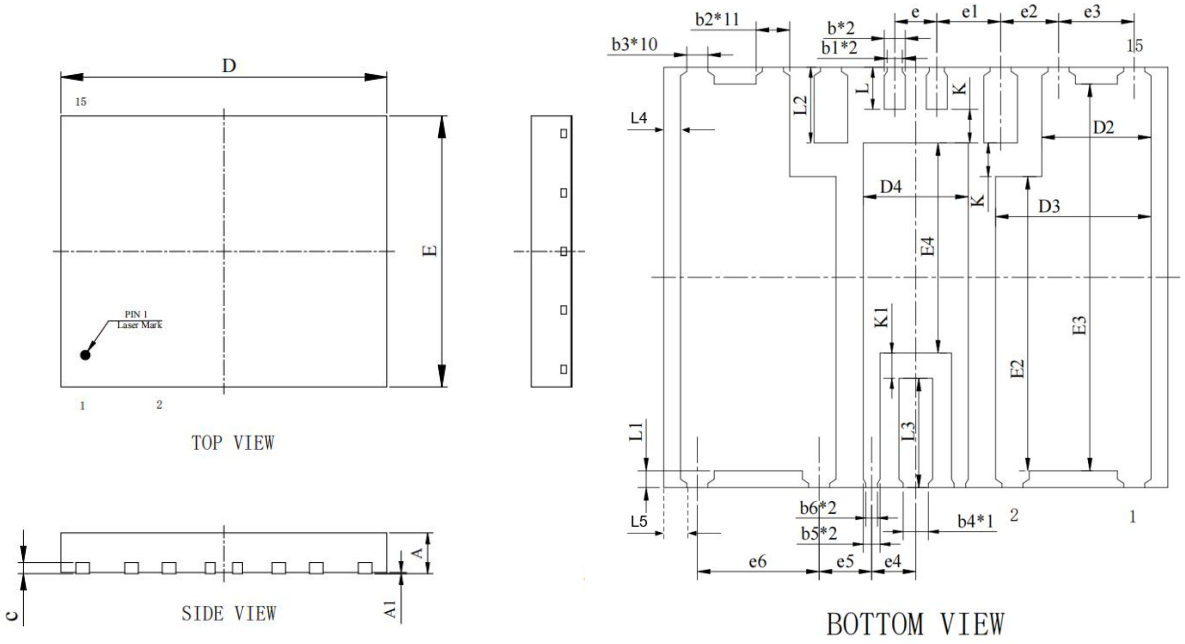


Figure 7. TMI8140-Q1 Recommended size of Pad

PACKAGE INFORMATION

DFN5*6_15

DFN5x6-15



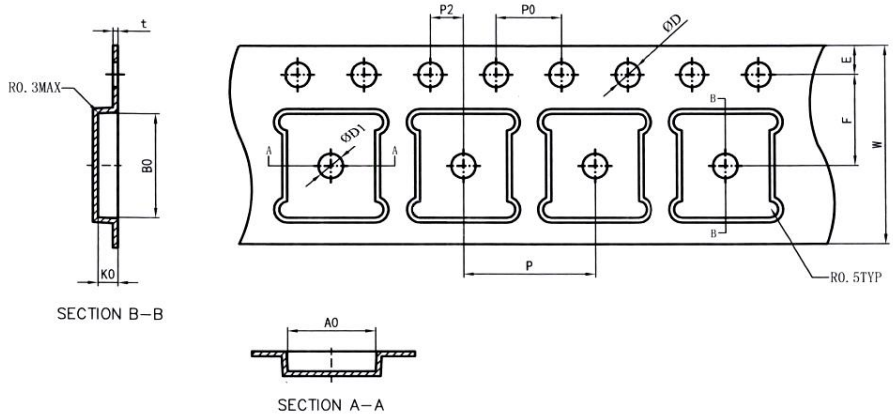
Symbol	Millimeter			Symbol	Millimeter		
	Min.	Nom.	Max.		Min.	Nom.	Max.
A	0.7	0.75	0.80	e2	0.69 BSC		
A1	0	0.02	0.05	e3	0.90 BSC		
b	0.20	0.25	0.30	e4	0.525 BSC		
b1	0.18 REF			e5	0.625 BSC		
b2	0.35	0.40	0.45	e6	1.45 BSC		
b3	0.25 REF			E	4.90	5.00	5.10
b4	0.30 REF			E2	3.40	3.50	3.60
b5	0.15	0.20	0.25	E3	4.50	4.60	4.70
b6	0.14 REF			E4	2.40	2.50	2.60
c	0.203 REF			L	0.45	0.50	0.55
D	5.90	6.00	6.10	L1	0.20 REF		
D2	1.20	1.30	1.40	L2	0.85	0.90	0.95
D3	1.75	1.85	1.95	L3	1.25	1.30	1.35
D4	1.15	1.25	1.35	L4	0.20 REF		
e	0.50 BSC			L5	0.265	0.275	0.285
e1	0.76 BSC			K	0.40 REF		
				K1	0.30 REF		

Notes:

1. Refer to JEDEC MS-012AA
2. All dimensions are in millimeter

TAPE AND REEL INFORMATION

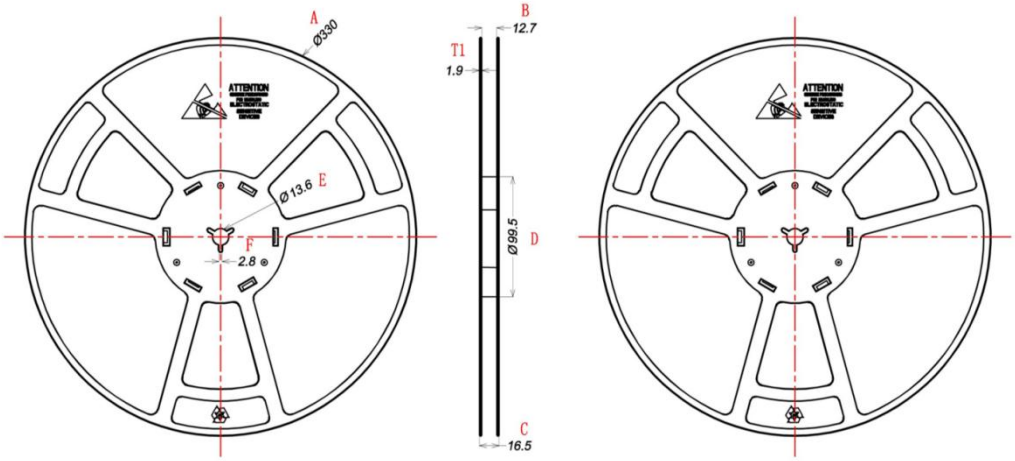
TAPE DIMENSIONS: DFN5*6-15



Unit: mm

E	F	P2	D	D1	P0	P0
1.7±0.10	5.50±0.05	2.00±0.05	$1.50\,^{+0.10}_{0}$	1.50MIN2	4.00±0.10	40.0±0.10
W	**P**	**A0**	**BO**	**K0**	**t**	
$12.0\,^{+0.20}_{-0.10}$	8.00±0.10	5.30±0.10	6.30±0.10	1.20±0.10	0.30±0.05	

REEL DIMENSIONS: DFN5*6-15



Unit: mm

A	B	C	D	E	F	T1
Ø 330±1	**12.7±0.5**	**16.5±0.3**	**Ø 99.5±0.5**	**Ø 13.6±0.2**	**2.8±0.2**	**1.9±0.2**

Note:

1) All Dimensions are in Millimeter
2) Quantity of Units per Reel is 5000
3) MSL level is level 3.

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