SGM8261-2
High-Performance, Bipolar-Input, Ultra Low Noise Operational Amplifier

GENERAL DESCRIPTION

The SGM8261-2 (dual) bipolar-input operational amplifier achieves very low noise density with an ultra low distortion of 0.00002% at 1kHz. The SGM8261-2 offers rail-to-rail output swing to within 600mV with a 2kΩ load, which increases headroom and maximizes dynamic range. The device also has a high output drive capability of ±60mA.

The device operates over a very wide supply range of 4.5V to 36V or ±2.25V to ±18V, on only 3.6mA of supply current per amplifier. The SGM8261-2 operational amplifier is unity-gain stable and provides excellent dynamic behavior over a wide range of load conditions.

The SGM8261-2 features completely independent circuitry for lowest crosstalk and freedom from interactions between channels, even when overdriven or overloaded.

The SGM8261-2 is available in Green SOIC-8, MSOP-8 and TDFN-3×3-8BL packages. It is specified from -40℃ to +85℃.

FEATURES

- **Superior Sound Quality**
- **Low Offset Voltage: ±50μV (TYP)**
- **Ultra Low Noise: 1.6nV/$\sqrt{Hz}$ at 1kHz**
- **Ultra Low Distortion: 0.00002% at 1kHz**
- **High Slew Rate: 16V/μs**
- **Gain-Bandwidth Product: 20MHz (G = +1)**
- **High Open-Loop Gain: 130dB**
- **Unity-Gain Stable**
- **Low Quiescent Current: 3.6mA/Amplifier**
- **Rail-to-Rail Output**
- **Support Single or Dual Power Supplies: 4.5V to 36V or ±2.25V to ±18V**
- **-40℃ to +85℃ Operating Temperature Range**
- **Available in Green SOIC-8, MSOP-8 and TDFN-3×3-8BL Packages**

APPLICATIONS

Professional Audio Equipment
Analog and Digital Mixing Consoles
High-End A/V Receivers

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM8261-2	SOIC-8	-40℃ to +85℃	SGM8261-2YS8G/TR	SGM 82612YS8 XXXXX	Tape and Reel, 2500
	MSOP-8	-40℃ to +85℃	SGM8261-2YMS8G/TR	SGM82612 YMS8 XXXXX	Tape and Reel, 4000
	TDFN-3×3-8BL	-40℃ to +85℃	SGM8261-2YTDD8G/TR	SGM 82612DD XXXXX	Tape and Reel, 4000

NOTE: **XXXXX** = Date Code and Vendor Code.
Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ to $-V_S$ 40V
Input Voltage Range ..... $(-V_S)$ - 0.3V to $(+V_S)$ + 0.3V
Input Current (All pins except power-supply pins)..... ±10mA
Output Short-Circuit Current ..... ±100mA
Junction Temperature ..... 150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... 260℃

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

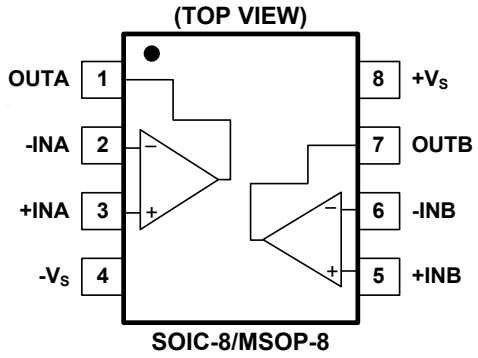
ESD SENSITIVITY CAUTION

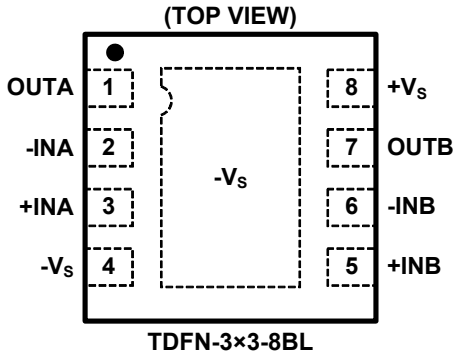
This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

PIN CONFIGURATIONS





NOTE:
For TDFN-3×3-8BL package, connect thermal die pad to $-V_S$. Soldering the thermal pad improves heat dissipation and provides specified performance.

ELECTRICAL CHARACTERISTICS

(At T_A = +25℃, V_S = 4.5V to 36V or V_S = ±2.25V to ±18V, R_L = 2kΩ, V_{CM} = V_{OUT} = V_S/2, unless otherwise noted.)

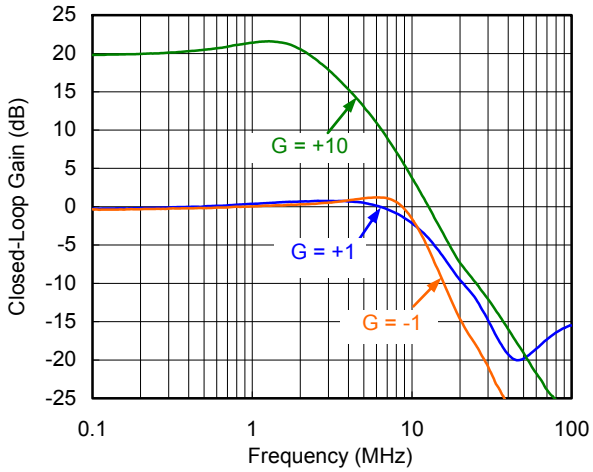
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
Input Offset Voltage (V_{OS})	V_S = ±15V		±50		μV
Input Offset Current (I_{OS})	V_{CM} = 0V		±20		nA
Input Bias Current (I_B)	V_{CM} = 0V		±60		nA
Input Common Mode Voltage Range (V_{CM})		($-V_S$) + 2		($+V_S$) - 2	V
Common Mode Rejection Ratio (CMRR)	($-V_S$) + 2V ≤ V_{CM} ≤ ($+V_S$) - 2V		120		dB
Open-Loop Voltage Gain (A_{OL})	($-V_S$) + 0.2V ≤ V_O ≤ ($+V_S$) - 0.2V, R_L = 10kΩ		130		dB
	($-V_S$) + 0.6V ≤ V_O ≤ ($+V_S$) - 0.6V, R_L = 2kΩ		120		
Input Offset Voltage Drift ($\Delta V_{OS}/\Delta_T$)			1		μV/℃
OUTPUT CHARACTERISTICS					
Output Voltage Swing from Rail	R_L = 10kΩ		±0.2		V
	R_L = 2kΩ		±0.6		
Output Short-Circuit Current (I_{SC})			±60		mA
AUDIO PERFORMANCE (G = +1, V_O = $3V_{RMS}$)					
Total Harmonic Distortion + Noise (THD + N)	G = +1, V_O = $3V_{RMS}$, f = 1kHz		0.00002		%
			-134		dB
Inter-modulation Distortion (IMD)	SMPTE/DIN Two-Tone, 4:1 (60Hz and 7kHz)		0.000015		%
			-136		dB
	DIM 30 (3kHz square wave and 15kHz sine wave)		0.000032		%
			-130		dB
	CCIF Twin-Tone (19kHz and 20kHz)		0.00013		%
			-118		dB
FREQUENCY RESPONSE					
Gain-Bandwidth Product (GBP)	G = 100		60		MHz
	G = 1		20		
Slew Rate (SR)	G = -1		16		V/μs
Full Power Bandwidth (1)	V_O = $1V_{P-P}$		2		MHz
Overload Recovery Time	G = -10		500		ns
Channel Separation (Dual)	f = 1kHz		-140		dB
NOISE PERFORMANCE					
Input Voltage Noise	f = 20Hz to 20kHz		1.7		μV_{P-P}
Input Voltage Noise Density (e_n)	f = 10Hz		2.3		$nV/\sqrt{Hz}$
	f = 100Hz		1.8		
	f = 1kHz		1.6		
Input Current Noise Density (i_n)	f = 1kHz		6		$pA/\sqrt{Hz}$
POWER SUPPLY					
Supply Voltage (V_S)		±2.25		±18	V
Quiescent Current/Amplifier (I_Q)	I_{OUT} = 0A		3.6		mA
Power Supply Rejection Ratio (PSRR)	V_S = ±2.25V to ±18V		0.1		μV/V

NOTE:
1. Full Power Bandwidth = SR/(2π × V_P), where SR = slew rate.

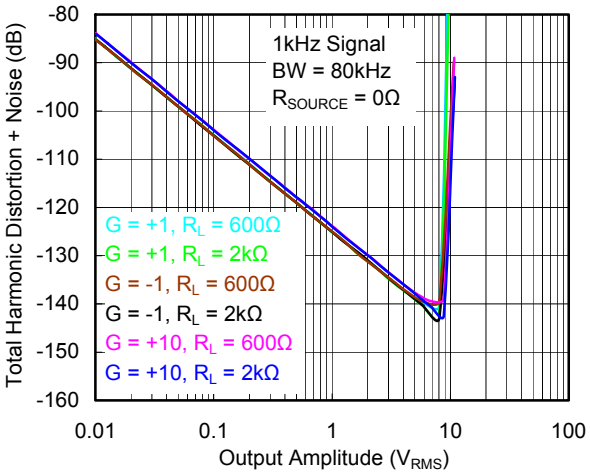
TYPICAL PERFORMANCE CHARACTERISTICS

(At T_A = +25℃, V_S = ±15 V, and R_L = 2kΩ, unless otherwise noted.)

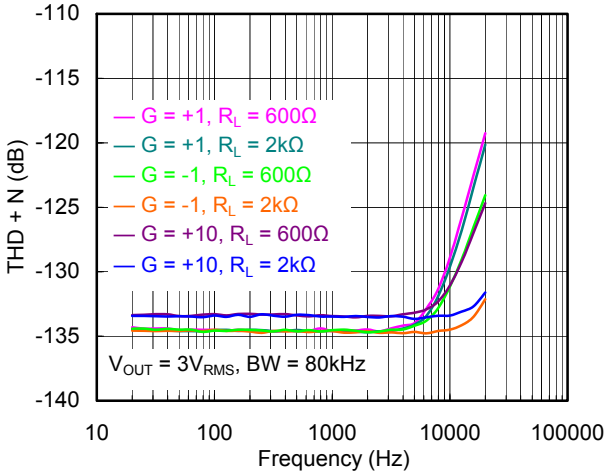
Closed-Loop Gain vs. Frequency



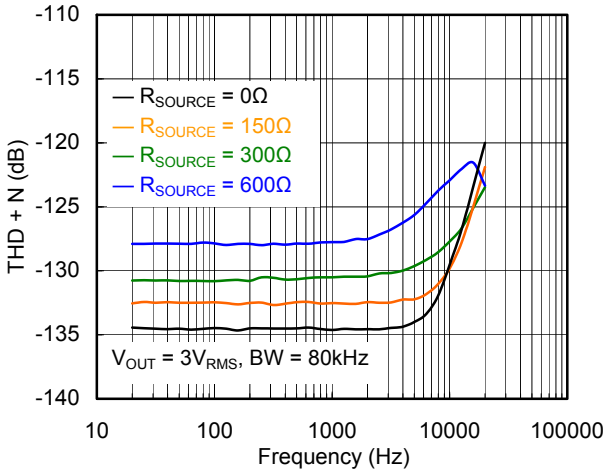
THD+N Ratio vs. Output Amplitude



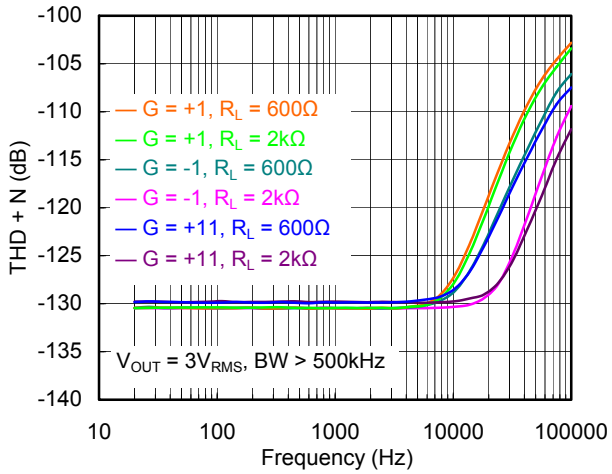
THD+N vs. Frequency



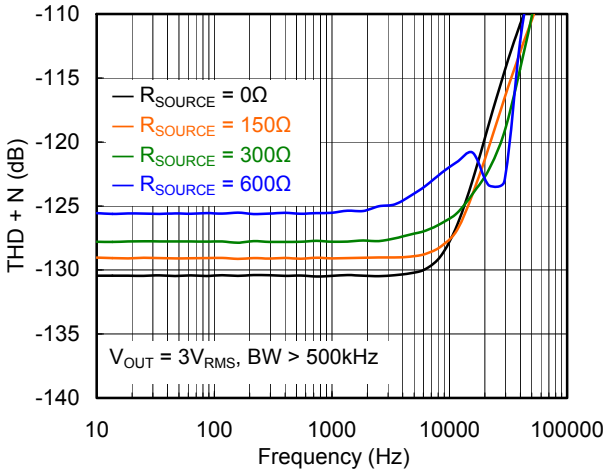
THD+N vs. Frequency



THD+N vs. Frequency

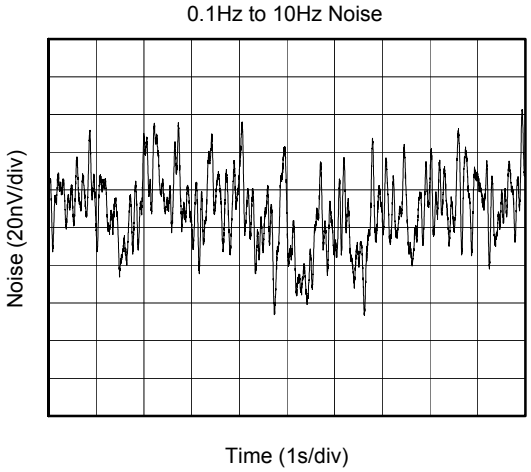


THD+N vs. Frequency



TYPICAL PERFORMANCE CHARACTERISTICS

(At T_A = +25℃, V_S = ±15 V, and R_L = 2kΩ, unless otherwise noted.)



APPLICATION INFORMATION

The SGM8261-2 is unity-gain stable, precision operational amplifier with very low noise; the device is also free from output phase reversal. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device power-supply pins. In most cases, 0.1μF capacitors are adequate.

Operating Voltage

The SGM8261-2 operational amplifier operates from 4.5V to 36V or ±2.25V to ±18V supplies while maintaining excellent performance. The SGM8261-2 can operate with as low as +4.5V between the supplies and with up to +36V between the supplies. However, some applications do not require equal positive and negative output voltage swing. With the SGM8261-2, power-supply voltages do not need to be equal. For example, the positive supply could be set to +25V with the negative supply at -5V. In all cases, the input common mode voltage must be maintained within the specified range. In addition, key parameters are assured over the specified temperature range of T_A = -40℃ to +85℃.

Input Protection

The input terminal of the SGM8261-2 is protected from excessive differential voltage with back-to-back diodes, as Figure 1 illustrates. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or G = +1 circuits, fast ramping input signals can forward bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward bias condition, the input signal current must be limited to 10mA or less. If the input signal current is not inherently limited, an input series resistor (R_I) and/or a feedback resistor (R_F) can be used to limit the signal input current. This input series resistor degrades the low-noise performance of the SGM8261-2 and is examined in the following Noise Performance section. Figure 1 shows an example configuration when both current-limiting input and feedback resistors are used.

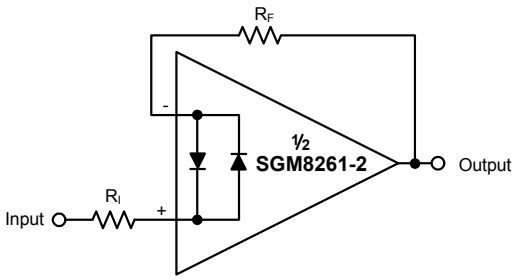


Figure 1. Pulsed Operation

APPLICATION INFORMATION

Noise Performance

Equation 1 shows the total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions referred to Figure 2).

The SGM8261-2 (GBP = 20MHz, G = +1) is shown with total circuit noise calculated. The operational amplifier itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise operational amplifier for a given application depends on the source impedance. For low source impedance, current noise is negligible, and voltage noise generally dominates. The low voltage noise of the SGM8261-2 operational amplifier makes them a good choice for use in applications where the source impedance is less than 1kΩ.

The equation shows the calculation of the total circuit noise, with these parameters:

$$E_O^2 = e_n^2 + (i_n R_S)^2 + 4kTR_S \quad (1)$$

- e_n = Voltage noise
- i_n = Current noise
- R_S = Source impedance
- k = Boltzmann's constant = 1.38×10^{-23}J/K
- T = Temperature in degrees Kelvin (K)

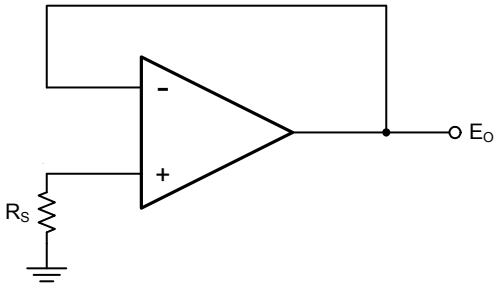


Figure 2. Unity-Gain Buffer Configuration

Basic Noise Calculations

Design of low-noise operational amplifier circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the operational amplifier, and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all noise components.

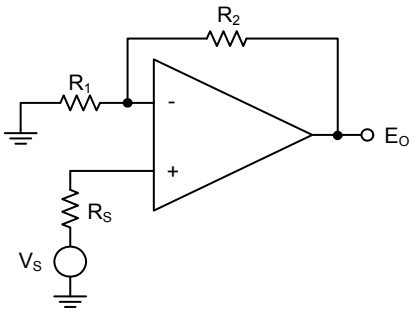
The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. The source impedance is usually fixed; consequently, select the operational amplifier and the feedback resistors to minimize the respective contributions to the total noise.

Figure 3 illustrates both inverting and non-inverting operational amplifier circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise.

The current noise of the operational amplifier reacts with the feedback resistors to create additional noise components. The feedback resistor values can generally be chosen to make these noise sources negligible. The equations for total noise are shown for both configurations.

APPLICATION INFORMATION

Noise in Non-inverting Gain Configuration



Noise at the output:

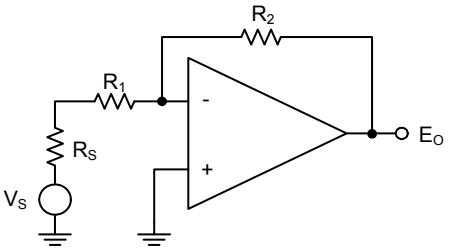
$$E_O^2 = \left[1+\frac{R_2}{R_1}\right]^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2 + (i_n R_S)^2 \left[1+\frac{R_2}{R_1}\right]^2$$

Where $e_S = \sqrt{4kTR_S} \times \left[1+\frac{R_2}{R_1}\right]$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \times \left[\frac{R_2}{R_1}\right]$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left[1+\frac{R_2}{R_1+R_S}\right]^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2$$

Where $e_S = \sqrt{4kTR_S} \times \left[\frac{R_2}{R_1+R_S}\right]$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \times \left[\frac{R_2}{R_1+R_S}\right]$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

NOTE: For the SGM8261-2 operational amplifier at 1kHz, e_n = 1.6nV/$\sqrt{Hz}$ and i_n = 6pA/$\sqrt{Hz}$.

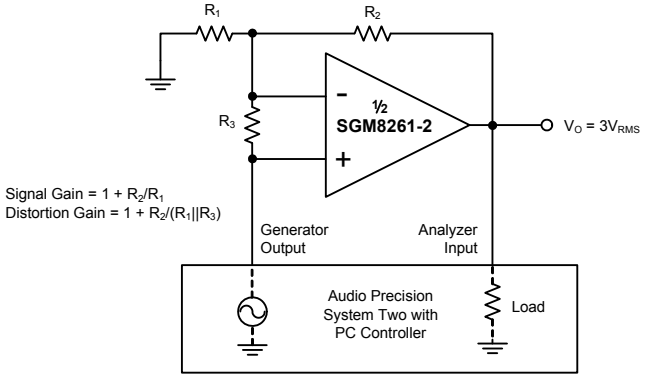
Figure 3. Noise Calculation in Gain Configurations

Total Harmonic Distortion Measurements

The SGM8261-2 operational amplifier has excellent distortion characteristics. THD+Noise is below 0.00015% (G = +1, V_O = $3V_{RMS}$, BW = 80kHz) throughout the audio frequency range, 20Hz to 20kHz, with a 2kΩ load.

The distortion produced by SGM8261-2 operational amplifier is below the measurement limit of many commercially available distortion analyzers. However, a special test circuit (such as Figure 4 shows) can be used to extend the measurement capabilities.

Operational amplifier distortion can be considered an internal error source that can be referred to the input. Figure 4 shows a circuit that causes the operational amplifier distortion to be 101 times (or approximately 40dB) greater than that normally produced by the operational amplifier. The addition of R_3 to the otherwise standard non-inverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101, thus extending the resolution by 101. Note that the input signal and load applied to the operational amplifier are the same as with conventional feedback without R_3. The value of R_3 should be kept small to minimize its effect on the distortion measurements.



SIG. GAIN	DIST. GAIN	R_1	R_2	R_3
1	101	∞	1kΩ	10Ω
-1	101	4.99kΩ	4.99kΩ	49.9Ω
+10	110	549Ω	4.99kΩ	49.9Ω

Figure 4. Distortion Test Circuit

APPLICATION INFORMATION

Validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with an audio precision system two distortion/noise analyzer, which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

Capacitive Loads

The dynamic characteristics of the SGM8261-2 have been optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (R_S equal to 50Ω, for example) in series with the output.

Power Dissipation

SGM8261-2 operational amplifier is capable of driving 2kΩ loads with a power-supply voltage up to ±18V. Internal power dissipation increases when operating at high supply voltages. Copper leadframe construction used in the SGM8261-2 operational amplifier improves heat dissipation compared to conventional materials. Circuit board layout can also help minimize junction temperature rise. Wide copper traces help dissipate the heat by acting as an additional heat sink. Temperature rise can be further minimized by soldering the devices to the circuit board rather than using a socket.

Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. Figure 5 illustrates the ESD circuits contained in the SGM8261-2 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation. An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device internal to the SGM8261-2 triggers when a fast ESD voltage pulse is impressed across the supply pins. Once triggered, it quickly activates and clamps the ESD pulse to a safe voltage level.

When the operational amplifier connects into a circuit such as the one Figure 5 shows, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

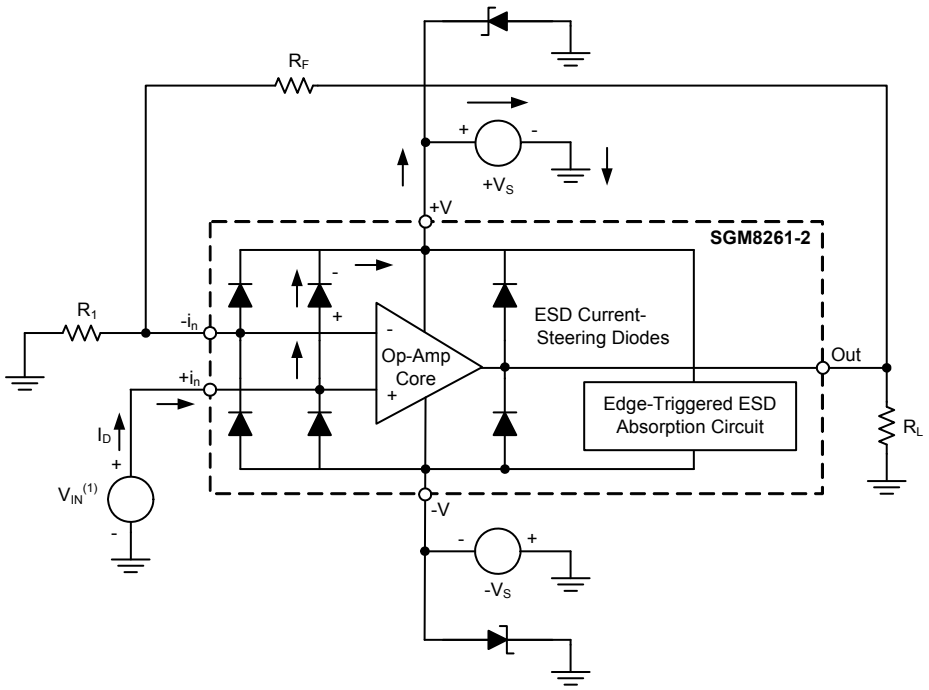
Figure 5 depicts a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage ($+V_S$) by 500mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the datasheet specifications recommend that applications limit the input current to 10mA.

APPLICATION INFORMATION

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings. In extreme but rare cases, the absorption device triggers on while $+V_S$ and $-V_S$ are applied. If this event happens, a direct current path is established between the $+V_S$ and $-V_S$ supplies. The power dissipation of the absorption device is quickly exceeded, and the extreme internal heating destroys the operational amplifier.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ and/or $-V_S$ are at 0V. Again, it depends on the supply characteristic while at 0V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source via the current steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is an uncertainty about the ability of the supply to absorb this current, external Zener diodes may be added to the supply pins as shown in Figure 5. The Zener voltage must be selected such that the diode does not turn on during normal operation. However, its Zener voltage should be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.



NOTE: 1. $V_{IN} = (+V_S) + 500mV$.

Figure 5. Equivalent Internal ESD Circuitry and Its Relation to a Typical Circuit Application

APPLICATION CIRCUIT

Figure 6 shows how to use the SGM8261-2 as an amplifier for professional audio headphones. The circuit shows the left side stereo channel. An identical circuit is used to drive the right side stereo channel.

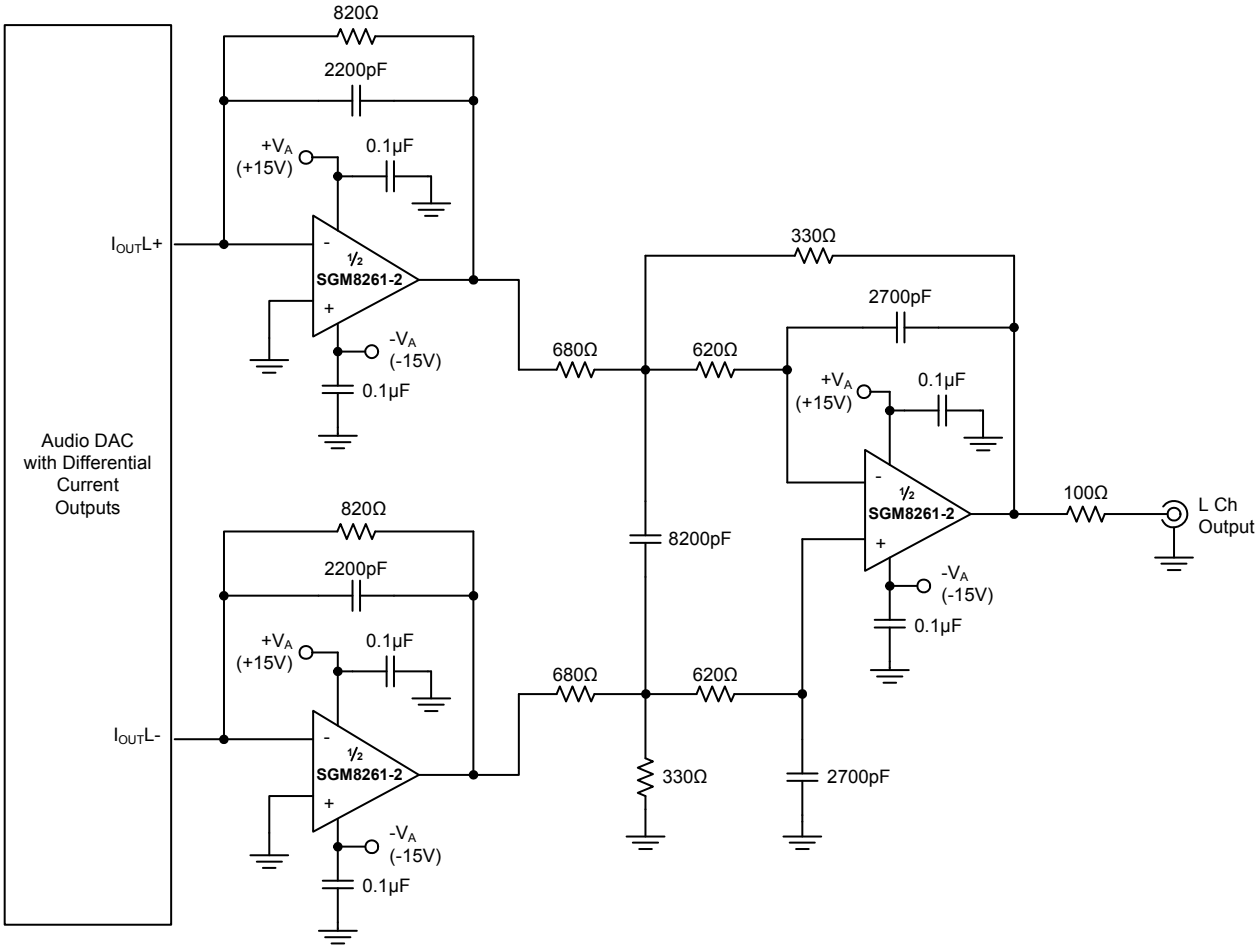
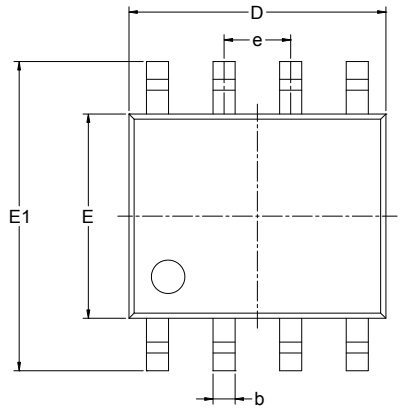
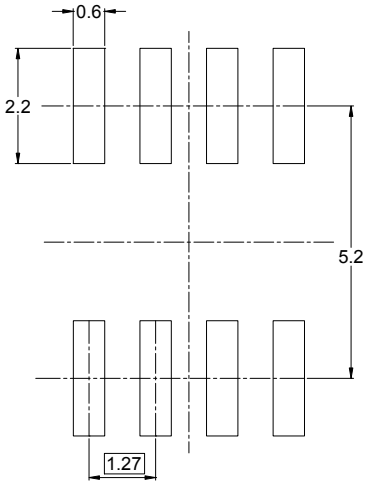


Figure 6. Audio DAC Post Filter (I/V Converter and Low-Pass Filter)

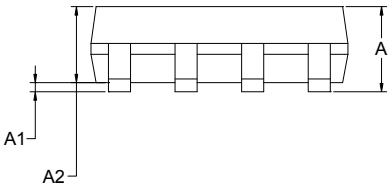
PACKAGE OUTLINE DIMENSIONS

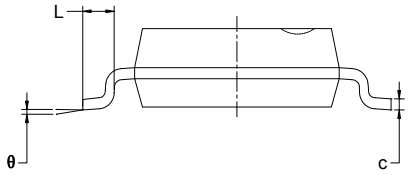
SOIC-8





RECOMMENDED LAND PATTERN (Unit: mm)

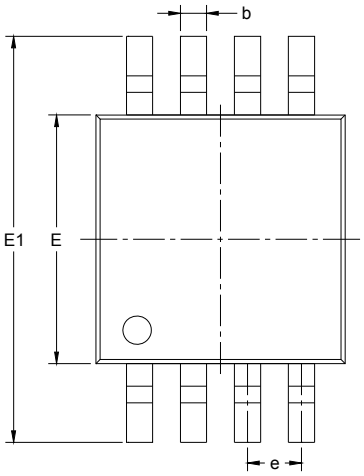


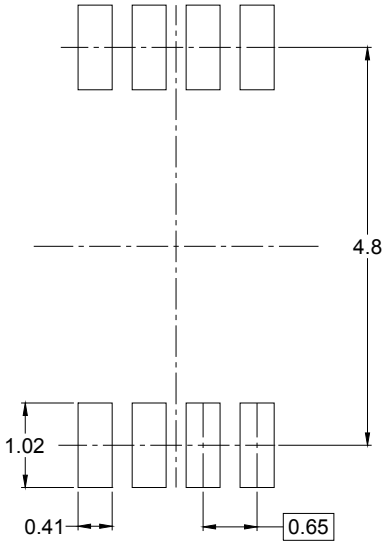


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

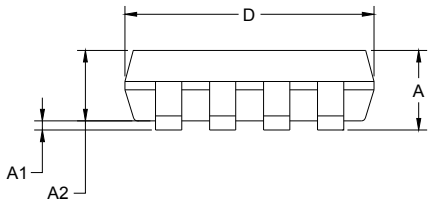
PACKAGE OUTLINE DIMENSIONS

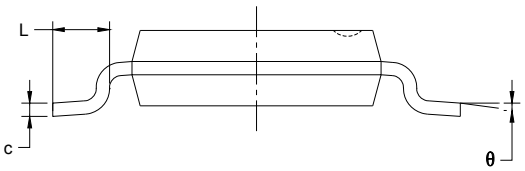
MSOP-8





RECOMMENDED LAND PATTERN (Unit: mm)

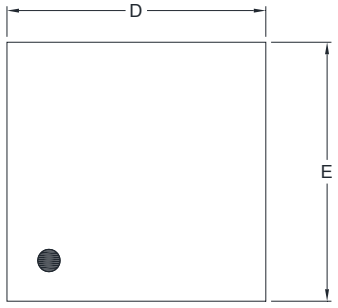




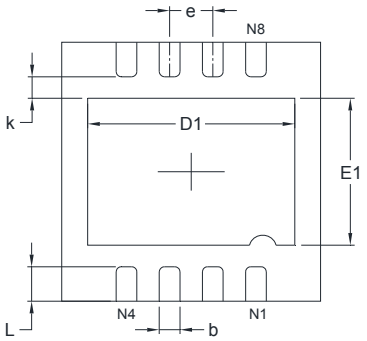
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
e	0.650 BSC		0.026 BSC	
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

PACKAGE OUTLINE DIMENSIONS

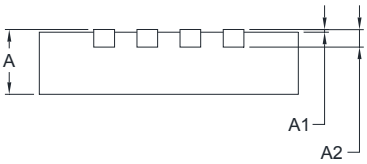
TDFN-3×3-8BL



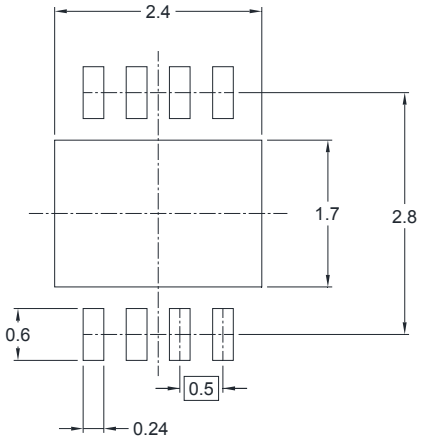
TOP VIEW



BOTTOM VIEW



SIDE VIEW

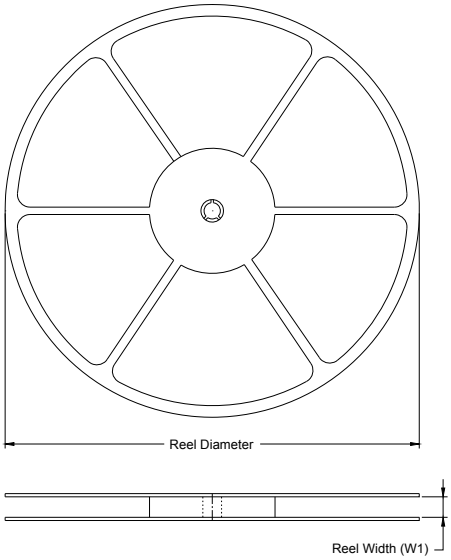


RECOMMENDED LAND PATTERN (Unit: mm)

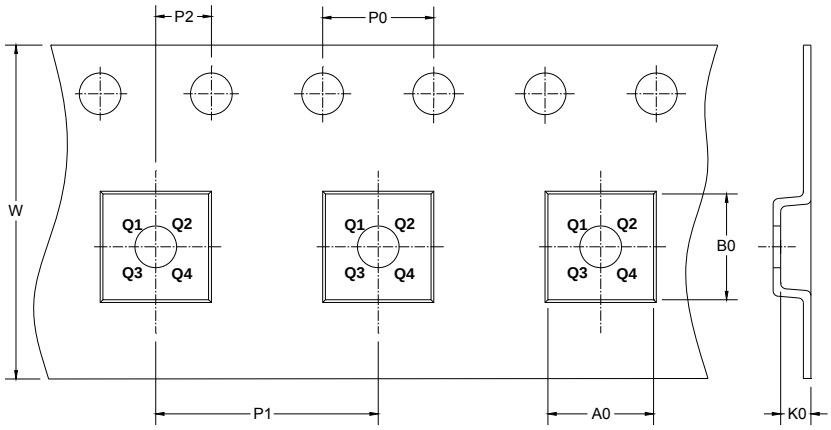
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	2.300	2.500	0.091	0.098
E	2.900	3.100	0.114	0.122
E1	1.600	1.800	0.063	0.071
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

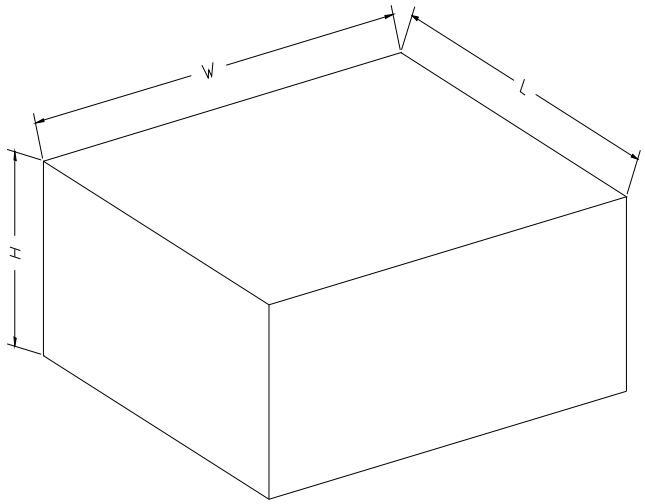
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8	13″	12.4	6.4	5.4	2.1	4.0	8.0	2.0	12.0	Q1
MSOP-8	13″	12.4	5.2	3.3	1.5	4.0	8.0	2.0	12.0	Q1
TDFN-3×3-8BL	13″	12.4	3.35	3.35	1.13	4.00	8.00	2.00	12.00	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002