SGM821
Nano-Power System Timer with Watchdog Function

GENERAL DESCRIPTION

The SGM821 is an ultra-low power and programmable watchdog timer, designed for system wake-up in duty-cycled and battery-powered applications, such as those in IoT. A μC is usually needed in these applications, so it is desirable to keep the μC in low power mode most of the time to maximize current savings, and only wake up in a specific time interval to collect data or service an interrupt. Although the internal timer of the μC can be used, it cannot meet the requirement of ultra-low power system due to its microamps current consumption.

The SGM821 with programmable interrupt timer consumes only 60nA (TYP) system current. Accordingly, it allows the μC to be placed in sleeping mode with the internal timer off which consumes much lower power consumption, and returns to active mode only upon an interrupt by the SGM821. So it is suitable for wireless sensor applications or other applications with smaller batteries.

The time interval of SGM821 can be programmed by an external resistance. The external resistance ranges from 500Ω to170kΩ and it provides a corresponding time interval from 100ms to 7200s. Due to the high accuracy of internal oscillator and resistance detecting precision, it is ideal for the use with tight tolerance systems.

The SGM821 is available in Green SOT-23-6 and TDFN-2×2-6AL packages. It operates over an ambient temperature range of -40℃ to +105℃.

FEATURES

- **Supply Voltage Range: 1.8V to 5.5V**
- **Current Consumption at 2.5V: 60nA (TYP)**
- **Selectable Time Intervals: 100ms to 7200s**
- **Resistor Programmable Time Interval**
- **Watchdog Functionality**
- **Manual Reset Input**
- **Available in Green SOT-23-6 and TDFN-2×2-6AL Packages**

APPLICATIONS

Battery-Powered Systems
Internet of Things (IoT)
Intruder Detection
Tamper Detection
Home Automation Sensors
Thermostats
Consumer Electronics
Remote Sensors
White Goods

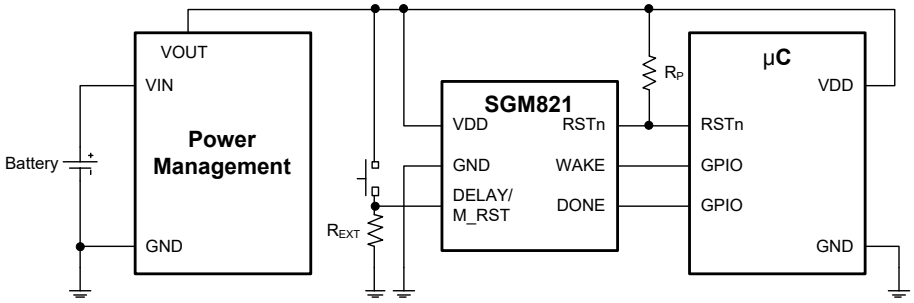


Figure 1. Simplified Application Schematic

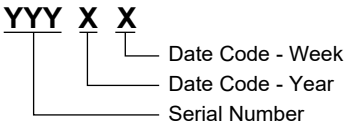
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM821	SOT-23-6	-40℃ to +105℃	SGM821GN6G/TR	RCEXX	Tape&Reel,3000
	TDFN-2×2-6AL	-40℃ to +105℃	SGM821GTDI6G/TR	RCF XXXX	Tape&Reel,3000

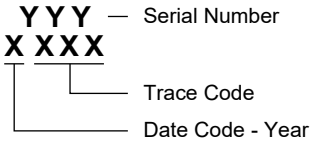
MARKING INFORMATION

NOTE: XX = Date Code. XXXX = Date Code and Trace Code.

SOT-23-6



TDFN-2×2-6AL



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VDD to GND)..... -0.3V to 6V
Input Voltage at Any Pin (1) .....-0.3V to VDD + 0.3V
Input Current on Any Pin.....±5mA
Package Thermal Resistance
SOT-23-6, θ_{JA} ..... ℃/W
TDFN-2×2-6AL, θ_{JA}..... ℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃

RECOMMENDED OPERATING CONDITIONS

Supply Voltage (VDD to GND).....1.8V to 5.5V
Operating Ambient Temperature Range.....-40℃ to +105℃

NOTE:
1. The voltage between any two pins should not exceed 6V.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

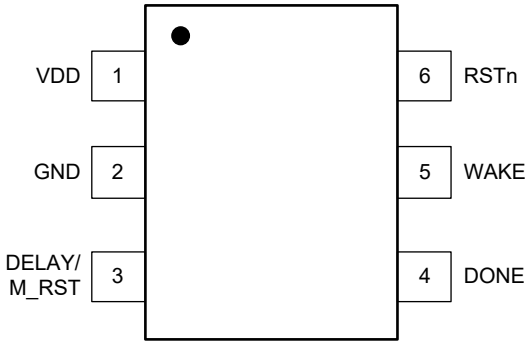
This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

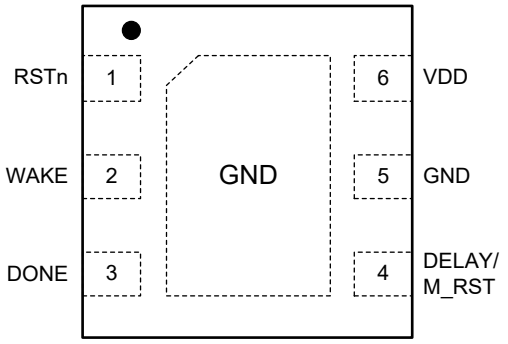
PIN CONFIGURATION

SGM821 (TOP VIEW)



SOT-23-6

SGM821 (TOP VIEW)



TDFN-2×2-6AL

PIN DESCRIPTION

PIN		NAME	TYPE	FUNCTION
SOT-23-6	TDFN-2×2-6AL			
1	6	VDD	P	Supply Voltage.
2	5	GND	G	Ground.
3	4	DELAY/ M_RST	I	One-Time Time Interval Set and Manual Reset. Resistance connected between this pin and GND is used to select the time interval. The value of the resistor is converted once after POR allowing a range of 500Ω to 170kΩ. This pin is also used as an input manual reset pin, and pulling this pin up to VDD will issue an RSTn.
4	3	DONE	I	Logic Watchdog Input. Digital signal driven by the μC to indicate successful processing of the WAKE signal.
5	2	WAKE	O	Watchdog output (Push-Pull). A Digital pulsed signal is generated to wake up the μC at the end of the programmed time interval.
6	1	RSTn	O	Reset Output (Open-Drain Output). Digital signal to RESET the μC. A pull-up resistance is required.
—	Exposed Pad	GND	—	Connect the thermal pad to a large-area ground plane. The exposed pad is internally connected to GND.

NOTE: G = Ground, P = Power, O = Output, I = Input.

ELECTRICAL CHARACTERISTICS

(VDD - GND = 2.5V, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply						
Supply Current (1)	I_{DD}	Operation mode		60		nA
		Digital conversion of external resistance (R_{EXT})		200		μA
Timer						
Time Interval Period	t_{IP}	Minimum time interval		100		ms
		Maximum time interval		7200		s
DONE Pulse Width	t_{DONE}			200		ns
RSTn Pulse Width	t_{RSTn}			320		ms
WAKE Pulse Width	t_{WAKE}			20		ms
Time to Convert R_{EXT}	t_{REXT}			100		ms
Digital Logic Levels						
Logic High Threshold DONE Pin	V_{IH}			0.8 × V_{CC}		V
Logic Low Threshold DONE Pin	V_{IL}			0.2 × V_{CC}		V
Logic Output High Level WAKE Pin	V_{OH}	I_{OUT} = 100μA		V_{CC} - 0.3		V
		I_{OUT} = 1mA		V_{CC} - 0.7		
Logic Output Low Level WAKE Pin	V_{OL}	I_{OUT} = -100μA		0.3		V
		I_{OUT} = -1mA		0.7		
RSTn Logic Output Low Level	V_{OL_RSTn}	I_{OL} = -1mA		0.3		V
RSTn High Level Output Current	I_{OH_RSTn}	V_{OH_RSTn} = VDD		10		nA
Logic High Threshold DELAY/M_RST Pin	V_{IHM_RST}			1.5		V

NOTES:

1. The supply current excludes load and pull-up resistor current. Input pins are at GND or VDD.
2. The accuracy for time interval settings below 1 second is ±100ms.
3. Operational life time test procedure equivalent to 10 years.

TIMING REQUIREMENTS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time RSTn	t_{RRSTn}	Capacitive load 50pF, $R_{PULL-UP}$ 100kΩ		11		μs
Fall Time RSTn	t_{FRSTn}	Capacitive load 50pF, $R_{PULL-UP}$ 100kΩ		50		ns
Rise Time WAKE	t_{RWAKE}	Capacitive load 50pF		50		ns
Fall Time WAKE	t_{FWAKE}	Capacitive load 50pF		50		ns
DONE to RSTn or WAKE to DONE Delay	t_{DDONE}	Minimum delay (1)		100		ns
		Maximum delay (1)		t_{IP} - 20ms		ms
Debounce Manual Reset	t_{DB}			20		ms
Valid Manual Reset	t_{M_RST}			20		ms

NOTE: 1. In case of RSTn from its falling edge or in case of WAKE from its rising edge.

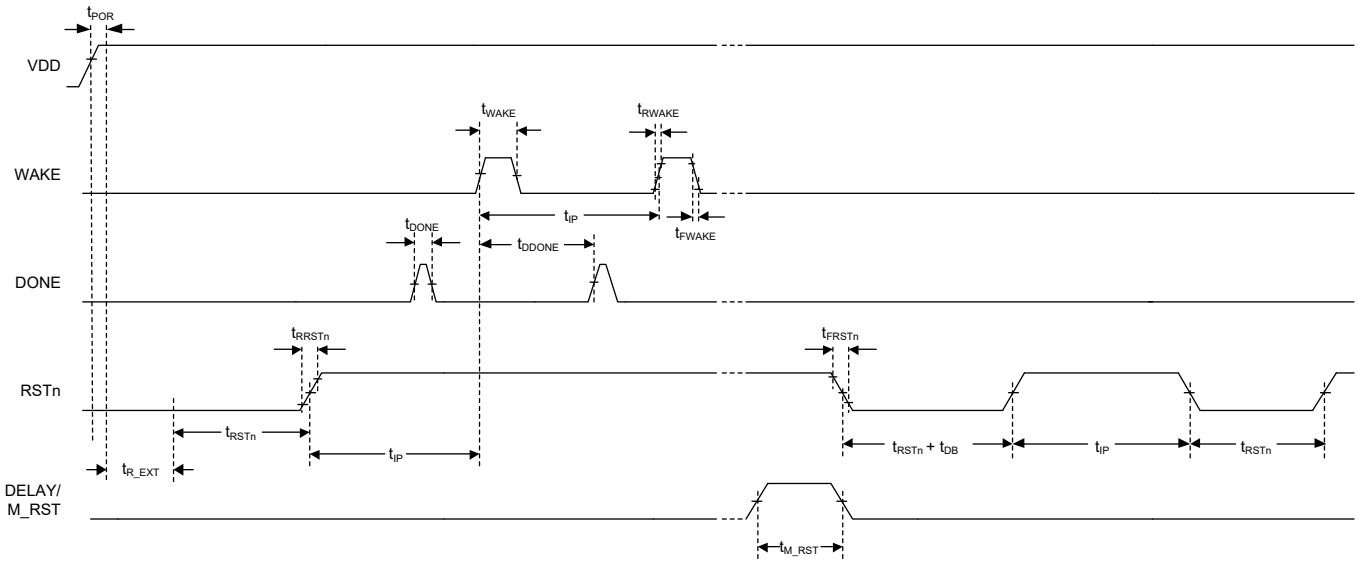


Figure 2. Timing Diagram

FUNCTIONAL BLOCK DIAGRAM

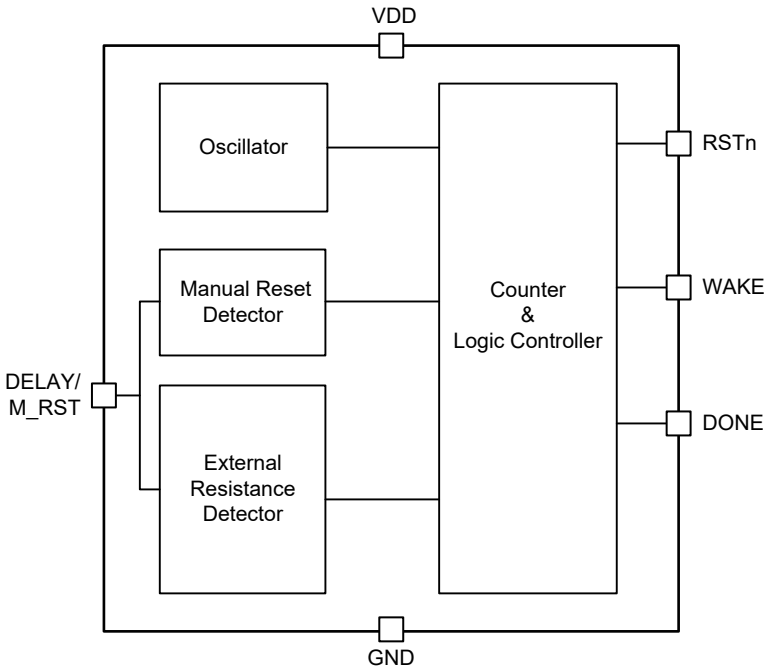


Figure 3. Functional Block Diagram

DETAILED DESCRIPTION

The SGM821 is a system wake-up watchdog timer designed for low-power applications. The SGM821 can be used in interrupt-driven applications and provides selectable timing from 100ms to 7200s.

The DONE, WAKE and RSTn signals are used to implement the watchdog function. The SGM821 is programmed to issue a periodic WAKE pulse to a μC which is in sleeping or standby mode. After receiving the WAKE pulse, the μC must issue a DONE signal to the SGM821 at least 20ms before the rising edge of the next WAKE pulse. If the DONE signal is not asserted, the SGM821 asserts the RSTn signal to reset the μC. A manual reset function is realized by momentarily pulling the DELAY/M_RST pin to VDD.

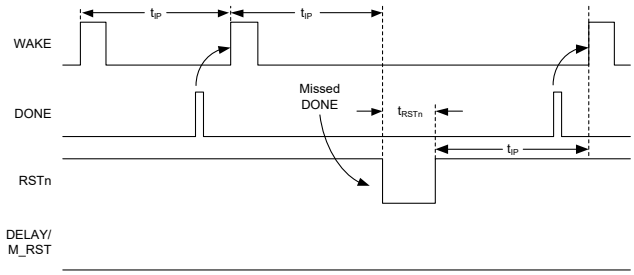


Figure 4. Watchdog

WAKE

The WAKE is an output signal, which is normally low most of the time. When the programmed time interval starts, the SGM821 will sent out a WAKE pulse if a valid DONE has been received in the previous time interval. If DONE is not recognized in the previous time interval, the RSTn will assert and WAKE pulse will not be generated. At the beginning of the first cycle or after RSTn is deasserted, WAKE will not be generated and SGM821 is waiting for a valid DONE in this new cycle. If a valid DONE is recognized, WAKE will be generated in the next time interval. Otherwise, RSTn will assert again.

DONE

The DONE is an input logic pin, and it is not allowed to be floating. The DONE is always driven by a μC to signal successful processing of the WAKE signal. The SGM821 recognizes a valid DONE signal as a low to high transition. If the DONE pulse is positive, it is recommended to set the pulse width larger than 200ns. And if two or more DONE signals are received within the one time interval, only the first DONE signal is processed. Notice that the DONE signal will not be recognized in the last 20ms of the current time interval.

If the DONE signal is received when the WAKE is still high, the WAKE will go low as soon as the DONE is recognized.

RSTn

To implement the reset interface between the SGM821 and the μC, a pull-up resistance is required. 100kΩ is recommended to minimize current consumption.

During the POR and the reading of the R_{EXT}, the RSTn signal is low. RSTn is asserted (low) for either one of the following conditions:

1. If the DELAY/M_RST pin is high for at least two consecutive cycles of the internal oscillator (approximately 20ms).

2. If the DONE is not received at least 20ms before the next WAKE rising edge (see Figure 4).

Start-Up

During start-up after POR, the SGM821 executes a one-time measurement of the external resistance attached to the DELAY/M_RST pin to determine the desired time interval for WAKE. This measurement interval is t_{R_EXT}. During this measurement, the external resistance detection block is temporarily working, so the power consumption of the chip is temporarily high. After detecting, the external resistance detection block is powered off, the power consumption goes down. A counter starts working after POR, and it is timeout after T_{REXT} (100ms, TYP) which signal the end of external resistance reading time. During the measurement, the power consumption of the chip is related to the external resistor, the smaller the resistance, the greater the power consumption.

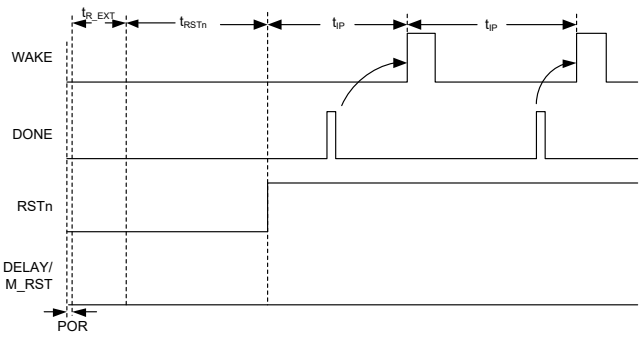


Figure 5. Start-Up

DETAILED DESCRIPTION (continued)

Normal Operating Mode

During normal operating mode, the SGM821 asserts periodic WAKE pulses in response to valid DONE pulses from the μC. If either a valid manual reset is applied (logic HIGH on DELAY/M_RST pin), or the μC does not issue a DONE pulse within the required time, the SGM821 asserts the RSTn signal to the μC and restarts its internal counters. See Figure 4 and Figure 6.

Configuring the WAKE Interval with the DELAY/M_RST Pin

The time interval between two adjacent WAKE pulses (rising edges) is selectable through an external resistor (R_{EXT}) between the DELAY/M_RST pin and ground. The value of the resistor R_{EXT} is converted one time after POR. The allowable range of R_{EXT} is 500Ω to 170kΩ. For high precise applications, at least a 1% precision resistance is recommended. See section Timer Interval Selection Using External Resistance on how to set the WAKE pulse interval using R_{EXT}. Capacitance connected to DELAY/M_RST pin is also not allowed. And it is also suggested that the traces connecting the resistance on this pin to GND be kept as short as possible to minimize parasitic capacitance. Besides, for good detection, other interfering signal should be kept far away.

The time between two adjacent RESET signals (falling edges), or between a RESET (falling edge) and a WAKE (rising edge), is given by the sum of the programmed time interval and the t_{RSTn} (reset pulse width).

Manual Reset

If DELAY/M_RST is connected to VDD, the SGM821 recognizes this as a manual reset condition. If manual reset asserts during t_{R_EXT}, the reading procedure may be aborted and restarted immediately. For the details, please contact with the manufacture. During normal operating mode after t_{R_EXT}, a pulse on the DELAY/M_RST pin is recognized as a valid manual reset only if it lasts at least 20ms (observation time is 30ms).

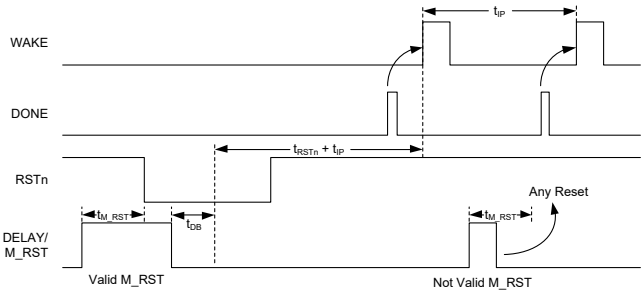


Figure 6. Manual Reset

DELAY/M_RST

A resistance in the range of 500Ω to 170kΩ needs to be connected to select a valid time interval. At the POR and during the reading of the resistance, the internal sensor and the resistor detection block are enabled. After the reading of the resistance, these analog circuits disabled, and DELAY/M_RST is only used as manual reset pin.

The manual reset detection is supported with a debounce feature which makes the SGM821 insensitive to the glitches on the DELAY/M_RST pin. When a valid manual reset signal is asserted on the DELAY/M_RST pin, the RSTn signal is asserted LOW after a delay of t_{M_RST}. RSTn remains low after a valid manual reset is asserted + t_{DB} + t_{RSTn}. Due to the asynchronous nature of the manual reset signal and its arbitrary duration, the LOW status of the RSTn signal maybe affected by an uncertainty of about ±5ms.

A valid manual reset puts all the digital output signals at their default values:

WAKE = low; RSTn = asserted low

Circuitry

The manual reset can be implemented using mechanical switches. The SGM821 offers two possible approaches according to the consideration of system power consumption. In cases that do not require the lowest power consumption, using a single-pole single-throw switch may offer a lower cost. However, for the low power system applications, a single-pole double-throw switch will provide a lower power solution.

DETAILED DESCRIPTION (continued)

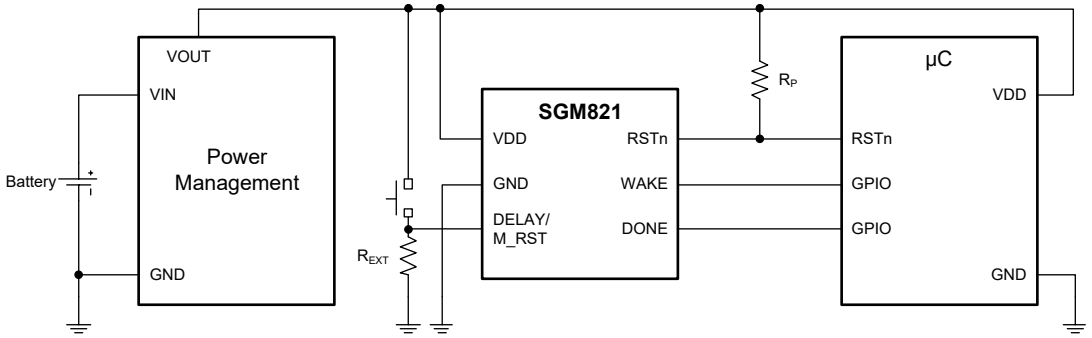


Figure 7. Manual Reset with SPST Switch

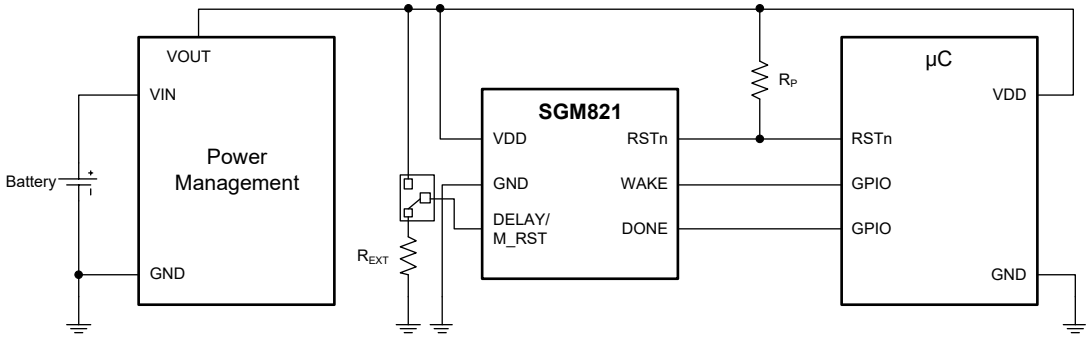


Figure 8. Manual Reset with SPDT Switch

Timer Interval Selection Using External Resistance

To set the time interval below 1 second, the external resistance R_{EXT} is selected according to Table 1.

To set the time interval over 1 second, the external resistance R_{EXT} is selected according to Equation 1.

$$R_{EXT} = 5.2 \times T^{0.393} \quad (1)$$

where:
T is the desired time interval in seconds,
R_{EXT} is the resistance value to use in kΩ.

Table 1. First 9 Time Intervals

t_{IP} (ms)	Resistance (Ω)
100	500
200	1000
300	1500
400	2000
500	2500
600	3000
700	3500
800	4000
900	4500

APPLICATION INFORMATION

Power Supply Recommendations

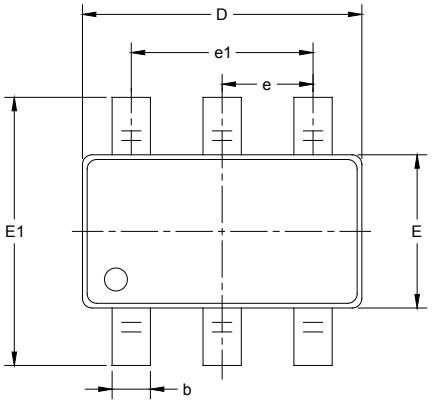
The SGM821 requires a voltage supply within 1.8V and 5.5V. A multilayer ceramic bypass X7R capacitor of 0.1μF between VDD and GND pin is recommended.

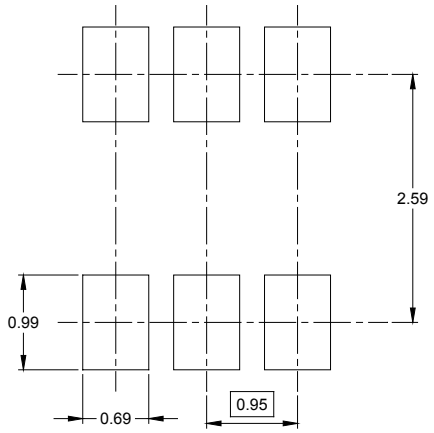
Layout Guidelines

The DELAY/M_RST pin is sensitive to parasitic capacitance. It is recommended that the traces connecting the resistance on this pin to GND be kept as short as possible to minimize parasitic capacitance. This capacitance can affect the initial set up of the time interval. Signal integrity on the WAKE and RSTn pins is also improved by keeping the trace length between the SGM821 and the μC short to reduce the parasitic capacitance.

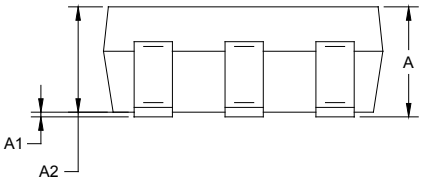
PACKAGE OUTLINE DIMENSIONS

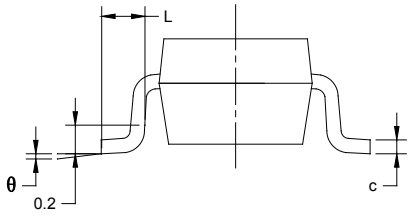
SOT-23-6





RECOMMENDED LAND PATTERN (Unit: mm)

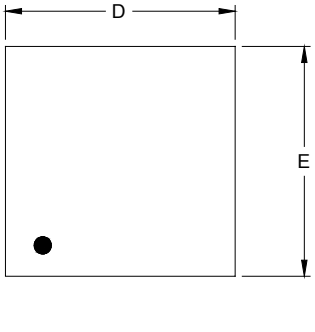




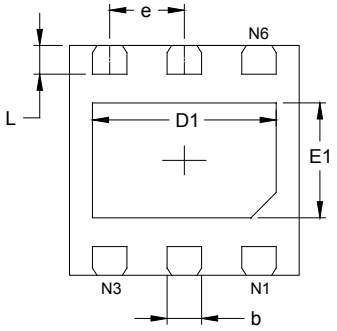
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 BSC		0.037 BSC	
e1	1.900 BSC		0.075 BSC	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

PACKAGE OUTLINE DIMENSIONS

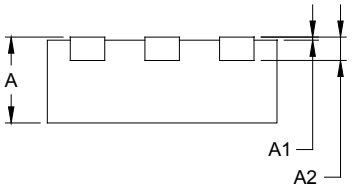
TDFN-2×2-6AL



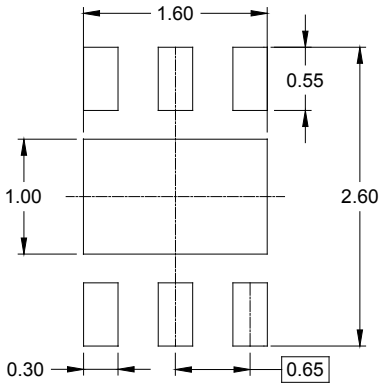
TOP VIEW



BOTTOM VIEW



SIDE VIEW

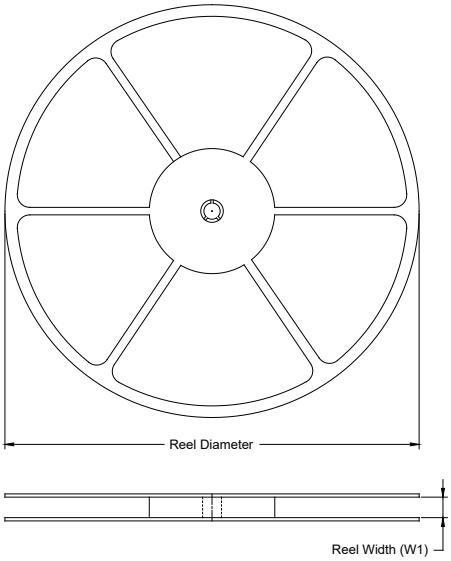


RECOMMENDED LAND PATTERN (Unit: mm)

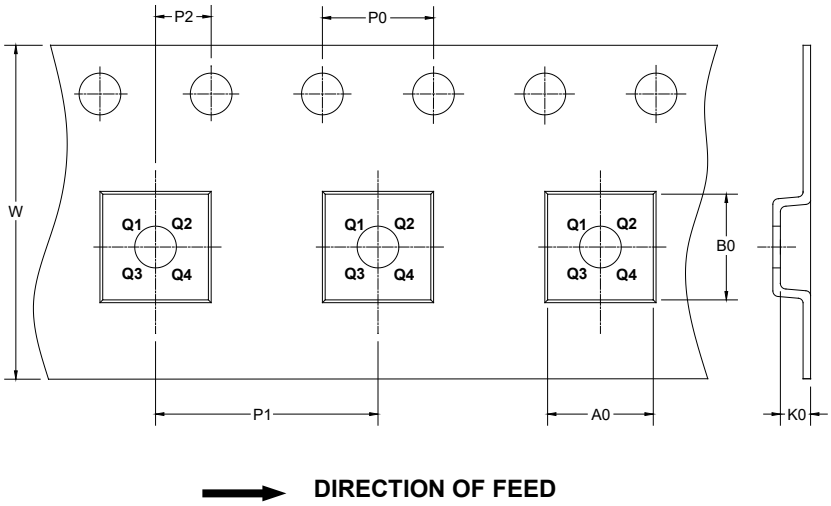
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	1.900	2.100	0.075	0.083
D1	1.500	1.700	0.059	0.067
E	1.900	2.100	0.075	0.083
E1	0.900	1.100	0.035	0.043
b	0.250	0.350	0.010	0.014
e	0.650 BSC		0.026 BSC	
L	0.174	0.326	0.007	0.013

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



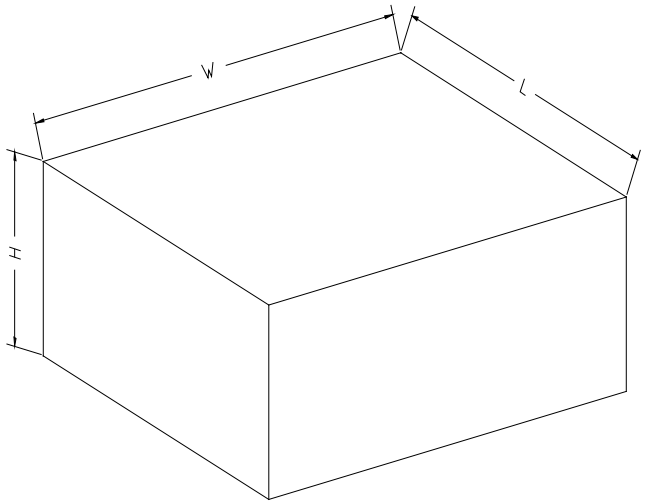
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-6	7″	9.5	3.17	3.23	1.37	4.0	4.0	2.0	8.0	Q3
TDFN-2×2-6AL	7″	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002