SGM4570Q
Dual-Supply Translating Transceiver with Auto Direction Sensing and Open-Drain

GENERAL DESCRIPTION

The SGM4570Q is a 4-bit, dual-supply translating transceiver. The auto direction sensing function allows a bidirectional voltage level translation for the device. The nA and nB are 4-bit data input-output ports and OE is an output enable input. V_{CCA} and V_{CCB} are two supply pins that accept the voltage from 1.65V to 3.6V and 2.3V to 5.5V respectively. This makes the translation among voltage nodes of 1.8V, 2.5V, 3.3V and 5V. OE and nA pins track the V_{CCA} supply, and nB pins track the V_{CCB} supply. When OE pin is held low, the outputs enter a high-impedance off-state.

This device is AEC-Q100 qualified (Automotive Electronics Council Standard Q100 Grade 1) and the use of this device is suitable for automotive applications.

FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
  Device Temperature Grade 1
  T_A = -40℃ to +125℃
- **V_{CCA} Supply Voltage Range: 1.65V to 3.6V**
- **V_{CCB} Supply Voltage Range: 2.3V to 5.5V**
- **Inputs Accept Voltages up to 5.5V**
- **Push-Pull Data Rates: 24Mbps (MAX)**
- **Support Partial Power-Down Mode**
- **Available in a Green TSSOP-14 Package**

APPLICATIONS

Automotive Applications
Computers
Mobile Phones

FUNCTION TABLE

SUPPLY VOLTAGE		INPUT	INPUT/OUTPUT	
V_{CCA} (1)	V_{CCB}	OE	nA	nB
1.65V to 3.6V	2.3V to 5.5V	L	Z	Z
1.65V to 3.6V	2.3V to 5.5V	H	Input or Output	Output or Input
GND (2)	GND (2)	*X*	Z	Z

H = High Voltage Level
L = Low Voltage Level
Z = High-Impedance Off-State
X = Don't Care

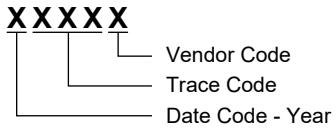
NOTES:
1. $V_{CCA} \leq V_{CCB}$ and $V_{CCA} \leq 3.6V$.
2. The device enters power-down mode when either V_{CCA} or V_{CCB} is at GND.

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE TOP MARKING	PACKING OPTION
SGM4570Q	TSSOP-14	-40℃ to +125℃	SGM4570QTS14G/TR	MEG TS14 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage Range, V_{CCA} ..... -0.5V to 6.5V
Supply Voltage Range, V_{CCB} ..... -0.5V to 6.5V
Input Voltage Range, V_I (2) ..... -0.5V to 6.5V
Output Voltage, V_O (2)
Active Mode, A or B ports ..... -0.5V to V_{CCO} + 0.5V
Power-Down or 3-State Mode
A Ports ..... -0.5V to 4.6V
B Ports ..... -0.5V to 6.5V
Input Clamping Current, I_{IK} (V_I < 0V) ..... -50mA
Output Clamping Current, I_{OK} (V_O < 0V) ..... -50mA
Output Current, I_O (V_O = 0V to V_{CC})
High-State ..... -50mA
Low-State 50mA
Supply Current, I_{CCA} or I_{CCB} 100mA
Ground Current, I_{GND} ..... -100mA
Junction Temperature (3) ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{CCA} ..... 1.65V to 3.6V
Supply Voltage Range, V_{CCB} ..... 2.3V to 5.5V
Input Transition Rise and Fall Rate, Δt/ΔV
A or B Ports, Push-Pull Driving
V_{CCA} = 1.65V to 3.6V, V_{CCB} = 2.3V to 5.5V ..... 10ns/V (MAX)
OE Input
V_{CCA} = 1.65V to 3.6V, V_{CCB} = 2.3V to 5.5V ..... 10ns/V (MAX)
Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

2. The minimum input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

3. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

ESD SENSITIVITY CAUTION

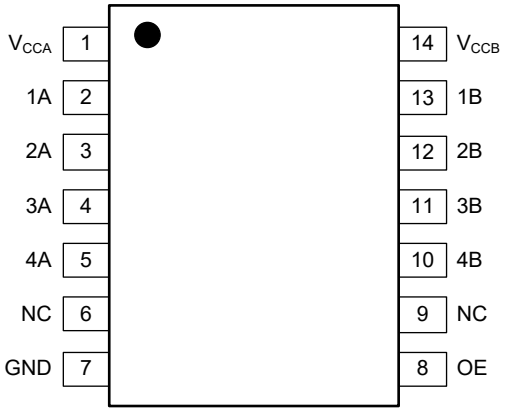
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TSSOP-14

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	V_{CCA}	Supply Voltage on A Ports.
2, 3, 4, 5	1A, 2A, 3A, 4A	Data Inputs/Outputs. They track the V_{CCA} supply.
6, 9	NC	No Connection.
7	GND	Ground.
8	OE	Output Enable Input. It tracks the V_{CCA} supply. (Active High)
10, 11, 12, 13	4B, 3B, 2B, 1B	Data Inputs/Outputs. They track the V_{CCB} supply.
14	V_{CCB}	Supply Voltage on B Ports.

ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃, unless otherwise noted.) (1)

PARAMETER	SYMBOL	CONDITIONS			TEMP	MIN	TYP	MAX	UNITS
High-Level Input Voltage	V_{IH}	A ports	V_{CCA} = 1.65V to 1.95V, V_{CCB} = 2.3V to 5.5V		Full	V_{CCA} - 0.2		V_{CCA}	V
			V_{CCA} = 2.3V to 3.6V, V_{CCB} = 2.3V to 5.5V		Full	V_{CCA} - 0.4		V_{CCA}	
		B ports	V_{CCA} = 1.65V to 3.6V, V_{CCB} = 2.3V to 5.5V		Full	V_{CCB} - 0.4		V_{CCB}	
		OE input	V_{CCA} = 1.65V to 3.6V, V_{CCB} = 2.3V to 5.5V		Full	0.75 × V_{CCA}		V_{CCA}	
Low-Level Input Voltage	V_{IL}	A or B ports	V_{CCA} = 1.65V to 3.6V, V_{CCB} = 2.3V to 5.5V		Full	0		0.15	V
		OE input	V_{CCA} = 1.65V to 3.6V, V_{CCB} = 2.3V to 5.5V		Full	0		0.35 × V_{CCA}	
High-Level Output Voltage	V_{OH}	A ports	I_O = -20μA, V_I ≥ V_{CCB} - 0.4V, V_{CCA} = 1.65V to 3.6V, V_{CCB} = 2.3V to 5.5V		Full	0.67 × V_{CCA}			V
		B ports	I_O = -20μA, V_I ≥ V_{CCA} - 0.2V, V_{CCA} = 1.65V to 3.6V, V_{CCB} = 2.3V to 5.5V		Full	0.67 × V_{CCB}			
Low-Level Output Voltage	V_{OL}	A or B ports	I_O = 1mA, V_I ≤ 0.15V, V_{CCA} = 1.65V to 3.6V, V_{CCB} = 2.3V to 5.5V		Full			0.4	V
Input Leakage Current	I_I	OE input	V_{CCA} = 1.65V to 3.6V, V_{CCB} = 2.3V to 5.5V		+25℃			±1	μA
					Full			±2	
Off-State Output Current	I_{OZ}	A or B ports	OE = 0V, V_{CCA} = 1.65V to 3.6V, V_{CCB} = 2.3V to 5.5V		+25℃			±1	μA
					Full			±2	
Power-Off Leakage Current	I_{OFF}	A ports	V_{CCA} = 0V, V_{CCB} = 0V to 5.5V		+25℃			±1	μA
					Full			±5	
		B ports	V_{CCB} = 0V, V_{CCA} = 0V to 3.6V		+25℃			±1	
					Full			±5	
Supply Current	I_{CC}	OE = 0V or V_{CCA}, nA, nB open							
		I_{CCA}	V_{CCA} = 1.65V to 3.6V, V_{CCB} = 2.3V to 5.5V		Full		3	12	μA
			V_{CCA} = 3.6V, V_{CCB} = 0V		Full		3.5	12	
			V_{CCA} = 0V, V_{CCB} = 5.5V		Full		-0.1	-2	
		I_{CCB}	V_{CCA} = 1.65V to 3.6V, V_{CCB} = 2.3V to 5.5V		Full		5	20	μA
			V_{CCA} = 3.6V, V_{CCB} = 0V		Full		-0.1	-2	
			V_{CCA} = 0V, V_{CCB} = 5.5V		Full		3.5	12	
		I_{CCA} + I_{CCB}	V_{CCA} = 1.65V to 3.6V, V_{CCB} = 2.3V to 5.5V		Full		8	32	μA
Input Capacitance	C_I	OE input	V_{CCA} = 3.3V, V_{CCB} = 3.3V		+25℃		4		pF
Input/Output Capacitance	$C_{I/O}$	A ports	V_{CCA} = 3.3V, V_{CCB} = 3.3V	Enabled	+25℃		12		pF
				Disabled	+25℃		5		
		B ports	V_{CCA} = 3.3V, V_{CCB} = 3.3V	Enabled	+25℃		12		
				Disabled	+25℃		5		

NOTE:

1. V_{CCA} ≤ V_{CCB} and V_{CCA} ≤ 3.6V.

DYNAMIC CHARACTERISTICS

(See Figure 1 for test circuit. See Figure 2 and Figure 3 for waveforms. Full = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	V_{CCB}						UNITS
				2.5V		3.3V		5.0V		
				MIN (1)	MAX (1)	MIN (1)	MAX (1)	MIN (1)	MAX (1)	
V_{CCA} = 1.8V										
High to Low Propagation Delay	t_{PHL}	nA to nB	Full	1	6.5	2.5	8.5	3.5	13	ns
Low to High Propagation Delay	t_{PLH}	nA to nB	Full	3	12	2.5	11	2.5	10.5	ns
High to Low Propagation Delay	t_{PHL}	nB to nA	Full	1	5	1.5	5	1.5	5.5	ns
Low to High Propagation Delay	t_{PLH}	nB to nA	Full	0.5	3	0.5	2.5	0.5	2	ns
Enable Time (2)	t_{EN}	OE to nA, nB	Full	1	160	4.5	180	4.5	280	ns
Disable Time (2)	t_{DIS}	OE to nA	Full	35	230	30	240	35	210	ns
		OE to nB	Full	50	215	50	300	30	190	
Low to High Output Transition Time	t_{TLH}	A ports	Full	3.5	17	3	17	2.5	16.5	ns
		B ports	Full	4	16	3.5	14	3	13	
High to Low Output Transition Time	t_{THL}	A ports	Full	0.5	7.5	0.5	7.5	0.5	7.5	ns
		B ports	Full	1.5	10	3.5	13	5	20	
Output Skew Time (3)	$t_{SK(O)}$	Between channels	Full		1.5		1.5		1.5	ns
Pulse Width	t_W	Data inputs	Full	50		41		41		ns
Data Rate	f_{DATA}		Full		20		24		24	Mbps
V_{CCA} = 2.5V										
High to Low Propagation Delay	t_{PHL}	nA to nB	Full	0.5	5	1	4.5	1.5	5.5	ns
Low to High Propagation Delay	t_{PLH}	nA to nB	Full	0.5	4	1	7	1.5	7.5	ns
High to Low Propagation Delay	t_{PHL}	nB to nA	Full	0.5	4.5	0.5	4	0.5	4.5	ns
Low to High Propagation Delay	t_{PLH}	nB to nA	Full	0.5	3.5	0.5	2.5	0.5	2.5	ns
Enable Time (2)	t_{EN}	OE to nA, nB	Full	2.5	18	0.5	30	2.5	140	ns
Disable Time (2)	t_{DIS}	OE to nA	Full	26	180	25	165	20	165	ns
		OE to nB	Full	50	165	55	250	35	170	
Low to High Output Transition Time	t_{TLH}	A ports	Full	2.5	11	1.5	10	1	9.5	ns
		B ports	Full	3	13	2	11	2	10	
High to Low Output Transition Time	t_{THL}	A ports	Full	0.5	6	0.5	5	0.5	5.5	ns
		B ports	Full	0.5	6.5	1	7	2	9	
Output Skew Time (3)	$t_{SK(O)}$	Between channels	Full		1.5		1.5		1.5	ns
Pulse Width	t_W	Data inputs	Full	50		41		41		ns
Data Rate	f_{DATA}		Full		20		24		24	Mbps

DYNAMIC CHARACTERISTICS (continued)

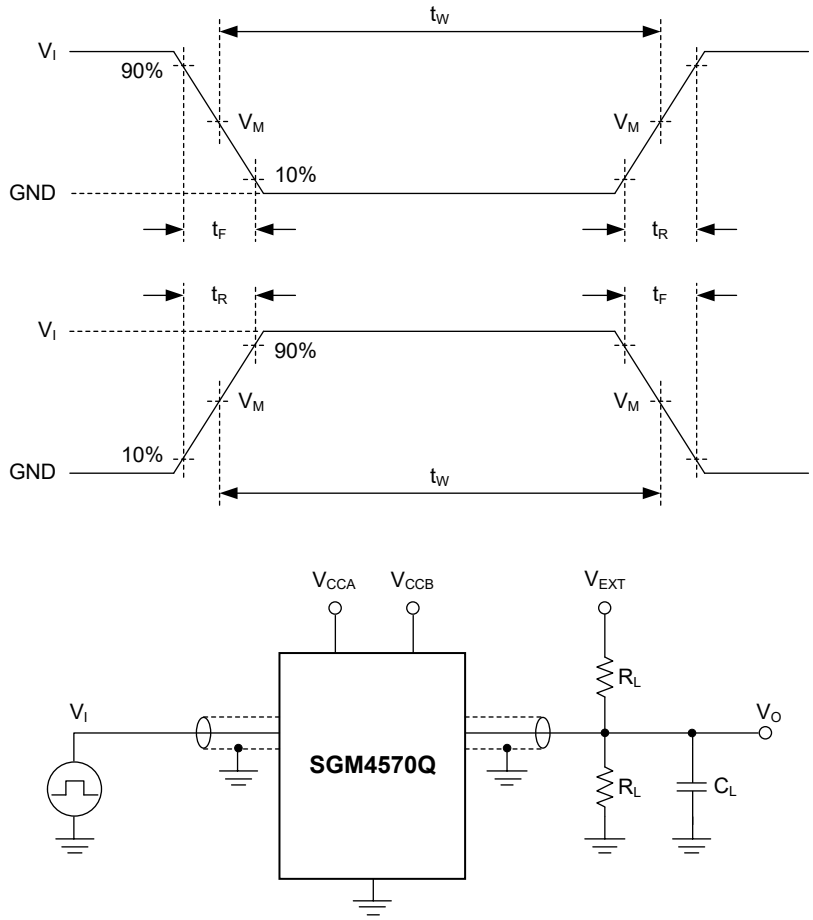
(See Figure 1 for test circuit. See Figure 2 and Figure 3 for waveforms. Full = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	V_{CCB}						UNITS
				2.5V		3.3V		5.0V		
				MIN (1)	MAX (1)	MIN (1)	MAX (1)	MIN (1)	MAX (1)	
V_{CCA} = 3.3V										
High to Low Propagation Delay	t_{PHL}	nA to nB	Full			0.5	4.5	1	4.5	ns
Low to High Propagation Delay	t_{PLH}	nA to nB	Full			0.5	4	1	5	ns
High to Low Propagation Delay	t_{PHL}	nB to nA	Full			0.5	4	0.5	4.5	ns
Low to High Propagation Delay	t_{PLH}	nB to nA	Full			0.5	3.5	0.5	3	ns
Enable Time (2)	t_{EN}	OE to nA, nB	Full			2	12	0.5	30	ns
Disable Time (2)	t_{DIS}	OE to nA	Full			35	220	40	215	ns
		OE to nB	Full			55	240	30	165	
Low to High Output Transition Time	t_{TLH}	A ports	Full			2	8	1.5	7	ns
		B ports	Full			2	9.5	2	8	
High to Low Output Transition Time	t_{THL}	A ports	Full			0.5	5.5	0.5	5	ns
		B ports	Full			0.5	5.5	0.5	6.5	
Output Skew Time (3)	$t_{SK(O)}$	Between channels	Full				1.5		1.5	ns
Pulse Width	t_W	Data inputs	Full			41		41		ns
Data Rate	f_{DATA}		Full				24		24	Mbps

NOTES:

1. Specified by design and characterization, not production tested.
2. t_{EN} is the same as t_{PZL} and t_{PZH}. t_{DIS} is the same as t_{PLZ} and t_{PHZ}.
3. Skew between any two outputs of the same package switches in the same direction.

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions for test circuit:

R_L: Load resistance.

C_L: Load capacitance (includes jig and probe).

V_{EXT}: External voltage used to measure switching time.

Figure 1. Test Circuit for Measuring Switching Times

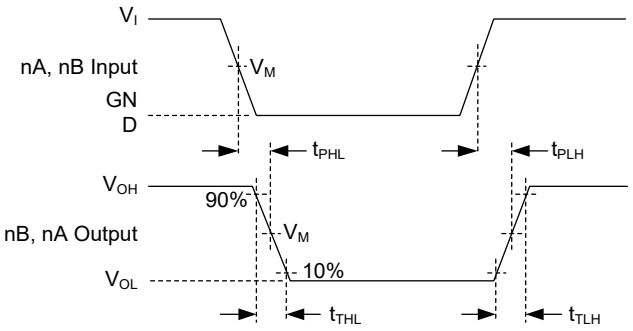
Table 1. Test Conditions

SUPPLY VOLTAGE		INPUT		LOAD		V_{EXT}		
V_{CCA}	V_{CCB}	V_I	t_R, t_F	C_L	R_L (2)	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.65V to 3.6V	2.3V to 5.5V	V_{CCI} (1)	≤ 1ns	15pF	50kΩ, 1MΩ	Open	2 × V_{CCO} (3)	Open

NOTES:

1. V_{CCI} is the supply voltage associated with the data input ports.
2. R_L = 50kΩ is used for enable time and disable time measurement.
   R_L = 1MΩ is used for the measurements of pulse width, propagation delay, data rate and output rise and fall time.
3. V_{CCO} is the supply voltage associated with the data output ports.

WAVEFORMS

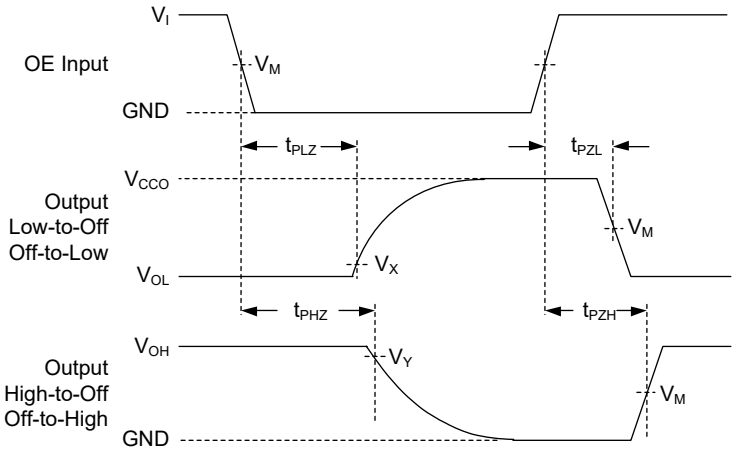


Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 2. Input (nA, nB) to Output (nB, nA) Propagation Delays



Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 3. Enable and Disable Times

Table 2. Measurement Points

SUPPLY VOLTAGE	INPUT		OUTPUT		
V_{CCO} (2)	V_I	V_M (3)	V_M	V_X	V_Y
1.8V	V_{CCI} (1)	0.5 × V_{CCI}	0.5 × V_{CCO}	V_{OL} + 0.15V	V_{OH} - 0.15V
2.5V	V_{CCI}	0.5 × V_{CCI}	0.5 × V_{CCO}	V_{OL} + 0.15V	V_{OH} - 0.15V
3.3V	V_{CCI}	0.5 × V_{CCI}	0.5 × V_{CCO}	V_{OL} + 0.3V	V_{OH} - 0.3V
5.0V	V_{CCI}	0.5 × V_{CCI}	0.5 × V_{CCO}	V_{OL} + 0.3V	V_{OH} - 0.3V

NOTES:

1. V_{CCI} is the supply voltage associated with the data input ports.
2. V_{CCO} is the supply voltage associated with the data output ports.
3. The measurement points should be V_{IH} or V_{IL} when the input rising or falling time exceeds 1ns.

APPLICATION INFORMATION

Voltage Level-Translation Applications

SGM4570Q can be used between two devices with different power supply voltages.

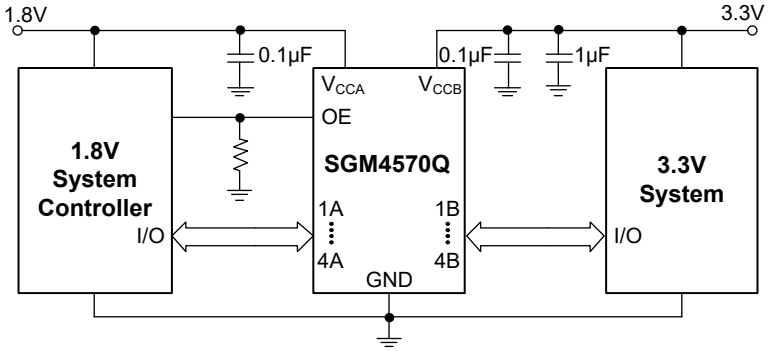


Figure 4. Recommended Application Circuit

Internal Structure

Figure 5 illustrates the internal structure of SGM4570Q. There is no control mechanism for the bidirectional transmission.

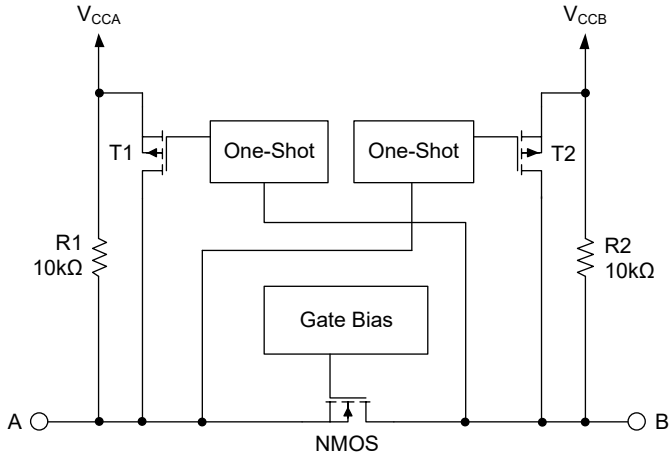


Figure 5. Internal Structure of SGM4570Q (one channel)

SGM4570Q can transmit the signal transparently with two enable mechanisms:

1. An NMOS transistor is placed between the two ports to turn on or off the transmission.
2. An accelerator is located at the output of SGM4570Q. Its function is to accelerate the rising edge of the signal.

For the application of low-to-high transition, the one-shot mechanism is significant as it can accelerate the transition of output. If the voltage level of the input signal reaches V_{IH}, the one-shot mechanism will be triggered. After that, one-shot mechanism is disabled and the pull-up resistor will dominate. The output impedance is within the range of 50Ω and 70Ω when the device is accelerating. If the users want to transmit a signal from the other direction, please make sure to transmit the signal after the one-shot mechanism is turned off to minimize dynamic current and contention. The pull-up resistors are in the internal of SGM4570Q.

Input Driver Requirements

The shape of the input signal affects the output directly, because SGM4570Q is a voltage translator with switching characteristics. The amount of sinking current is determined by the structure of driver (push-pull or open-drain). In addition, the output impedance and the edge-rate of the driver will determine the properties of propagation delay, max data rate and transition time of high-to-low output. The typical value shown in this datasheet is under the condition of 50Ω output impedance.

APPLICATION INFORMATION (continued)

Output Load Considerations

The application of heavy capacitive load would affect the ability of one-shot mechanism, which means that the output of the device may not reach the positive supply rail within the duration of one-shot pulse. To reduce this possibility, users need to use shorter traces in PCB and less capacitive connectors. In addition, another advantage of using short traces is to provide low-impedance, avoiding oscillation of the signal, allowing reflection of the signal within one-shot duration and avoiding retriggering of one-shot function.

Power-up

For the application of SGM4570Q, the V_{CCA} should be less than V_{CCB}. However, it does not matter if the power supply voltage is ramping, and the sequence of power-up for both V_{CCA} and V_{CCB} is not defined. If one of the two power supplies is switched off, the internal circuit can disable the operation of SGM4570Q.

Enable and Disable

The OE pin is used to disable the output of the device, which means that if this pin is low, all of the transmitting pins are in high-impedance mode. The disable time (t_{DIS}) of this process is defined between the start of low position at OE pin and the start of output disables. For the definition of enable time (t_{EN}), it refers to the time between when OE pin is high and when the one-shot circuit is launched. In addition, if the users want to keep the device in off-state (high-impedance mode) when the power supply voltage is rising or falling, please connect OE pin to ground with a suitable resistor. And the value of the selected resistor is determined by the sinking-current capability of the driver.

Pull-up or Pull-down Resistors on I/O Lines

For both A and B sides, each transmission pin is pulled up to the power supply of A and B respectively. An external resistor that is parallel with the internal 10kΩ resistor can be added, which will affect the value of V_{OL}. However, the internal pull-up resistor will be disabled if OE pin is low.

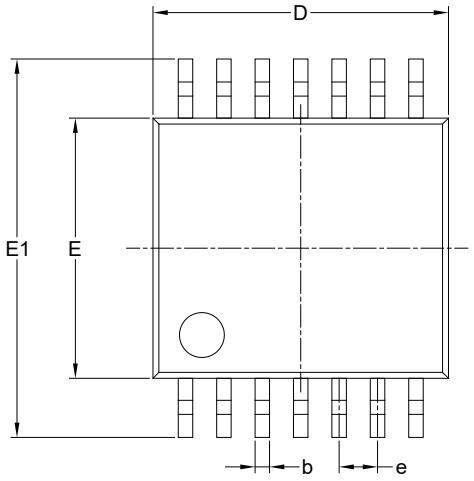
REVISION HISTORY

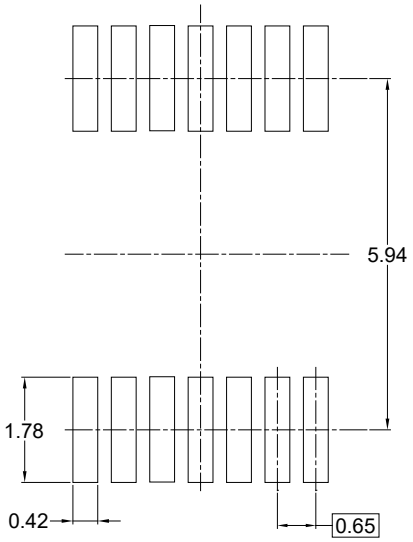
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (MARCH 2023) to REV.A	Page
Changed from product preview to production data	All

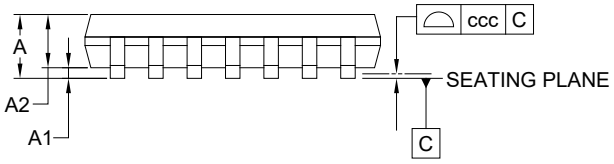
PACKAGE OUTLINE DIMENSIONS

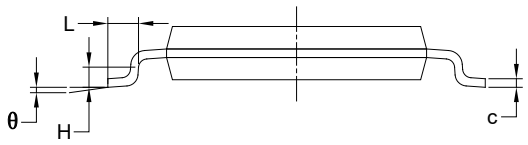
TSSOP-14





RECOMMENDED LAND PATTERN (Unit: mm)



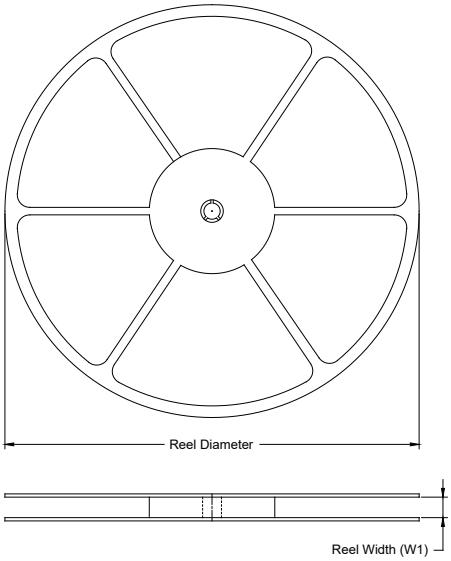


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	4.860	-	5.100
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

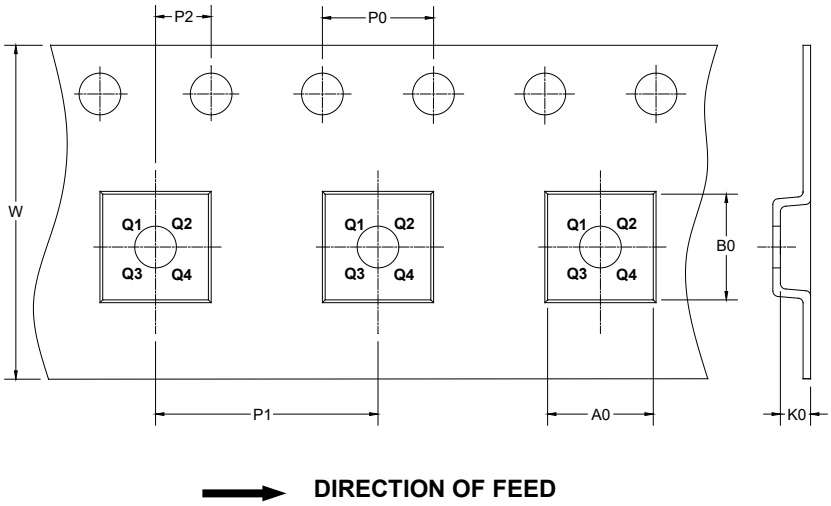
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

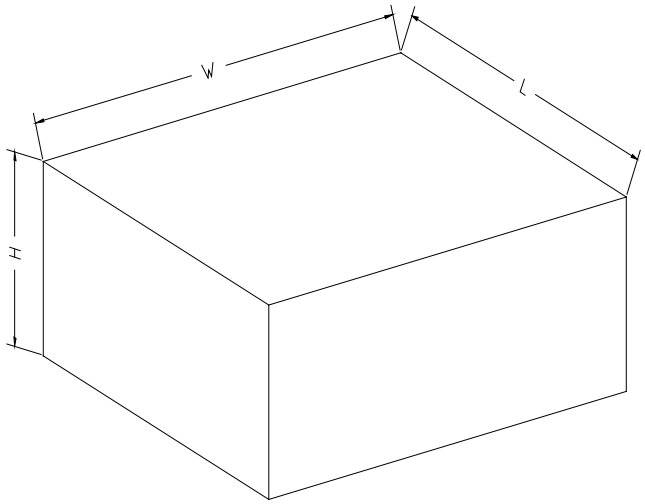
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-14	13″	12.4	6.80	5.40	1.50	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002