

# SGM721Q Automotive, 11MHz, Rail-to-Rail I/O CMOS Operational Amplifier

## **GENERAL DESCRIPTION**

The SGM721Q is a single, low voltage, low noise and low power operational amplifier for automotive applications. This device can operate from 2.1V to 5.5V single supply, and consumes low quiescent current.

The SGM721Q features a 1.5mV typical input offset voltage. The minimum input common mode voltage is within 0.1V below the negative rail, and the output swing is rail-to-rail with heavy loads. It exhibits a high gain-bandwidth product of 11MHz and a slew rate of  $7V/\mu s$ . These specifications make the operational amplifier appropriate for various applications.

The SGM721Q is available in a Green SOT-23-5 package. It is specified over the extended industrial temperature range (-40°C to +125°C).

This device is AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and it is suitable for automotive applications.

## FEATURES

- AEC-Q100 Qualified for Automotive Applications Device Temperature Grade 1 T<sub>A</sub> = -40°C to +125°C
- Input Offset Voltage: 1.5mV (TYP)
- High Gain-Bandwidth Product: 11MHz
- High Slew Rate: 7V/µs
- Settling Time to 0.1% with 2V Step: 0.4µs
- Overload Recovery Time: 0.5µs
- Low Noise: 8.5nV/<del>√Hz</del> at 10kHz
- Rail-to-Rail Input and Output
- Supply Voltage Range: 2.1V to 5.5V
- Input Voltage Range: -0.1V to 5.6V with V<sub>s</sub> = 5.5V
- Low Quiescent Current: 1.2mA (TYP)
- Available in a Green SOT-23-5 Package

## **APPLICATIONS**

Automotive Application Sensor Automotive Inverter Automotive Audio Active Filter Driver of A/D Converter Photodiode Amplification



## PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION	
SGM721Q	SOT-23-5	-40°C to +125°C	SGM721QN5G/TR	0GQXX	Tape and Reel, 3000	

### MARKING INFORMATION

NOTE: XX = Date Code.

YYY X X Date Code - Week

Date Code - Year
Date Code - Year
Serial Number

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

## **ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, +V <sub>S</sub> to -V <sub>S</sub>	6V
Input Common Mode Voltage Rang	e
	V <sub>S</sub> ) - 0.3V to (+V <sub>S</sub> ) + 0.3V
Package Thermal Resistance	
SOT-23-5, θ <sub>JA</sub>	163.5°C/W
Junction Temperature	+150°C
Storage Temperature Range	65°C to +150°C
Lead Temperature (Soldering, 10s)	+260°C

## **RECOMMENDED OPERATING CONDITIONS**

Operating Temperature Range .....-40°C to +125°C

## **OVERSTRESS CAUTION**

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

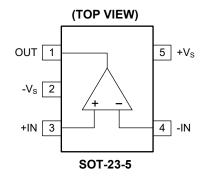
#### **ESD SENSITIVITY CAUTION**

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

#### DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

## **PIN CONFIGURATION**



# **ELECTRICAL CHARACTERISTICS**

(V<sub>S</sub> = 5V, V<sub>CM</sub> = V<sub>S</sub>/2, and R<sub>L</sub> = 600 $\Omega$ , typical values are at T<sub>A</sub> = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS	
Input Characteristics	•						
Input Offset Voltage (V <sub>OS</sub> )		+25°C		1.5		mV	
Input Offset Voltage Drift ( $\Delta V_{OS}/\Delta T$ )		+25°C		5.5		µV/°C	
Input Bias Current (I <sub>B</sub> )		+25°C		10		pА	
Input Offset Current (I <sub>OS</sub> )		+25°C		10		pА	
Input Common Mode Voltage Range ( $V_{CM}$ )	V <sub>S</sub> = 5.5V	+25°C		-0.1 to 5.6		V	
Ourse Martin Data dia Patia (OMD	$V_{\rm S}$ = 5.5V, $V_{\rm CM}$ = -0.1V to 4V	+25°C		81		dB	
Common Mode Rejection Ratio (CMRR)	$V_{\rm S}$ = 5.5V, $V_{\rm CM}$ = -0.1V to 5.6V	+25°C		75			
Open Lean Veltage Cain $(\Lambda_{-})$	$V_{OUT}$ = 0.15V to 4.85V, $R_L$ = 600 $\Omega$	+25°C		89		dB	
Open-Loop Voltage Gain (A <sub>OL</sub> )	$V_{OUT}$ = 0.05V to 4.95V, R <sub>L</sub> = 10k $\Omega$	+25°C		100			
Output Characteristics							
	R <sub>L</sub> = 600Ω	+25°C		0.076		- v	
Output Voltage Swing from Rail	R <sub>L</sub> = 10kΩ	+25°C		0.006			
Output Current (I <sub>OUT</sub> )		+25°C		58		mA	
Closed-Loop Output Impedance	f = 1MHz, G = 1	+25°C		9.5		Ω	
Power Supply	•			· · ·			
Operating Voltage Range		+25°C	2.1		5.5	V	
Power Supply Rejection Ratio (PSRR)	$V_{\rm S}$ = 2.1V to 5.5V, $V_{\rm CM}$ = (-V <sub>S</sub> ) + 0.5V	+25°C		79		dB	
Quiescent Current (I <sub>Q</sub> )	I <sub>OUT</sub> = 0mA	+25°C		1.2		mA	
Dynamic Performance	•			· · ·			
Gain-Bandwidth Product (GBP)	C <sub>L</sub> = 50pF	+25°C		11		MHz	
Phase Margin ( $\phi_{O}$ )	C <sub>L</sub> = 50pF	+25°C		60		۰	
Full-Power Bandwidth (BW <sub>P</sub> )	< 1% distortion, $V_{OUT}$ = 1 $V_{P-P}$	+25°C		200		kHz	
Slew Rate (SR)	G = 1, 2V output step	+25°C		7		V/µs	
Settling Time to 0.1% (t <sub>s</sub> )	G = 1, 2V output step	+25°C		0.4		μs	
Overload Recovery Time	$V_{IN} \times G = V_S$	+25°C		0.5		μs	
Noise Performance	·	•					
	f = 1kHz	+25°C		12.5		\	
Input Voltage Noise Density (e <sub>n</sub> )	f = 10kHz	+25℃		8.5		nV/√H	

## **APPLICATION INFORMATION**

#### **Rail-to-Rail Input**

When SGM721Q works at the power supply between 2.1V and 5.5V, the input common mode voltage range is from  $(-V_S) - 0.1V$  to  $(+V_S) + 0.1V$ . In Figure 1, the ESD diodes between the inputs and the power supply rails will clamp the input voltage not to exceed the rails.

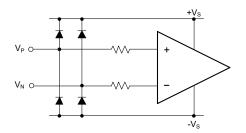


Figure 1. Input Equivalent Circuit

#### **Input Current-Limit Protection**

For ESD diode clamping protection, when the current flowing through ESD diode exceeds the maximum rating value, the ESD diode and amplifier will be damaged, so current-limit protection will be added in some applications. One resistor is selected to limit the current not to exceed the maximum rating value. In Figure 2, a series input resistor is used to limit the input current to less than 10mA, but the drawback of this current-limit resistor is that it contributes thermal noise at the amplifier input. If this resistor must be added, its value must be selected as small as possible.

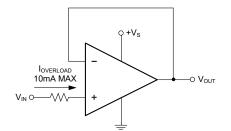


Figure 2. Input Current-Limit Protection

## **Rail-to-Rail Output**

The SGM721Q supports rail-to-rail output operation. In single power supply application, for example, when +V<sub>S</sub> = 5V, -V<sub>S</sub> = GND, 10k $\Omega$  load resistor is tied from OUT pin to ground, the typical output swing range is from 0.006V to 4.994V.

#### **Driving Capacitive Loads**

The SGM721Q is designed for driving the 4700pF capacitive load with unity-gain stable. If greater capacitive load must be driven in application, the circuit in Figure 3 can be used. In this circuit, the IR drop voltage generated by  $R_{ISO}$  is compensated by feedback loop.

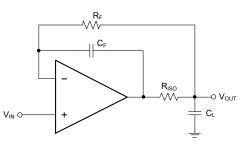


Figure 3. Circuit to Drive Heavy Capacitive Load

#### **Power Supply Decoupling and Layout**

A clean and low noise power supply is very important in amplifier circuit design, besides of input signal noise, the power supply is one of important source of noise to the amplifier through  $+V_s$  and  $-V_s$  pins. Power supply bypassing is an effective method to clear up the noise at power supply, and the low impedance path to ground of decoupling capacitor will bypass the noise to GND. In application,  $10\mu$ F ceramic capacitor paralleled with  $0.1\mu$ F or  $0.01\mu$ F ceramic capacitor is used in Figure 4. The ceramic capacitors should be placed as close as possible to  $+V_s$  and  $-V_s$  power supply pins.

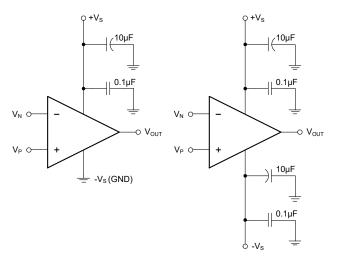


Figure 4. Amplifier Power Supply Bypassing



## **APPLICATION INFORMATION (continued)**

#### Grounding

In low speed application, one node grounding technique is the simplest and most effective method to eliminate the noise generated by grounding. In high speed application, the general method to eliminate noise is to use a complete ground plane technique, and the whole ground plane will help distribute heat and reduce EMI noise pickup.

## Reduce Input-to-Output Coupling

To reduce the input-to-output coupling, the input traces must be placed as far away from the power supply or output traces as possible. The sensitive trace must not be placed in parallel with the noisy trace in same layer. They must be placed perpendicularly in different layers to reduce the crosstalk. These PCB layout techniques will help to reduce unwanted positive feedback and noise.

## **Typical Application Circuits**

#### **Difference Amplifier**

The circuit in Figure 5 is a design example of classical difference amplifier. If  $R_4/R_3$  =  $R_2/R_1$ , then  $V_{OUT}$  = ( $V_P$  -  $V_N$ ) ×  $R_2/R_1$  +  $V_{REF}$ .

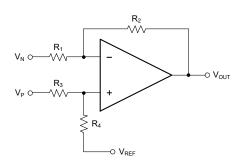
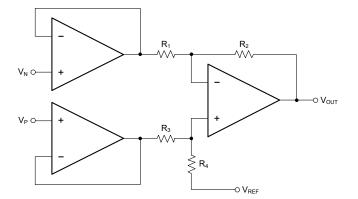


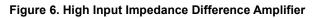
Figure 5. Difference Amplifier

#### High Input Impedance Difference Amplifier

The circuit in Figure 6 is a design example of high input impedance difference amplifier, the added amplifiers at

the input are used to increase the input impedance and eliminate drawback of low input impedance in Figure 5.





#### Active Low-Pass Filter

The circuit in Figure 7 is a design example of active low-pass filter, the DC gain is equal to  $-R_2/R_1$  and the -3dB corner frequency is equal to  $1/2\pi R_2C$ . In this design, the filter bandwidth must be less than the bandwidth of the amplifier, the resistor values must be selected as low as possible to reduce ringing or oscillation generated by the parasitic parameters in PCB layout.

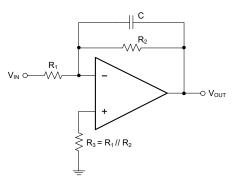
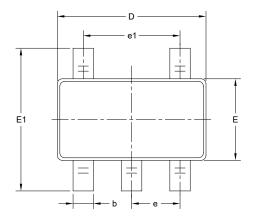


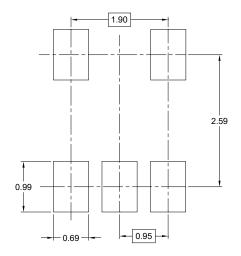
Figure 7. Active Low-Pass Filter



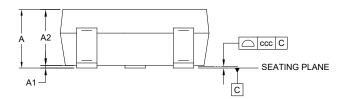
## PACKAGE OUTLINE DIMENSIONS

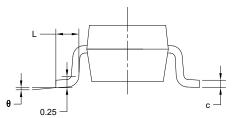
## SOT-23-5





#### RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dir	Dimensions In Millimeters						
Symbol	MIN	MOD	МАХ					
A	-	-	1.450					
A1	0.000	-	0.150					
A2	0.900	-	1.300					
b	0.300	-	0.500					
С	0.080	-	0.220					
D	2.750	-	3.050					
E	1.450	-	1.750					
E1	2.600	-	3.000					
е	0.950 BSC							
e1	1.900 BSC							
L	0.300	-	0.600					
θ	0°	-	8°					
ссс	0.100							

#### NOTES:

1. This drawing is subject to change without notice.

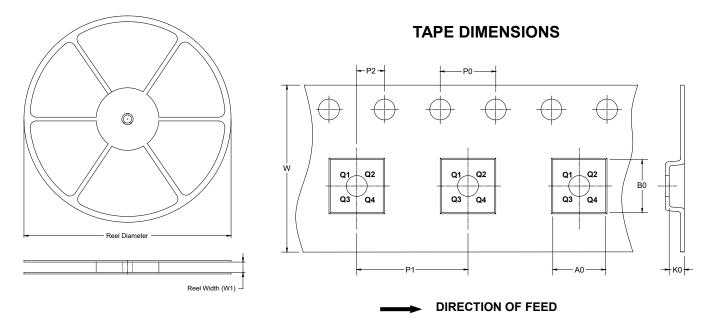
2. The dimensions do not include mold flashes, protrusions or gate burrs.

3. Reference JEDEC MO-178.



## TAPE AND REEL INFORMATION

### **REEL DIMENSIONS**

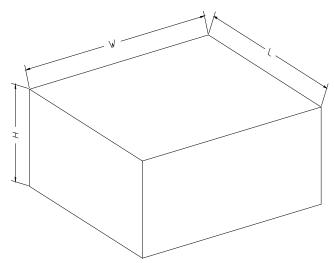


NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-5	7″	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3

## **CARTON BOX DIMENSIONS**



NOTE: The picture is only for reference. Please make the object as the standard.

## **KEY PARAMETER LIST OF CARTON BOX**

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton	
7" (Option)	368	227	224	8	
7"	442	410	224	18	DD0002

