SGM90508

8-Channel, 12-Bit, Configurable ADC/VDAC/IDAC with On-Chip Reference, I²C Interface

GENERAL DESCRIPTION

The SGM90508 features 8 input/output (I/O) pins, which can be independently configured as voltage digital-to-analog converter (VDAC) outputs, current digital-to-analog converter (IDAC) outputs, analog-to-digital converter (ADC) inputs, digital outputs, or digital inputs. When an I/O pin is configured as an analog output, it is driven by a 12-bit VDAC. The VDAC output range can be configured to 0V to V_{REF} or 0V to 2 × V_{REF}. When an I/O pin is configured as an ADC input, it is an analog input to ADC by an analog multiplexer. The ADC input range can be configured to V_{REF} or 2 × V_{REF}. The I/O pins can also be configured as digital general-purpose input or output (GPIO) pins.

The SGM90508 contains an integrated 2.5V, 11ppm/℃ (TYP) reference that is turned off by default. And the chip has an on-chip temperature sensor, which can read out the die temperature through an ADC read sequence.

The SGM90508 is available in Green TSSOP-16, TQFN-3×3-16BL and WLCSP-2.05×2.05-16B packages. It operates over an ambient temperature range of -40℃ to +105℃.

FEATURES

- **Configurable 8 I/O Pins**
  - **8 Channels, 12-Bit VDAC**
  - **4 Channels, 12-Bit IDAC**
  - **8 Channels, 12-Bit ADC**
  - **8 Channels, GPIO**
- **Ultra-Low Drift IDAC: 100ppm/℃ (TYP)**
- **On-Chip Temperature Sensor**
- **Supply Monitor**
- **I²C Interface**
- **Available in Green TSSOP-16, TQFN-3×3-16BL and WLCSP-2.05×2.05-16B Packages**

APPLICATIONS

Optical Module
Industrial Automation
General-Purpose Analog and Digital I/O

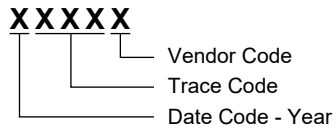
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM90508	TSSOP-16	-40℃ to +105℃	SGM90508GTS16G/TR	SGM90508 GTS16 XXXXX	Tape and Reel, 4000
	TQFN-3×3-16BL	-40℃ to +105℃	SGM90508GTSK16G/TR	00XSK XXXXX	Tape and Reel, 4000
	WLCSP-2.05×2.05-16B	-40℃ to +105℃	SGM90508GG/TR	90508 XXXXX XX#XX	Tape and Reel, 3000

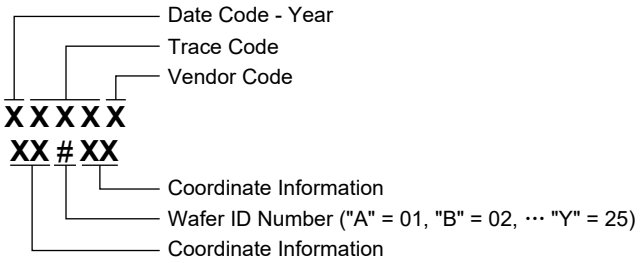
MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.

TSSOP-16/TQFN-3×3-16BL



WLCSP-2.05×2.05-16B



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to GND)

V_{DD} (1) ..... -0.3V to 6V

V_{LOGIC} (1) ..... -0.3V to 6V

Analog Input Voltage ..... -0.3V to V_{DD} + 0.3V

Digital Input Voltage ..... -0.3V to V_{LOGIC} + 0.3V

Digital Output Voltage ..... -0.3V to V_{LOGIC} + 0.3V

V_{REF} ..... -0.3V to V_{DD} + 0.3V

Package Thermal Resistance

TSSOP-16, θ_{JA} ..... 88℃/W

TQFN-3×3-16BL, θ_{JA} ..... 91℃/W

WLCSP-2.05×2.05-16B, θ_{JA} ..... 97℃/W

Junction Temperature ..... +150℃

Storage Temperature Range ..... -65℃ to +150℃

Lead Temperature (Soldering, 10s) ..... +260℃

ESD Susceptibility

HBM 1500V

CDM 500V

NOTE:

1. V_{DD} is powered up first, and the V_{DD} voltage must be higher than or equal to the V_{LOGIC} voltage.

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +105℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

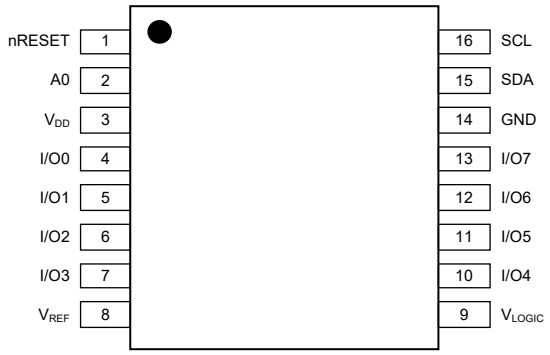
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

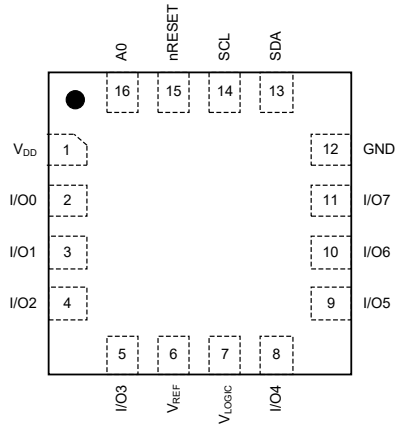
PIN CONFIGURATIONS

(TOP VIEW)



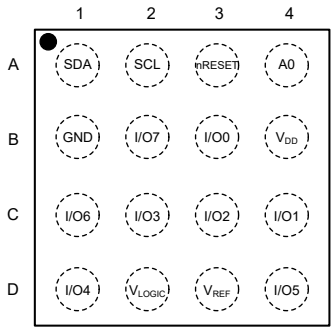
TSSOP-16

(TOP VIEW)



TQFN-3×3-16BL

(TOP VIEW)



WLCSP-2.05×2.05-16B

PIN DESCRIPTION

PIN			NAME	FUNCTION
TSSOP-16	TQFN-3×3-16BL	WLCSP-2.05×2.05-16B		
1	15	A3	nRESET	Asynchronous Reset Pin. This pin is active low. Tie this pin high for normal working.
2	16	A4	A0	Address Input Pin. Set the LSB of the 7-bit slave address.
3	1	B4	V_{DD}	Power Supply Pin.
4, 5, 6, 7, 10, 11, 12, 13	2, 3, 4, 5, 8, 9, 10, 11	B3, C4, C3, C2, D1, D4, C1, B2	I/O0 to I/O7	Input/Output 0 through Input/Output 7. These pins can be independently configured as VDACs, ADCs, or GPIOs. I/O0 to I/O3 can be independently configured as IDAC output. The function of each pin is software configured in the configuration registers.
8	6	D3	V_{REF}	Reference Input/Output Pin. If the internal reference is enabled, a 2.5V reference voltage is connected internally. An outside decoupling capacitor is recommended on this pin.
9	7	D2	V_{LOGIC}	Interface Power Supply Pin.
14	12	B1	GND	Ground.
15	13	A1	SDA	Serial Data Input Pin. SDA is an open-drain pin. It must be pulled up to the V_{LOGIC} supply by an external resistor.
16	14	A2	SCL	Serial Clock Input Pin. SCL is an open-drain pin. It must be pulled up to the V_{LOGIC} supply by an external resistor.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V to 5.5V, V_{REF} = 2.5V (internal), 1.7V ≤ V_{LOGIC} ≤ V_{DD}, T_A = -40℃ to +105℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Performance (f_{IN} = 1kHz Sine Wave)						
Resolution				12		Bits
Input Range		ADC range select bit = 0	0		V_{REF}	V
		ADC range select bit = 1	0		2 × V_{REF}	
Integral Nonlinearity	INL			±1.1		LSB
Differential Nonlinearity	DNL			±0.9		LSB
Offset Error	E_O			5.7		mV
Gain Error	E_G			0.09		% FSR
Track Time (1)	t_{TRACK}		500			ns
Conversion Time (1)	t_{CONV}				2	μs
Signal-to-Noise Ratio (2)	SNR	V_{DD} = 2.7V, input range = 0V to V_{REF}		68		dB
		V_{DD} = 3.3V, input range = 0V to V_{REF}		66		
		V_{DD} = 5.5V, input range = 0V to 2 × V_{REF}		66		
Signal-to-Noise + Distortion	SINAD	V_{DD} = 2.7V, input range = 0V to V_{REF}		68		dB
		V_{DD} = 3.3V, input range = 0V to V_{REF}		66		
		V_{DD} = 5.5V, input range = 0V to 2 × V_{REF}		65		
Total Harmonic Distortion	THD	V_{DD} = 2.7V, input range = 0V to V_{REF}		-79		dB
		V_{DD} = 3.3V, input range = 0V to V_{REF}		-77		
		V_{DD} = 5.5V, input range = 0V to 2 × V_{REF}		-77		
Spurious Free Dynamic Range	SFDR	V_{DD} = 2.7V, input range = 0V to V_{REF}		80		dB
		V_{DD} = 3.3V, input range = 0V to V_{REF}		78		
		V_{DD} = 5.5V, input range = 0V to 2 × V_{REF}		78		
Channel-to-Channel Isolation		f_{IN} = 1kHz		-95		dB
Full Power Bandwidth		At -3dB		22		MHz
		At -0.1dB		3		
VDAC Performance (3)						
Resolution				12		Bits
Output Range		DAC range select bit = 0	0		V_{REF}	V
		DAC range select bit = 1	0		2 × V_{REF}	
Integral Nonlinearity	INL		-4.5		3.5	LSB
Differential Nonlinearity	DNL		-0.99		1	LSB
Offset Error	E_O		-21		22	mV
Offset Error Drift (1)				9		μV/℃
Gain Error	E_G	Output range = 0V to V_{REF}	-0.7		0.92	% FSR
		Output range = 0V to 2 × V_{REF}	-0.87		0.6	
Zero-Code Error				1.1	12	mV
Total Unadjusted Error	TUE	Output range = 0V to V_{REF}		±0.07	±1.14	% FSR
		Output range = 0V to 2 × V_{REF}		±0.19	±0.72	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 5.5V, V_{REF} = 2.5V (internal), 1.7V ≤ V_{LOGIC} ≤ V_{DD}, T_A = -40℃ to +105℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VDAC Performance (3)						
Capacitive Load Stability		R_{LOAD} = ∞			2	nF
		R_{LOAD} = 1kΩ			10	
Resistive Load (1)			1			kΩ
Short-Circuit Current				25		mA
DC Crosstalk (1)		Due to single channel, full-scale output change	-4		4	μV
DC Output Impedance				0.2		Ω
DC Power Supply Rejection Ratio (1)	PSRR	DAC code = mid-scale, V_{DD} = 3V ± 10% or 5V ± 10%		0.01		mV/V
Load Impedance at Rails (4)				57		Ω
Load Regulation		V_{DD} = 5V ± 10%, DAC code = mid-scale, -10mA ≤ I_{OUT} ≤ 10mA		150		μV/mA
		V_{DD} = 3V ± 10%, DAC code = mid-scale, -10mA ≤ I_{OUT} ≤ 10mA		100		
Power-Up Time		Exiting power-down mode, V_{DD} = 5V		3.4		μs
VDD ACPSRR		100Hz		96		dB
		1kHz		76		
		10kHz		61		
		100kHz		56		
Slew Rate				0.41		V/μs
Settling Time				3.3		μs
DAC Glitch Impulse				4		nV-sec
DAC to DAC Crosstalk				7		nV-sec
Digital Crosstalk				0.8		nV-sec
Analog Crosstalk				4		nV-sec
Digital Feedthrough				0.1		nV-sec
Multiplying Bandwidth		DAC code = full-scale, output range = 0V to 2 × V_{REF}		240		kHz
Output Voltage Noise Spectral Density		DAC code = mid-scale, output range = 0V to 2 × V_{REF}, measured at 10kHz		210		nV/√Hz
Signal-to-Noise Ratio	SNR			79		dB
Spurious Free Dynamic Range	SFDR			81		dB
Signal-to-Noise + Distortion	SINAD			75		dB
Total Harmonic Distortion	THD			-77		dB
Reference Input						
V_{REF} Input Voltage			2		V_{DD}	V
V_{REF} Input Impedance		DAC output range = 0V to 2 × V_{REF}		15		kΩ
		DAC output range = 0V to V_{REF}		20		
Reference Output						
V_{REF} Output Voltage		At ambient	2.484	2.5	2.516	V
		Factory precision	2.498	2.5	2.502	
V_{REF} Temperature Coefficient				11		ppm/℃

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 5.5V, V_{REF} = 2.5V (internal), 1.7V ≤ V_{LOGIC} ≤ V_{DD}, T_A = -40℃ to +105℃, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Output								
Capacitive Load Stability			R_{LOAD} = 2kΩ			5		μF
Output Impedance			V_{DD} = 2.7V			0.02		Ω
			V_{DD} = 5V			0.02		Ω
Output Voltage Noise			0.1Hz to 10Hz			13		μVp-p
Output Voltage Noise Density			At ambient, f = 1kHz, C_L = 1μF			210		nV/√Hz
Line Regulation			At ambient, sweeping V_{DD} from 2.7V to 5.5V			4		μV/V
			At ambient, sweeping V_{DD} from 2.7V to 3.3V			14		
Load Regulation	Sourcing		At ambient, -5mA ≤ load current ≤ 5mA			10		μV/mA
	Sinking		At ambient, -5mA ≤ load current ≤ 5mA			10		
Output Current Load Capability			V_{DD} ≥ 3V			±5		mA
GPIO Input (5)								
High Input Voltage		V_{IH}			0.7 × V_{DD}			V
Low Input Voltage		V_{IL}					0.3 × V_{DD}	V
Input Capacitance (1)						20		pF
Hysteresis						0.5		V
Input Current						±1		μA
GPIO Output (5)								
High Output Voltage		V_{OH}	I_{SOURCE} = 1mA	V_{DD} = 2.7V	2.3			V
				V_{DD} = 5.5V	5.2			
Low Output Voltage		V_{OL}	I_{SINK} = 1mA	V_{DD} = 2.7V			0.4	V
				V_{DD} = 5.5V			0.4	
Logic Input								
High Input Voltage		V_{INH}			0.7 × V_{LOGIC}			V
Low Input Voltage		V_{INL}					0.3 × V_{LOGIC}	V
Input Current		I_{IN}				±1		μA
Input Capacitance (1)		C_{IN}				10		pF
Logic Output (SDA)								
High Output Voltage		V_{OH}	I_{SOURCE} = 200μA	V_{DD} = 2.7V	1.4			V
				V_{DD} = 5.5V	5.2			
Low Output Voltage		V_{OL}	I_{SINK} = 200μA	V_{DD} = 2.7V			0.4	V
				V_{DD} = 5.5V			0.4	
Floating-State Output Capacitance (1)						10		pF
Temperature Sensor (1)								
Resolution						12		Bits
Operating Temperature Range					-40		+105	℃
Accuracy						±3		℃
Track Time (1)		t_{TRACK}	ADC buffer enabled			2		μs
			ADC buffer disabled			2		
Supply Monitor Accuracy						0.5		%

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 5.5V, V_{REF} = 2.5V (internal), 1.7V ≤ V_{LOGIC} ≤ V_{DD}, T_A = -40℃ to +105℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power Requirements							
Analog Supply Voltage	V_{DD}			2.7		5.5	V
Analog Supply Current	I_{DD}	Digital inputs = 0V or V_{DD}, I/O0 to I/O7 configured as DACs and ADCs, internal reference on, ADC buffer on, DAC code = 0xFFF, range is 0V to 2 × V_{REF} for DACs and ADCs				4.5	mA
		Power-down mode				580	μA
		Normal mode, V_{DD} = 5V	I/O0 to I/O7 are DACs, internal reference, gain = 2		1.14		mA
			I/O0 to I/O7 are DACs, external reference, gain = 2		0.9		mA
			I/O0 to I/O7 are DACs and sampled by the ADC, internal reference, gain = 2		2.4		mA
			I/O0 to I/O7 are DACs and sampled by the ADC, external reference, gain = 2		2.15		mA
			I/O0 to I/O7 are ADCs, internal reference, gain = 2		1.94		mA
			I/O0 to I/O7 are ADCs, external reference, gain = 2		1.7		mA
			I/O0 to I/O7 are general-purpose outputs		0.67		mA
			I/O0 to I/O7 are general-purpose inputs		0.67		mA
		Normal mode, V_{DD} = 3V	I/O0 to I/O7 are DACs, internal reference, gain = 1		0.91		mA
			I/O0 to I/O7 are DACs, external reference, gain = 1		0.73		mA
			I/O0 to I/O7 are DACs and sampled by the ADC, internal reference, gain = 1		2.14		mA
			I/O0 to I/O7 are DACs and sampled by the ADC, external reference, gain = 1		1.96		mA
			I/O0 to I/O7 are ADCs, internal reference, gain = 1		1.75		mA
			I/O0 to I/O7 are ADCs, external reference, gain = 1		1.56		mA
			I/O0 to I/O7 are general-purpose outputs		0.51		mA
			I/O0 to I/O7 are general-purpose inputs		0.51		mA
Digital I/O Supply Voltage	V_{LOGIC}			1.7		V_{DD}	V
Digital I/O Supply Current	I_{LOGIC}					15	μA

NOTES:

1. Guaranteed by design and characterization. Not production tested.
2. All specifications are tested with an input signal at 0.5dB below full-scale, unless otherwise noted. All available input ranges are described in full-scale input range (FSR), but not performance guaranteed.
3. DC specifications are tested when the output is floating, unless otherwise noted. The linearity is calculated with the code range of 64 to 4032.
4. When drawing a load current at either power rail, there will be a voltage dropping respect to the power rail as there is a 57Ω typical output impedance of the chip output channel. For example, when sourcing 1mA, the minimum output voltage dropping = 57Ω × 1mA = 57mV.
5. When the I/O pins are configured as GPIOs, the according input network circuit is powered by V_{DD}, and all inputs threshold and electrical limitations are restricted by V_{DD}.

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V to 5.5V, V_{REF} = 2.5V (internal), 1.7V ≤ V_{LOGIC} ≤ V_{DD}, T_A = -40℃ to +105℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IDAC Performance (3)						
Resolution				12		Bits
Full-Scale Output				80		mA
Supply Voltage (1)			3		5.5	V
Output Compliance Range			0	V_{DD} - 0.6		V
Full-Scale Error (1)		IDAC set to 85% of full-scale		10		%
Minimum Output Current		Minimum code = 256		5		mA
IDAC Temperature Drift				100		ppm/℃
Setting Time		To 0.1%, ±4mA change from mid-scale		6.8		μs
		Full-scale to 5mA		2.2		
VDD ACPSRR		100Hz		96		dB
		1kHz		76		
		10kHz		61		
		100kHz		56		

TIMING CHARACTERISTICS

(All input signals are specified with $t_R = t_F$ = 1ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2, V_{DD} = 2.7V to 5.5V, 1.7V ≤ V_{LOGIC} ≤ V_{DD}, 2.5V ≤ V_{REF} ≤ V_{DD}, T_A = -40℃ to +105℃, unless otherwise noted.)

PARAMETER	SYMBOL	STANDARD MODE			FAST MODE			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
SCL Operating Frequency	f_{SCL}	0.01		0.1	0.01		0.4	MHz
Bus Free Time between START and STOP Condition	t_1	4700			600			ns
Hold Time after Repeated START Condition. After This Period, the First Clock is Generated.	t_2	4000			600			ns
Repeated START Condition Setup Time	t_9	4700			600			ns
Stop Condition Setup Time	t_{10}	4000			600			ns
Data Hold Time	t_5	20			20			ns
Data Setup Time	t_8	250			100			ns
SCL Clock Low Time	t_3	4700			1300			ns
SCL Clock High Time	t_7	4000			600			ns
Clock/Data Fall Time	t_6			300			300	ns
Clock/Data Rise Time	t_4			1000			300	ns

NOTES:
1. Guaranteed by design and characterization. Not production tested.
2. Note that t_6 (MIN) for SDA output is 20ns in normal/fast mode. Glitch filter capability is 50ns in normal/fast mode.

TIMING DIAGRAM

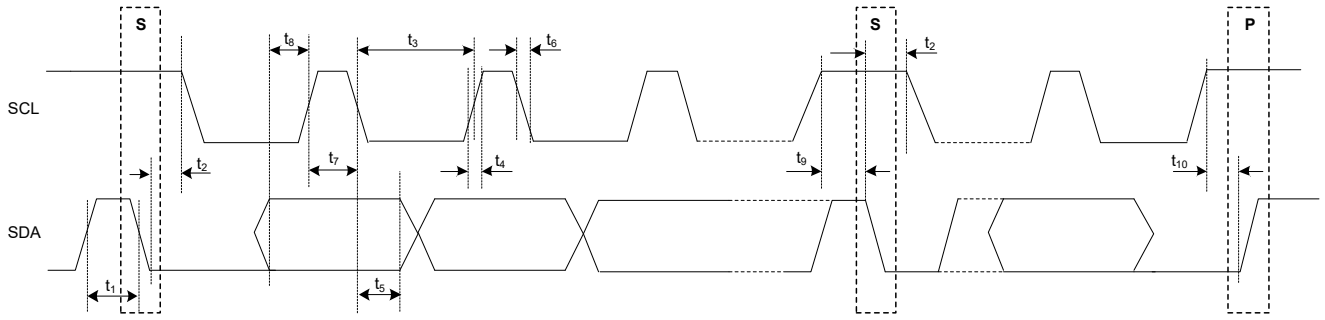
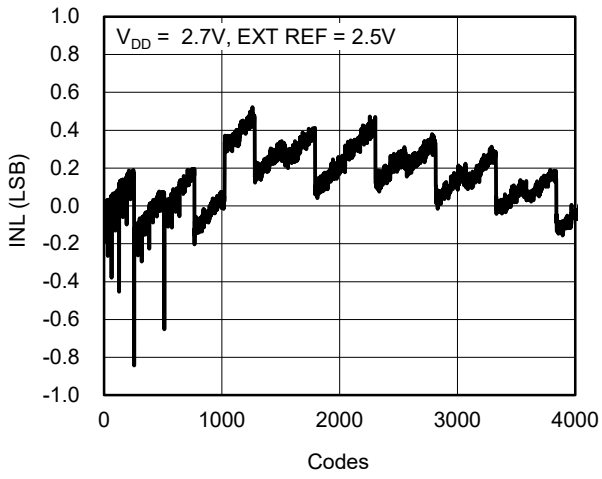


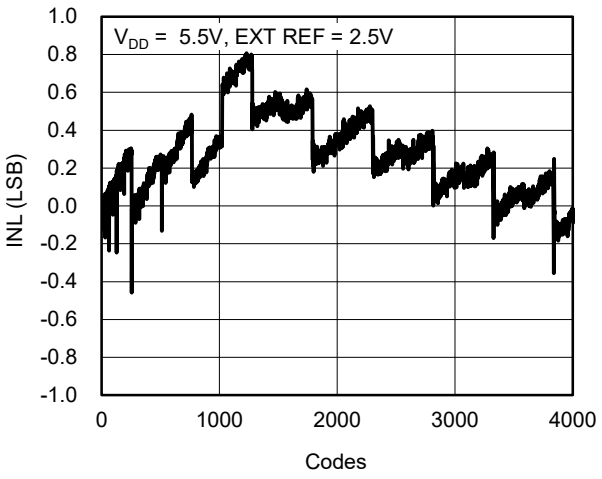
Figure 1. I²C Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

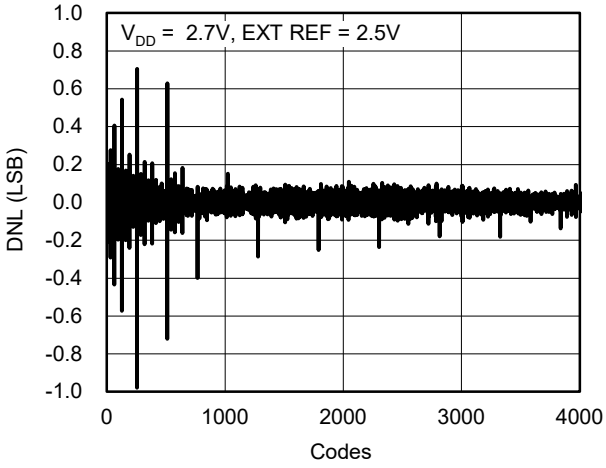
ADC INL (V_{DD} = 2.7V)



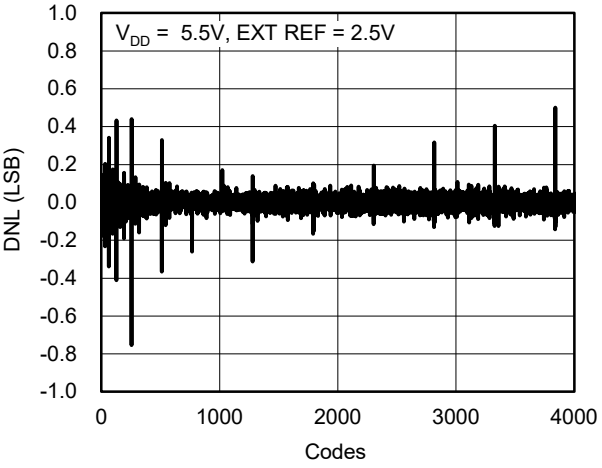
ADC INL (V_{DD} = 5.5V)



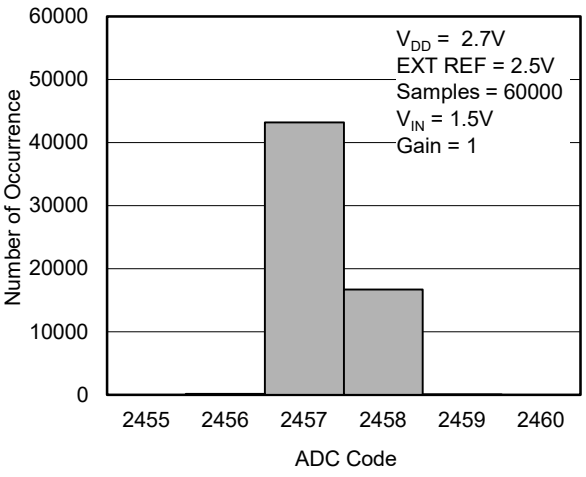
ADC DNL (V_{DD} = 2.7V)



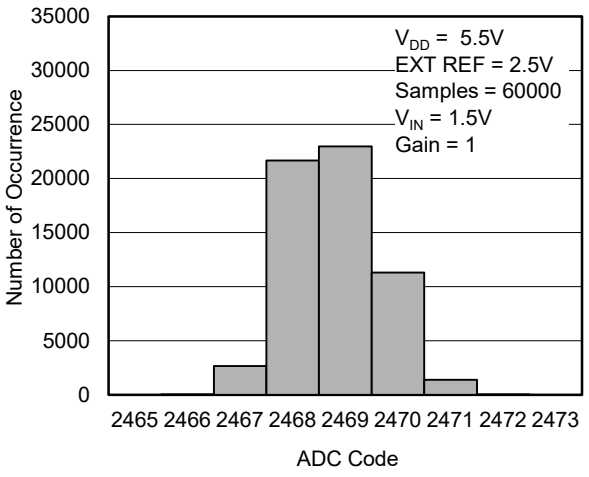
ADC DNL (V_{DD} = 5.5V)



Histogram of ADC Codes (V_{DD} = 2.7V)

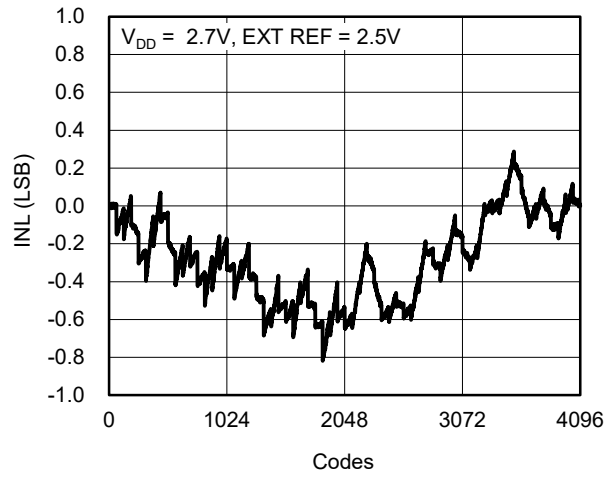


Histogram of ADC Codes (V_{DD} = 5.5V)

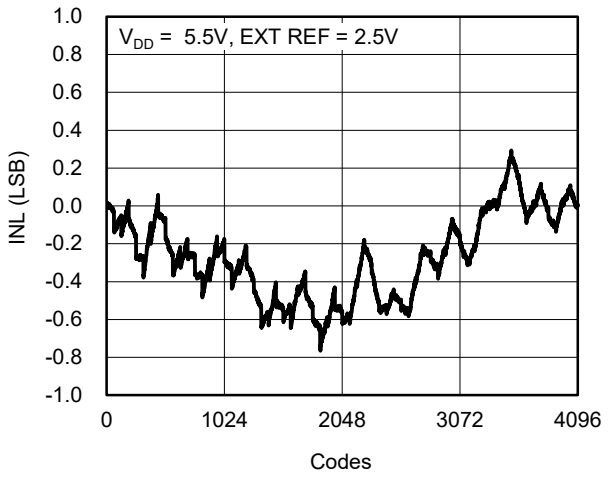


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

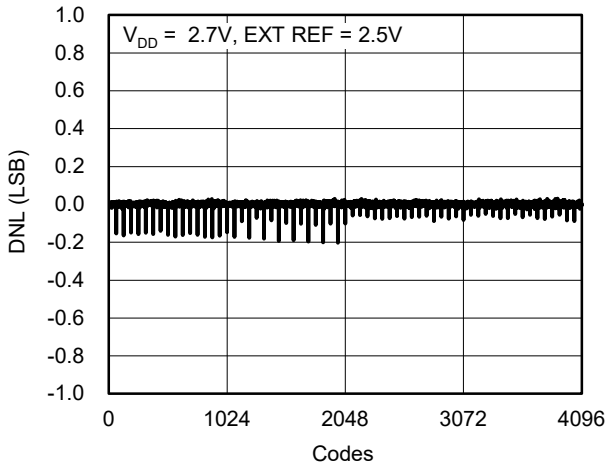
DAC INL (V_{DD} = 2.7V)



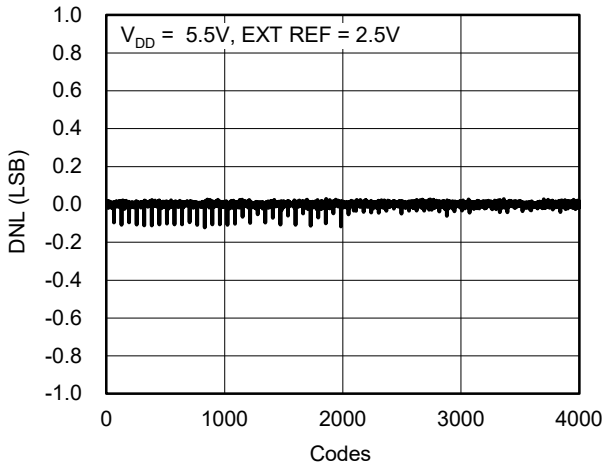
DAC INL (V_{DD} = 5.5V)



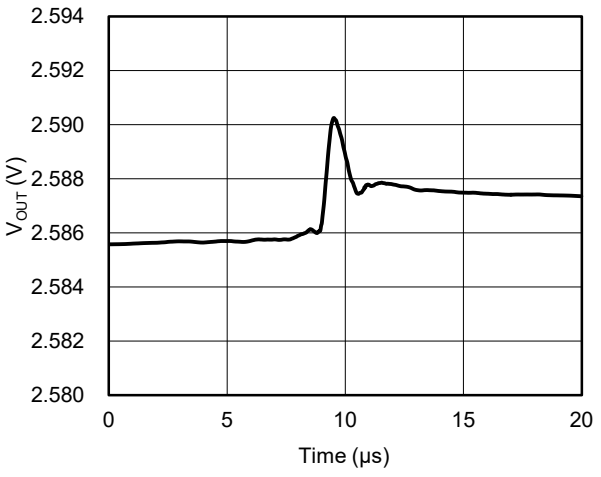
DAC DNL (V_{DD} = 2.7V)



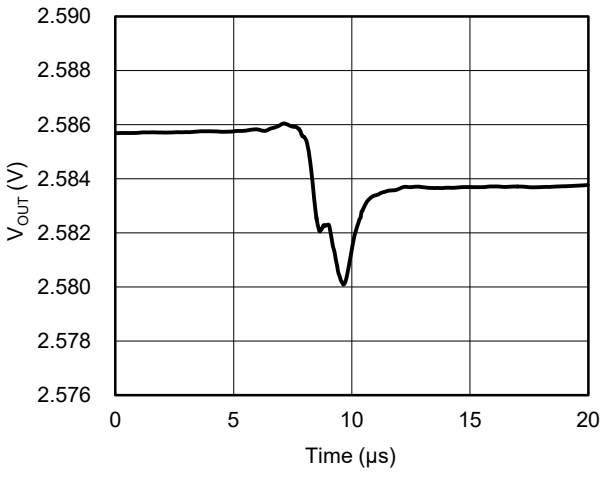
DAC DNL (V_{DD} = 5.5V)



DAC Digital-to-Analog Glitch (Rising)

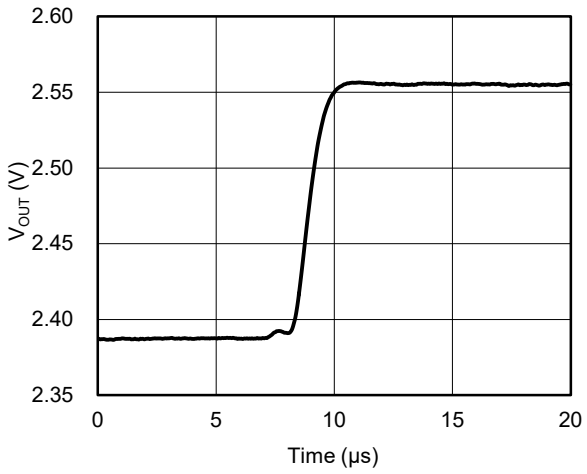


DAC Digital-to-Analog Glitch (Falling)

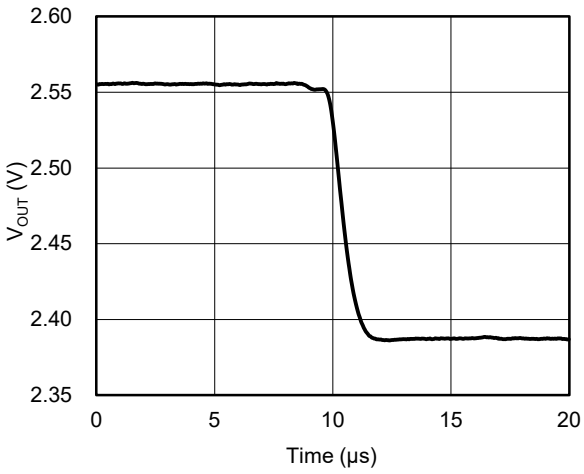


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

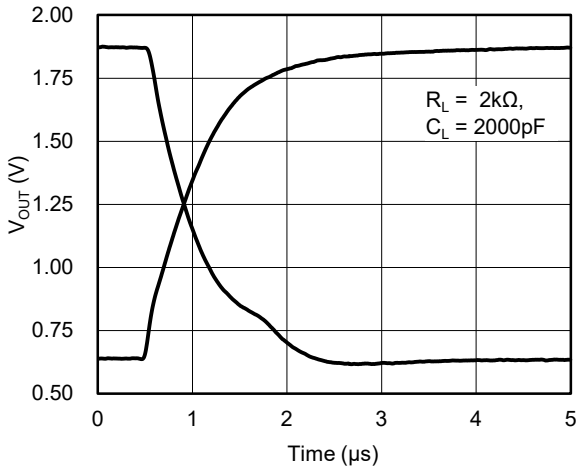
DAC Settling Time (100 Code Change Rising Edge)



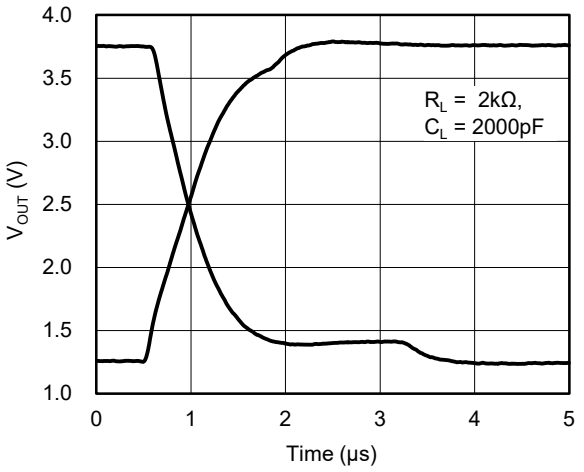
DAC Settling Time (100 Code Change Falling Edge)



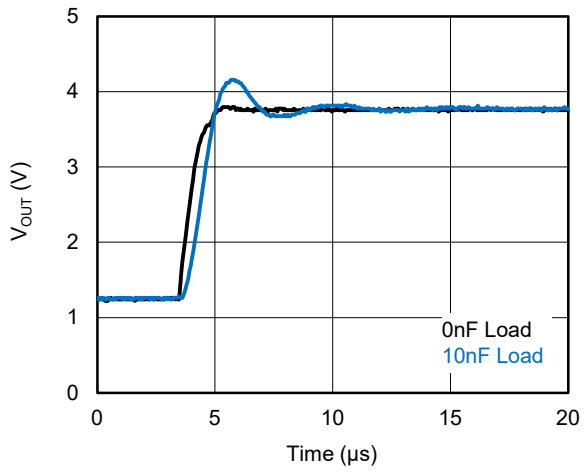
DAC Settling Time (Output Range = 0V to V_{REF})



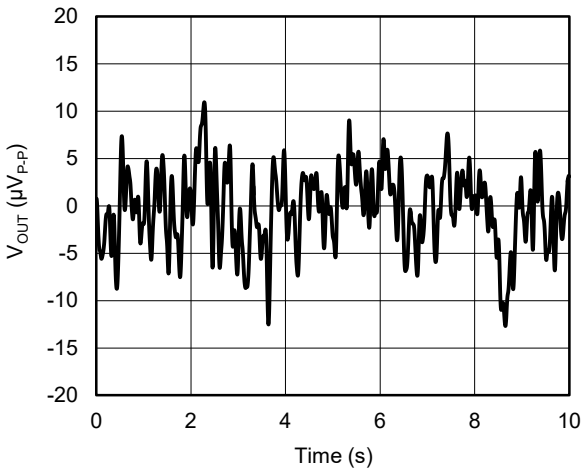
DAC Settling Time (Output Range = 0V to 2 × V_{REF})



DAC Settling Time vs. Capacitive Load

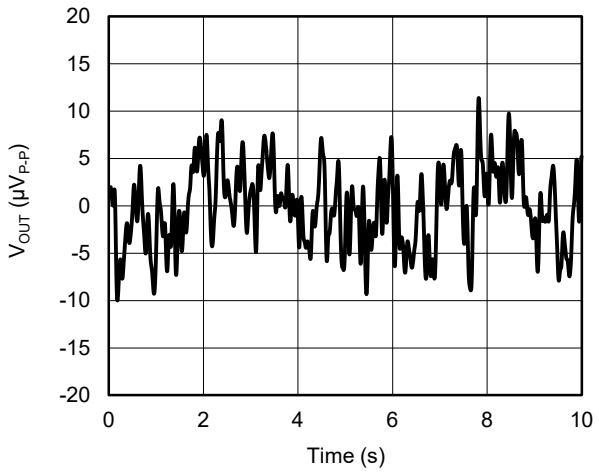


Internal Reference 1/f Noise

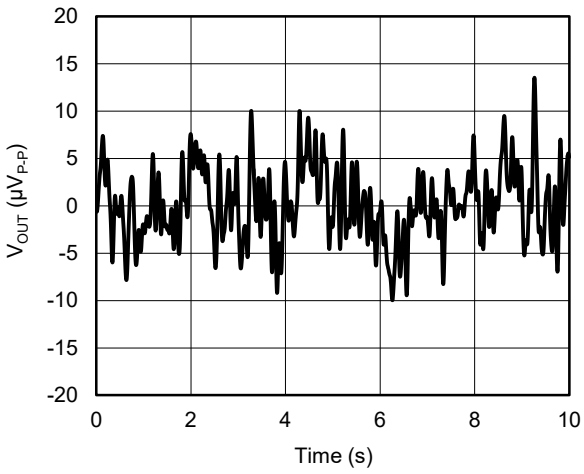


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

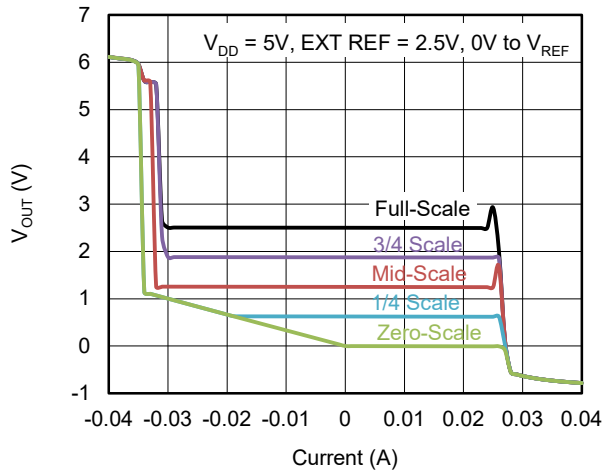
DAC 1/f Noise with External Reference



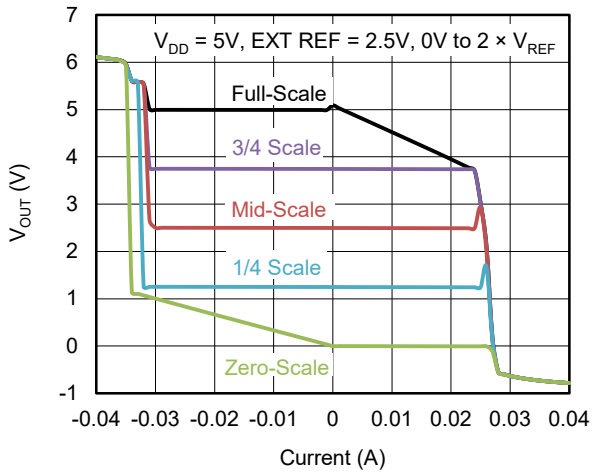
DAC 1/f Noise with Internal Reference



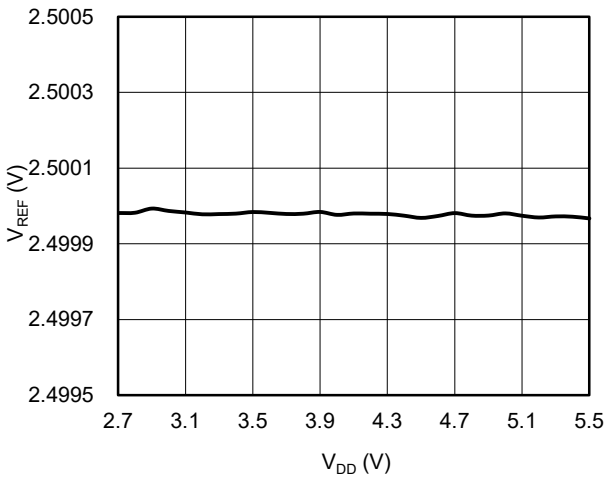
DAC Output Sink and Source Capability



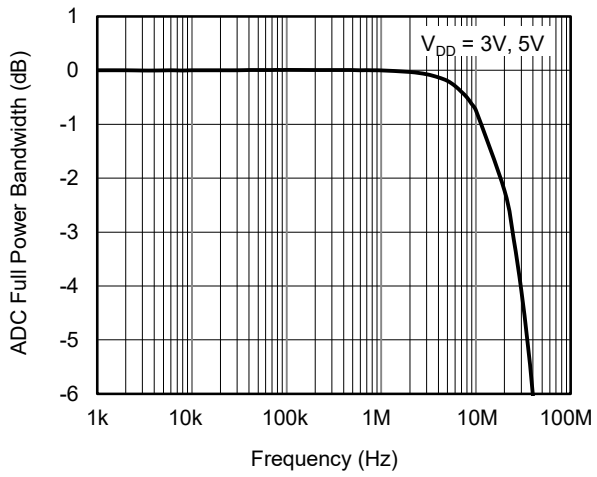
DAC Output Sink and Source Capability



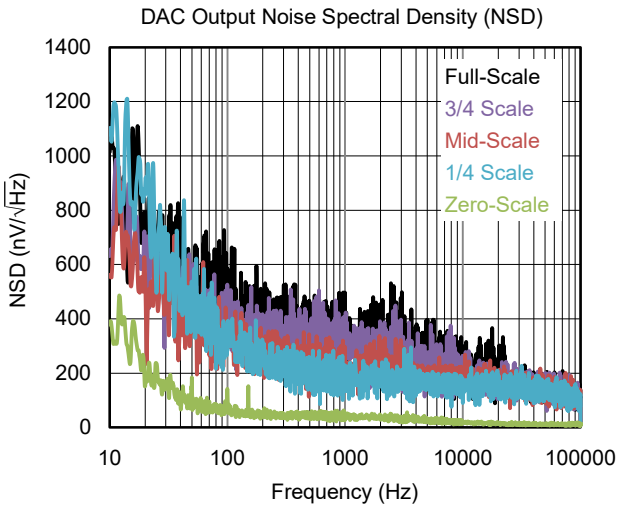
Reference Line Regulation

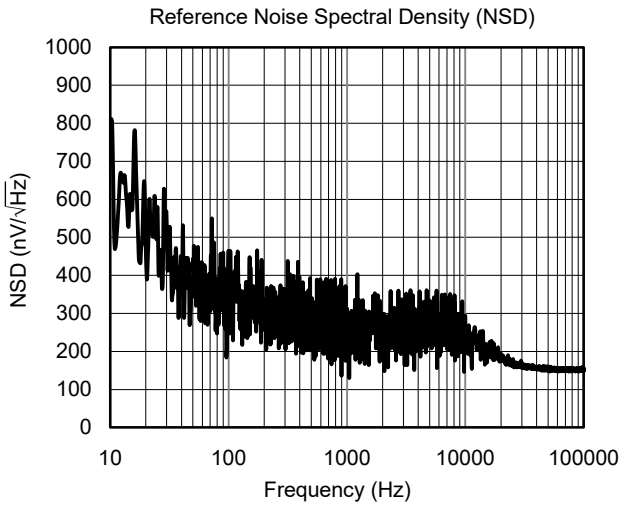


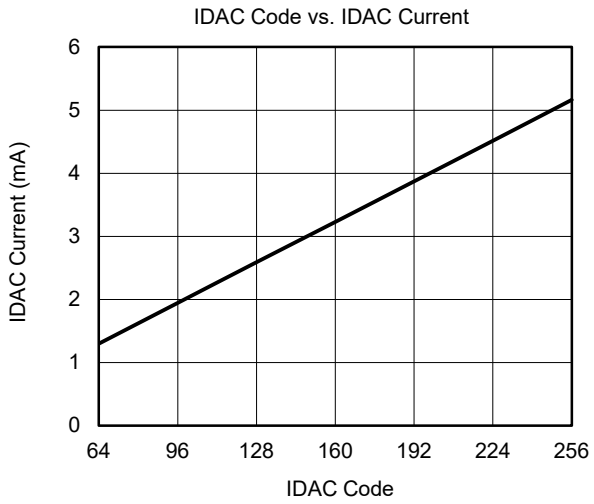
ADC Full Power Bandwidth vs. Frequency

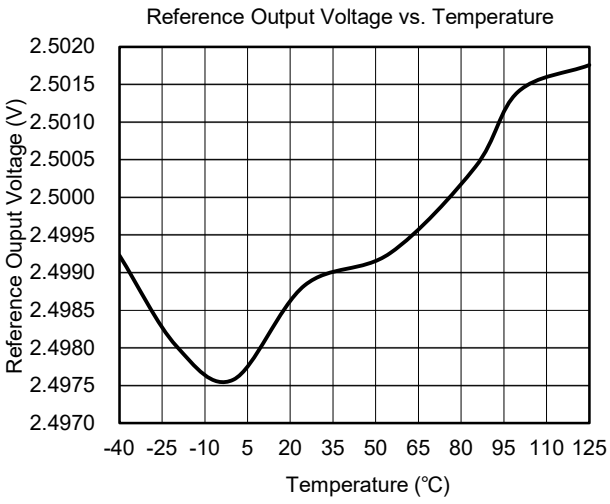


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

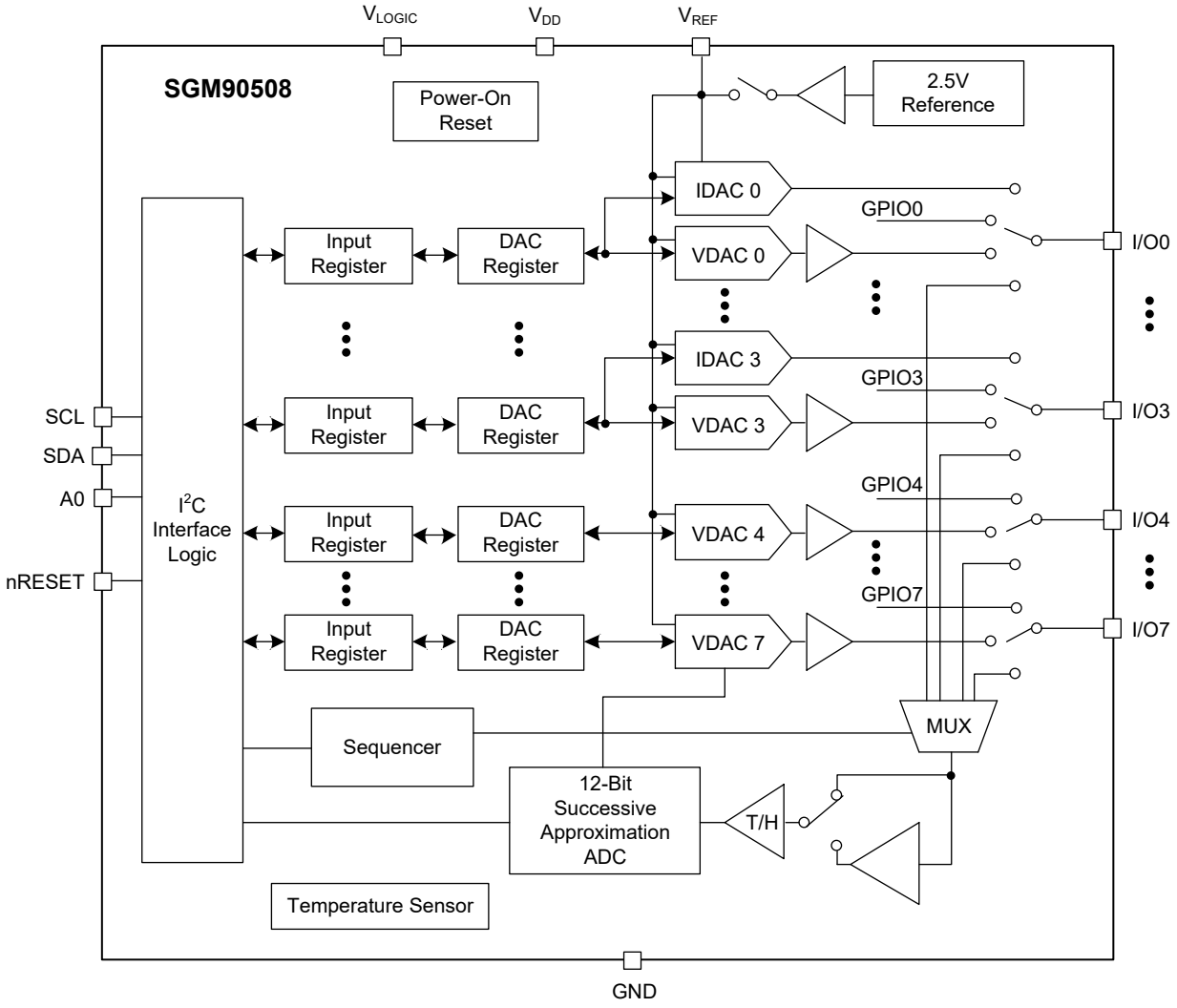








FUNCTIONAL BLOCK DIAGRAM



NOTE:
When the I/O pins are configured as GPIOs, the according input network circuit is powered by V_{DD}, and all inputs threshold and electrical limitations are restricted by V_{DD}.

Figure 2. Block Diagram

DETAILED DESCRIPTION

VDAC Section

The SGM90508 has eight 12-bit VDAC channels. The VDAC output range can be set to 0V to V_{REF} or 0V to 2 × V_{REF}. And the output range configuration is shared by all channels. The input code to the VDAC is straight binary, so the ideal output voltage can be calculated based on the following equation:

$$V_{OUT} = G \times V_{REF} \times \left(\frac{D_{IN}}{2^N} \right) \quad (1)$$

Where:

G = 1 for an output range of 0V to V_{REF} or G = 2 for an output range of 0V to 2 × V_{REF}.

V_{REF} = Voltage on the V_{REF} pin.

D_{IN} = Decimal equivalent of the binary code, which is loaded to the DAC register. It can range from 0 to 4095.

N = 12.

IDAC Section

The output range of the IDAC channels is the same whether the reference voltage is V_{REF} or 2 × V_{REF}. The input code to the IDAC is straight binary. Therefore, the ideal output current is given by

$$I_{OUT} = I_{MAX} \times \left(\frac{D_{IN}}{2^N} \right) \quad (2)$$

Where:

I_{MAX} = Current full output range, which is typically 80mA.

D_{IN} = Equal decimal code that is loaded to the DAC register. It can range from 0 to 4095.

N = 12.

ADC Section

The ADC is a fast, 12-bit, unipolar power supply, SAR ADC. Each conversion takes 2μs. The ADC input range can be configured as 0V to V_{REF} or 0V to 2 × V_{REF}. All ADC channels share the same input range. The ADC output code is straight binary format. It is possible to set an I/Ox pin as both a DAC and an ADC. In this case, the I/O is a DAC output, and at the same time, the DAC voltage can be read back by an ADC conversion and read sequence.

GPIO Section

Each I/Ox pins can be used as a GPIO pin. An output can be set by write data register. An input can be read by configuration register. When an I/Ox pin is set as an output, it is possible to read its status by setting it as an input pin at the same time as well.

When the I/O pins are configured as GPIOs, the according input network circuit is powered by V_{DD}, and all inputs threshold and electrical limitations are restricted by V_{DD}.

Internal Reference

The SGM90508 has an on-chip 2.5V reference. The internal reference is powered off by default. To enable the internal reference, the bit D9 is set in the power-down and reference control register (refer to Table 18).

Reset Function

The SGM90508 has a hardware nRESET pin. A falling edge on the nRESET pin will asynchronously reset all registers and all I/O pins to the default status. It will take the chip about 250μs (MAX) to complete the reset. It is not suggested to do any operation during this time.

The SGM90508 also has a software reset command that can perform the reset function as same as the nRESET pin.

Temperature Sensor

The SGM90508 has an integrated temperature sensor that can be used to estimate the temperature of die. The temperature conversion time is 3μs if the ADC buffer is enabled. If the buffer is disabled, the time is 3μs.

Calculation of the temperature is shown below:

When ADC gain = 1:

$$\text{Temperature}(℃) = 25 + \frac{(\text{ADC Code} - (0.56/V_{REF}) \times 4095)}{(3.015 \times (2.5/V_{REF}))} \quad (3)$$

When ADC gain = 2:

$$\text{Temperature}(℃) = 25 + \frac{(\text{ADC Code} - (0.56/(2 \times V_{REF})) \times 4095)}{(1.508 \times (2.5/V_{REF}))} \quad (4)$$

The codes range returned by the ADC is approximately 721 to 1144, and its temperature range is from -40℃ to +105℃.

DETAILED DESCRIPTION (continued)

Serial Interface

The SGM90508 has a 2-wire, I²C-compatible serial interface. The SGM90508 works as a slave device. A typical timing diagram of I²C operation sequence is shown in Figure 1. The device provides two modes: standard mode (100kHz) and fast mode (400kHz). The SGM90508 has a 7-bit slave address that six MSBs are set to 0b001000, and its LSB is set by A0 address pin.

Write Operation

An example write operation is shown in Figure 3.

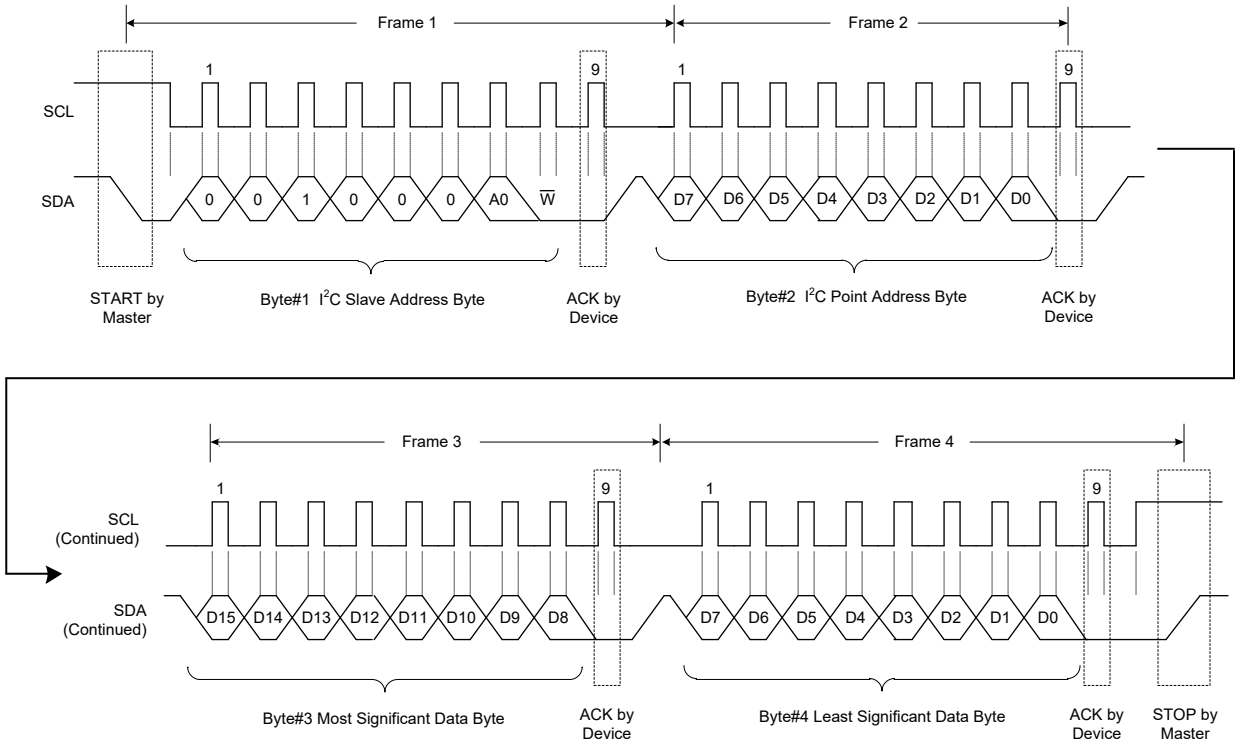


Figure 3. 4-Byte I²C Write Operation

DETAILED DESCRIPTION (continued)

Read Operation

Examples of read operation are shown in Figure 4 and Figure 5. It is also possible to perform a block readback of ADC conversions, which is shown in Figure 6.

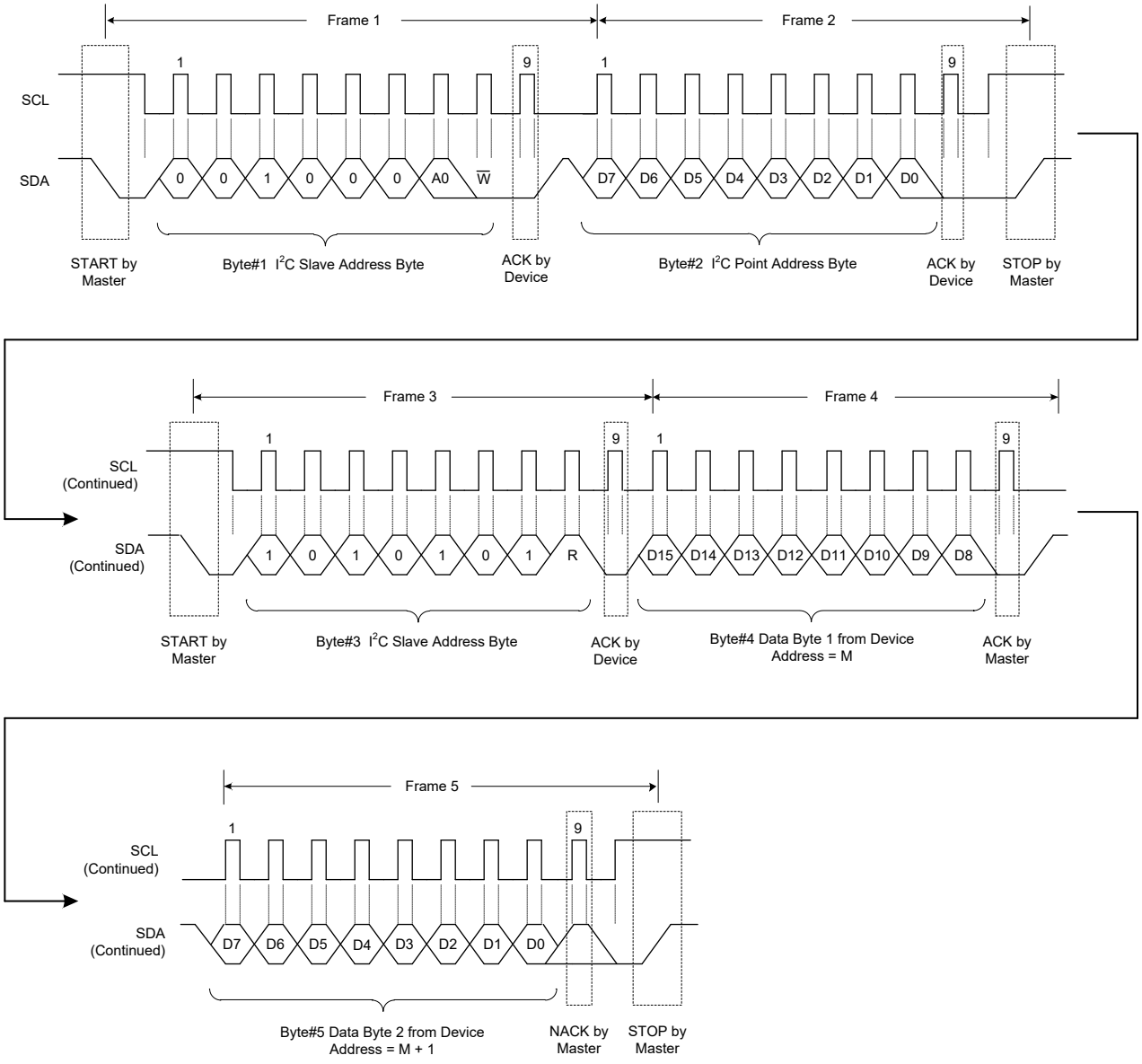


Figure 4. One 16-Bit Word Read Operation

DETAILED DESCRIPTION (continued)

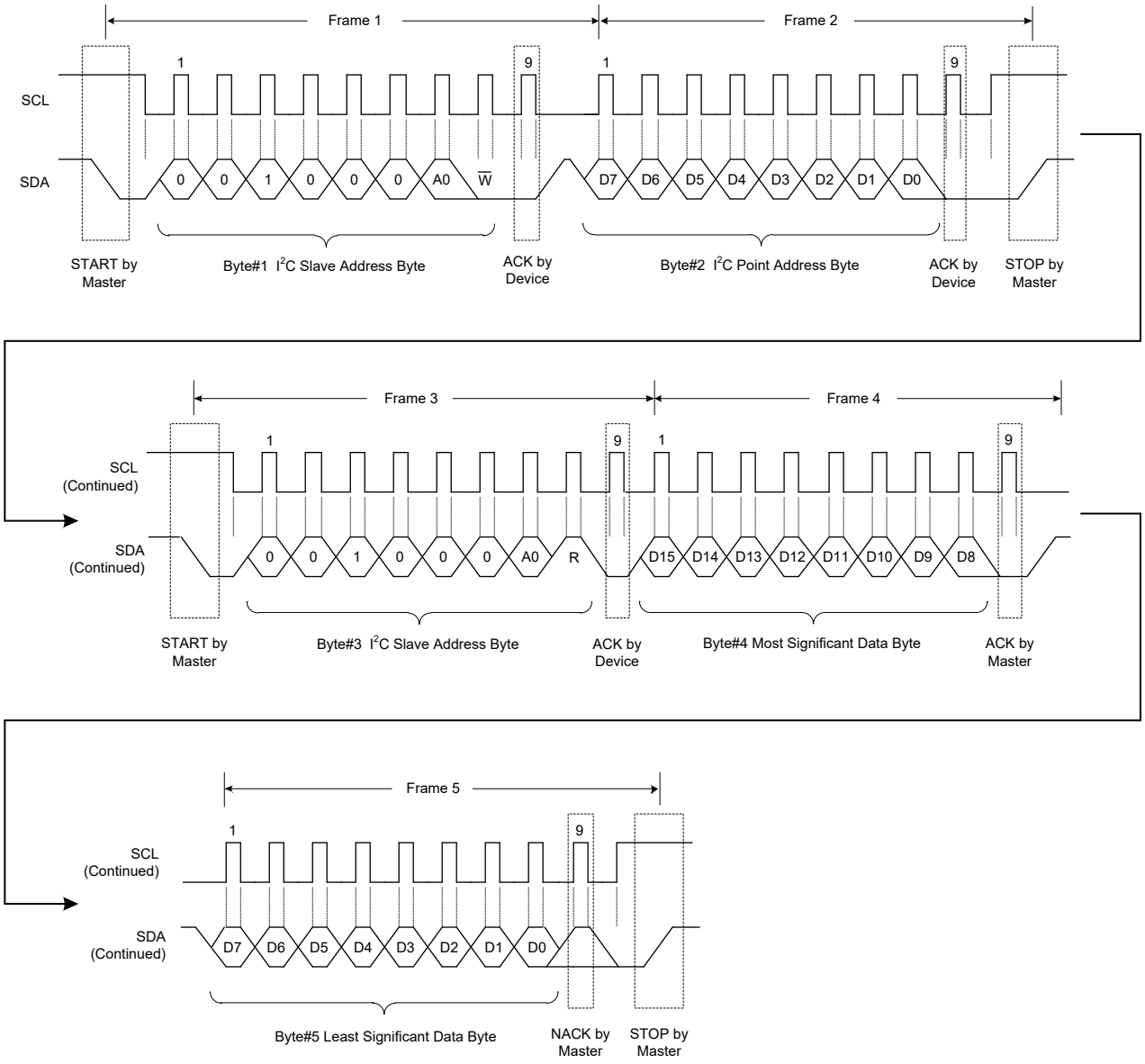
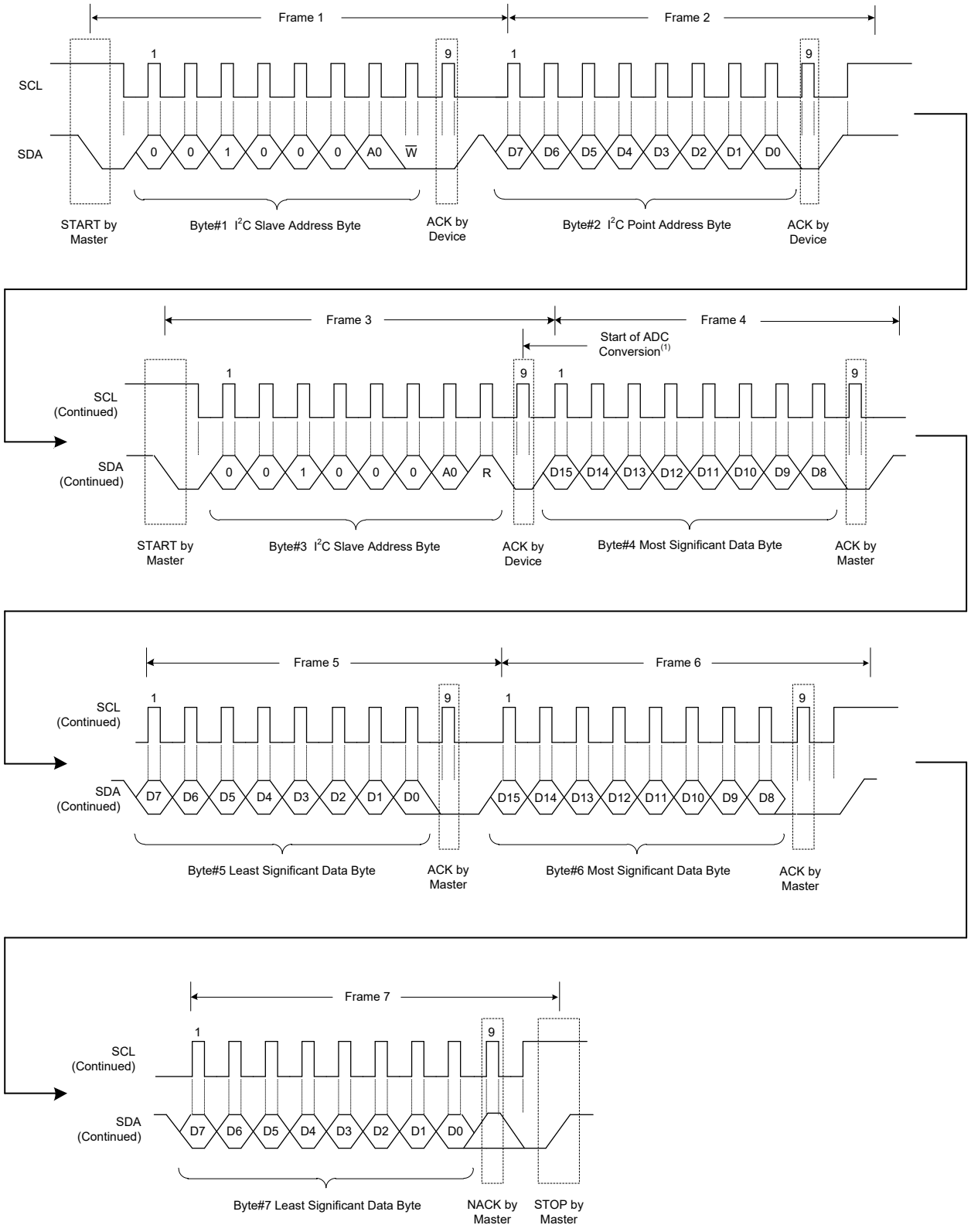


Figure 5. One 16-Bit Word Read Operation (Maintain Control of the Bus)

DETAILED DESCRIPTION (continued)



NOTE:
1. Only applicable if an ADC sequence has been selected.

Figure 6. I²C Block Read Operation

DETAILED DESCRIPTION (continued)

Pointer Byte

The pointer byte contains 8 bits.

Table 1. Pointer Byte Configuration

D7	D6	D5	D4	D3	D2	D1	D0
Mode Bits				Mode Dependent Data Bits			

Table 2. Mode Bits Details

D7	D6	D5	D4	Description
0	0	0	0	Configuration mode
0	0	0	1	DAC write (1)
0	1	0	0	ADC readback
0	1	0	1	DAC readback (2)
0	1	1	0	GPIO readback
0	1	1	1	Register readback

NOTES:
1. This write operation is both applicable when I/Ox is setting as a VDAC output or an IDAC output (IDAC is only available on I/O0 to I/O3).
2. This readback operation is both applicable when I/Ox is setting as a VDAC output or an IDAC output (IDAC is only available on I/O0 to I/O3).

DETAILED DESCRIPTION (continued)

Control Registers

The control register maps are shown in Table 3.

Table 3. Control Register Maps

Pointer Byte D[7:0]	Register Name	Description	Default Value
00000000	NOP	No operation	0x0000
00000001	IDAC Current Boost Register	Option to increase IDAC full-scale current by 10%	0x0000
00000010	ADC Sequence Register	Select ADC channels for conversion	0x0000
00000011	General-Purpose Control Register	DAC (1) and ADC control register	0x0000
00000100	ADC Pin Configuration Register	Configure pins working as ADC inputs	0x0000
00000101	VDAC Pin Configuration Register	Configure pins working as VDAC outputs	0x0000
00000110	Pull-Down Configuration Register	Configure pins with a 85kΩ pull-down resistor to GND	0x00FF
00000111	LDAC Mode Register	Configure the operation of the load DAC (1) (LDAC) function	0x0000
00001000	GPIO Write Configuration Register	Configure pins working as general-purpose outputs	0x0000
00001001	GPIO Write Data Register	Write data to the general-purpose outputs	0x0000
00001010	GPIO Read Configuration Register	Configure pins working as general-purpose inputs	0x0000
00001011	Power-Down and Reference Control Register	Power down selected DAC channels and the internal reference	0x0000
00001100	Open-Drain Configuration Register	Configure open-drain output for general-purpose output pins	0x0000
00001101	Three-State Pins	Configure which I/O pins are three-state	0x0000
00001110	IDAC Pin Configuration Register	Configure pins working as IDAC outputs	0x0000
00001111	Software Reset	Reset the SGM90508	0x0000

NOTE:
1. This operation is applicable when I/Ox is setting as a VDAC output or an IDAC output (IDAC is only available on I/O0 to I/O3).

IDAC Current Boost Register

Table 4. IDAC Current Boost Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT VALUE
D[15:9]	Reserved	Reserved, set these bits to 0.	000 0000
D[8]	IBOOST3	IDAC3 Full-Scale Boost.	0
D[7]	IBOOST2	IDAC2 Full-Scale Boost.	0
D[6]	IBOOST1	IDAC1 Full-Scale Boost.	0
D[5]	IBOOST0	IDAC0 Full-Scale Boost.	0
D[4:0]	Reserved	Reserved, set these bits to 0.	0 0000

DETAILED DESCRIPTION (continued)

General-Purpose Control Register

The general-purpose control register configures the basic working conditions of VDAC, IDAC and ADC (see Table 5). These functions include output range of VDAC (IDAC), the input range of ADC, configure the ADC buffer, and enable the pre-charge function of ADC (more details see the ADC section).

Configure the SGM90508

After power-up, the SGM90508 I/O pins are configured as 85kΩ resistors connected to GND by default. The I/O pins can be software re-configured as VDAC outputs, IDAC outputs (refer to NOTE 1 of Table 6), ADC inputs, digital outputs, digital inputs, three-state, or connected to GND with 85kΩ pull-down resistors.

An I/Ox pin can be configured as a VDAC (IDAC) (refer to NOTE 1 of Table 6) and ADC at the same time, the primary function is as a VDAC (IDAC) (refer to NOTE 1 of Table 6) and the ADC can be used to measure the voltage being provided by the VDAC (IDAC) (refer to NOTE 1 of Table 6).

Table 5. General-Purpose Control Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT VALUE
D[15:10]	Reserved	Reserved. Must be set to 0.	00 0000
D[9]	ADC Auxiliary Buffer Configuration	0 = ADC auxiliary buffer disabled (default) 1 = ADC auxiliary buffer enabled	0
D[8]	Reserved	Reserved. Must be set to 0.	0
D[7]	Lock Configuration	I/O Configuration Lock Setting 0 = The contents of the I/O pin configuration registers can be changed (default) 1 = The contents of the I/O pin configuration registers cannot be changed	0
D[6]	Write All DACs (1)	Writing All DACs Enable 0 = For the coming DAC writes, the DAC address bits determine which DAC channel is written to (default) 1 = For the coming DAC writes, the DAC address bits are ignored and all DAC channels are updated with the same data	0
D[5]	ADC Range Select	ADC Range Setting 0 = Set the ADC range 0V to V_{REF} (default) 1 = Set the ADC range 0V to 2 × V_{REF}	0
D[4]	DAC Range Select (1)	DAC Range Setting 0 = Set the DAC range 0V to V_{REF} (default) 1 = Set the DAC range 0V to 2 × V_{REF}	0
D[3:0]	Reserved	Reserved. Must set these bits to 0.	0000

NOTE:
1. This operation is applicable when I/Ox is setting as a VDAC output or an IDAC output (IDAC is only available on I/O0 to I/O3).

Table 6. I/O Pin Configuration Register Format (2)

D7	D6	D5	D4	D3	D2	D1	D0
I/O7	I/O6	I/O5	I/O4	I/O3 (1)	I/O2 (1)	I/O1 (1)	I/O0 (1)

NOTES:
1. IDACx is only available on I/O0 to I/O3.
2. After configuring the function (VDAC, IDAC, ADC and GPIO) Configuration Register, setting the corresponding bits in I/O Pin Configuration Registers to '1' that enable the function on the selected I/O pins.

DETAILED DESCRIPTION (continued)

An Example of Configuring I/O Pin as VDACs

In the following example, I/O1 and I/O7 are configured as VDACs.

1. The first byte is composed of 7-bit chip address and 1-bit writing bit.
2. The second byte is pointer address byte 0b00000101 (VDAC pin configuration register).
3. The third byte is the most significant data byte (0b00000000) to be written to target register (VDAC pin configuration register).
4. The forth byte is the least significant data byte (0b10000010) to be written to target register (VDAC pin configuration register).

An Example of Configuring I/O Pin as IDACs

In the following example, I/O0 and I/O3 are configured as IDACs.

1. The first byte is composed of 7-bit chip address and 1-bit writing bit.
2. The second byte is pointer address byte 0b00001110 (IDAC pin configuration register).
3. The third byte is the most significant data byte (0b00000000) to be written to target register (IDAC pin configuration register).
4. The forth byte is the least significant data byte (0b00001001) to be written to target register (IDAC pin configuration register).

DAC (VDAC and IDAC) Write Operation

The data is written to a DAC when the mode bits (bits D[7:4]) of the pointer byte are 0b0001 (see Table 2). Bits D[2:0] determine which DAC is addressed. This operation is both applicable, when I/Ox is setting as a VDAC output or an IDAC output (IDAC is only available on I/O0 to I/O3).

LDAC (VDAC and IDAC) Mode Operation

This operation is applicable when I/Ox is setting as a VDAC output or an IDAC output (IDAC is only available on I/O0 to I/O3).

Table 7. LDAC Mode Register

D1	D0	LDAC Mode
0	0	Data written to an input register is immediately copied to a DAC register, and the DAC output updates (default).
0	1	Data written to an input register is not copied to a DAC register. The DAC output is not updated.
1	0	Data in the input registers is copied to the corresponding DAC registers. After the data transfer is completed, the DAC outputs are updated simultaneously.
1	1	Reserved.

DETAILED DESCRIPTION (continued)

DAC (VDAC and IDAC) Readback

The input register of each DAC can be read back via the I²C interface. The data can be read back from a DAC only when there is not an ADC conversion sequence taking place.

In a DAC data register readback sequence, the second byte is the point address byte. The point byte is composed of 0b0101 (D[7:3]) and the bit D[3:0] that select the DAC channel to be read back. And when the 16-bit data of DAC data register is read back, the first 4-bit is '0b1xxx', and the following 12-bit is the register data (the data format is shown in Table 9). The D[15] bit is set to '1' which indicates that this is a result the DAC register. The D[14:12] shows the DAC register address.

An Example of DAC Input Register Readback

The data in the DAC2 input register can be read back in the following examples.

1. The first byte is composed of 7-bit chip address and 1-bit writing bit.
2. The second byte is pointer address byte 0b01010010 (pointer address = 0b0101 + DAC2 address).
3. The third byte is composed of 7-bit chip address and 1-bit reading bit.
3. The forth byte is the most significant data byte of the readback 16-bit data (MSB byte = 1-bit 0b1 + 3-bit DAC2 address + 4-bit MSB of 12-bit DAC data).
4. The fifth byte is the least significant data byte of the readback 16-bit data (LSB byte = 8-bit data of 12-bit DAC data).

IDAC Enable and Write Operation

The SGM90508 has 4 channels IDAC outputs, it can be enabled by setting IDAC configuration register according bit.

Table 8. DAC Pointer Byte Address

DAC Address	D7	D6	D5	D4	D3	D2	D1	D0
DAC0 (1)	0	0	0	1	0	0	0	0
DAC1 (1)	0	0	0	1	0	0	0	1
DAC2 (1)	0	0	0	1	0	0	1	0
DAC3 (1)	0	0	0	1	0	0	1	1
DAC4	0	0	0	1	0	1	0	0
DAC5	0	0	0	1	0	1	0	1
DAC6	0	0	0	1	0	1	1	0
DAC7	0	0	0	1	0	1	1	1

NOTE:
1. This operation is applicable when I/Ox is setting as a VDAC output or an IDAC output (IDAC is only available on I/O0 to I/O3).

Table 9. DAC Data Register Format

MSB LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	DAC Address			12-Bit DAC Data											

DETAILED DESCRIPTION (continued)

ADC Operation

If SGM90508 works as a multi-channel ADC, it works as same as a traditional multi-channel ADC with a multiplexer switching the inputs. Each serial current data transfer selects the next channel for conversion. Before start a conversion, the ADC sequence register must be set (as show in Table 10 and Table 11). In the ADC sequence register, the REP bit can be set to let the ADC repeat the conversion sequence.

After the sequence register setting is completed, the ADC begins to process the first channel in sequence. ADC data can be read out by any available format, if multi-channel is enabled, block reading is more efficient.

If multi-channel is enabled, the ADC converts all enabled channels in ascending order. Conversion is triggered by the rising edge of SCL at the acknowledge (ACK) before the MSB.

If REP bit is enabled in ADC sequence register, the ADC will repeat the conversion sequence if all the selected channels have been converted. If REP bit is cleared during the cycle, the ADC will finish the current conversion and send out the result in subsequent I²C ADC data reading.

The ADC conversion result of one channel is a 16-bit format data. The D[15] bit is set to '0' which indicates that this is an ADC result data. The D[14:12] shows the ADC channel address. The following 12-bit D[11:0] is the ADC data (the data format is shown in Table 11).

In the section of An Example of Configuring the ADC for Conversion, shows the example of how to configure I/O7 and I/O0 and read ADC conversion result.

The ADC sequence can be re-configured if there is not an on-going conversion. When a new ADC sequence is set, ADC ignores all to be converted channels which are selected in previous setting and will start in new sequence immediately. Clear the REP, TEMP and according ADC selected bits can stop the ADC conversion sequence.

Table 10. ADC Sequence Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT VALUE
D[15:11]	Reserved	Reserved. Must be set to 0.	0 0000
D[10]	V_{DD} Monitor Enable	V_{DD} Monitor Enable 0 = V_{DD} monitor disable (default) 1 = V_{DD} monitor enable, V_{DD}/4 will be converted by ADC, the result can be read by ADC data register, more details refer to Table 11	0
D[9]	REP	ADC Sequence Repetition 0 = Sequence repetition disabled (default) 1 = Sequence repetition enabled	0
D[8]	TEMP	Include Temperature Sensor Sampling in ADC Sequence 0 = Disable temperature sensor readback (default) 1 = Enable temperature sensor readback	0
D[7:0]	ADC[7:0]	Set corresponding bits to '1' enable the appropriate ADC channel in the conversion sequence. Default all are '0'.	0000 0000

Table 11. ADC Data Register Format

MSB LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	ADC Address (1)			12-Bit ADC Data											
1	000 (2)			12-Bit Temperature Sensor Channel Data											
1	001 (3)			12-Bit V_{DD}/4 Channel Data											

NOTES:
1. When D[15] = 0, the ADC addresses are as follows: 000 = ADC0, …, 111 = ADC7.
2. When D[15:12] = 1000, ADC result is internal temperature sensor sampling data.
3. When D[15:12] = 1001, ADC result is V_{DD}/4 sampling data.

DETAILED DESCRIPTION (continued)

An Example of Configuring the ADC for Conversion

In the following example, the ADC7 and ADC0 are configured for the ADC conversion sequence.

The first step is setting I/O7 and I/O0 for ADC (configure ADC pin configuration register).

1. The first byte is composed of 7-bit chip address and 1-bit writing bit.
2. The second byte is pointer address byte 0b00000100 (ADC pin configuration register).
3. The third byte is the most significant data byte (0b00000000) to be written to target register (ADC pin configuration register).
4. The forth byte is the least significant data byte (0b10000001) to be written to target register (ADC Pin Configuration register).

The second step is setting ADC7 and ADC0 for ADC (configure ADC sequence register).

1. The first byte is composed of 7-bit chip address and 1-bit writing bit.
2. The second byte is pointer address byte 0b00000010 (ADC sequence register).
3. The third byte is the most significant data byte (0b00000010) to be written to target register (ADC sequence register).
4. The forth byte is the least significant data byte (0b10000001) to be written to target register (ADC sequence register).

The third step is selecting ADC7 for ADC readback (configure ADC readback) and read ADC data by block read.

1. The first byte is composed of 7-bit chip address and 1-bit writing bit.
2. The second byte is pointer address byte 0b01000000 (ADC address ADC7).
3. The third byte is composed of 7-bit chip address and 1-bit reading bit.
4. The forth byte is the MSB byte of ADC7 conversion result (MSB byte = 1-bit 0b0 + 3-bit ADC7 address + 4-bit MSB of 12-bit ADC7 data).
5. The fifth byte is the LSB byte of ADC7 conversion result (LSB byte = 8-bit data of 12-bit ADC7 data).
6. If continuously read, the sixth byte is the MSB byte of ADC0 conversion result (MSB byte = 1-bit 0b0 + 3-bit ADC0 address + 4-bit MSB of 12-bit ADC0 data).
7. If continuously read, the seventh byte is the LSB byte of ADC0 conversion result (LSB byte = 8-bit data of 12-bit ADC0 data).

And so on, repeating 4 ~ 7 operations. If the reading does not stop, the data of ADC7 and ADC0 will keep being updated and reported.

GPIO Operation

Each of I/Ox pins of the SGM90508 can be configured as a general-purpose digital input or output pin.

Setting Pins as Inputs

To set an I/Ox pin as a general-purpose input, set the according bit in the GPIO read configuration register to 1.

DETAILED DESCRIPTION (continued)

Setting Pins as Outputs

Table 12. GPIO Write Configuration Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT VALUE
D[15:8]	Reserved	Reserved. These bits must be set to 0.	0000 0000
D[7:0]	GPIO7 to GPIO0	Select I/Ox Pins as GPIO Outputs 0 = I/Ox function depends on the pin configuration registers (default) 1 = I/Ox is a general-purpose output pin	0000 0000

Table 13. GPIO Open-Drain Control Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT VALUE
D[15:8]	Reserved	Reserved. These bits must be set to 0.	0000 0000
D[7:0]	Open-Drain 7 to Open-Drain 0	Sets Output Pins as Open-Drain 0 = I/Ox is a push/pull output pin (default) 1 = I/Ox is an open-drain output pin	0000 0000

Table 14. GPIO Write Data Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT VALUE
D[15:8]	Reserved	Reserved. These bits must be set to 0.	0000 0000
D[7:0]	GPIO7 to GPIO0	Sets the State of a GPIO Output 0 = I/Ox output logic low (default) 1 = I/Ox output logic high	0000 0000

Three-State Pins

Table 15. Three-State Configuration Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT VALUE
D[15:8]	Reserved	Reserved. These bits must be set to 0.	0000 0000
D[7:0]	TSO[7:0]	Set Pins as Three-State Outputs 0 = I/Ox function depends on the pin configuration registers (default) 1 = I/Ox is a three-state output pin	0000 0000

85kΩ Pull-Down Resistor Pins

Table 16. Pull-Down Configuration Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT VALUE
D[15:8]	Reserved	Reserved. These bits must be set to 0.	0000 0000
D[7:0]	Pull_Down[7:0]	Set Pins as Weak Pull-Down Outputs 0 = I/Ox function depends on the pin configuration registers 1 = I/Ox is connected to GND through an 85kΩ pull-down resistor (default)	1111 1111

IDAC Configure Register

Table 17. IDAC Configuration Register Details (Address: 0xE)

BITS	BIT NAME	DESCRIPTION	DEFAULT VALUE
D[7:4]	Reserved	Reserved. Set these bits to 0.	0000
D[3]	IDAC3_EN	When IDACx is enabled, voltage output will be disabled automatically. IDACx has higher priority than VDAC. 2x output range bit is not effective with IDAC.	
D[2]	IDAC2_EN		
D[1]	IDAC1_EN		
D[0]	IDAC0_EN		

DETAILED DESCRIPTION (continued)

Power-Down and Reference Control

The SGM90508 has a power-down and reference control register, and it can power down internal reference and DACs (see Table 18). There is no dedicated control for the ADC power-down, but the ADC is automatically powered down if there is no an ADC operation.

Reset Function

The SGM90508 can be reset by setting the reset register (pointer byte = 0b00001111). This operation resets all registers to the default values.

The SGM90508 can be reset to its default conditions by writing 0x0DAC to the reset register (pointer byte = 0b00001111). This resets all registers to the default values and reconfigures the I/Ox pins to their default values (85kΩ pull-down to GND).

Table 18. Power-Down and Reference Control Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT VALUE
D[15:11]	Reserved	Reserved. These bits must be set to 0.	0 0000
D[10]	PD_ALL	Power-Down DACs and Internal Reference 0 = The power-down states of the reference and DACs depend on D[9] and D[7:0] bits (default) 1 = The reference, the DACs, and the ADC are powered down	0
D[9]	EN_REF	Enable Internal Reference 0 = The reference and its buffer are powered down (default). Set this bit if an external reference is used (default) 1 = The reference and its buffer are powered on. The reference is available on the V_{REF} pin	0
D[8]	Reserved	Reserved. Must be set to 0.	0
D[7:0]	PD[7:0]	Power-Down DACs 0 = The channel is in normal operating mode (default) 1 = The channel is powered down if it is configured as a DAC	0000 0000

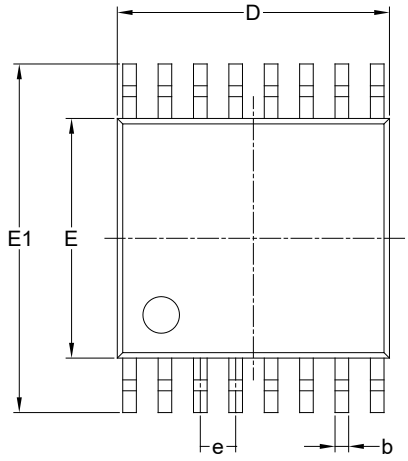
REVISION HISTORY

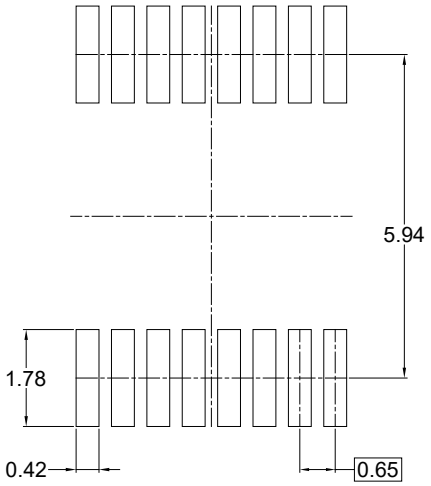
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (DECEMBER 2023) to REV.A	Page
Changed from product preview to production data	All

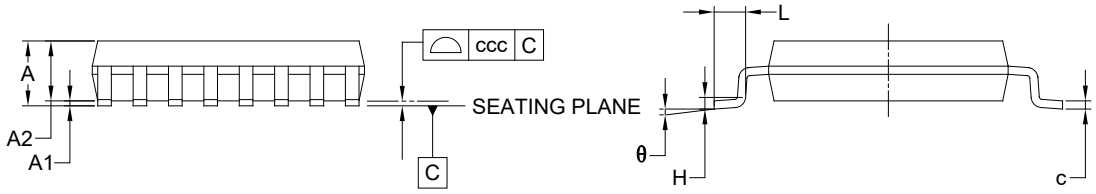
PACKAGE OUTLINE DIMENSIONS

TSSOP-16





RECOMMENDED LAND PATTERN (Unit: mm)

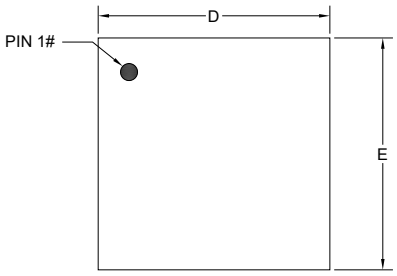


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	4.860	-	5.100
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

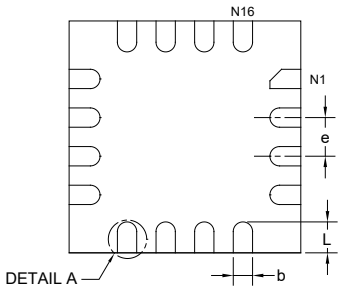
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

PACKAGE OUTLINE DIMENSIONS

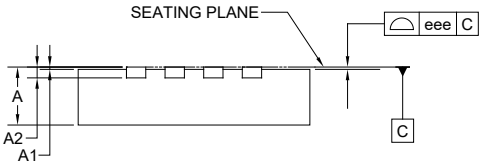
TQFN-3×3-16BL



TOP VIEW

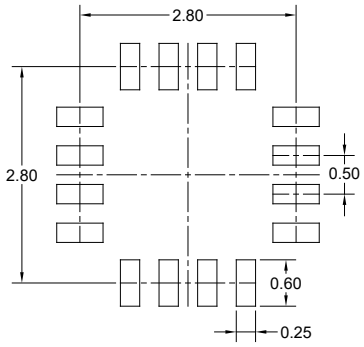


BOTTOM VIEW



SIDE VIEW

DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



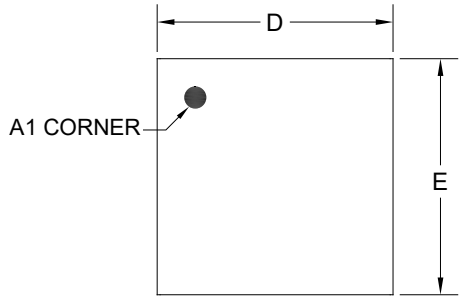
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	-	0.800
A1	-0.004	-	0.050
A2	0.110 REF		
b	0.200	-	0.300
D	2.900	-	3.100
E	2.900	-	3.100
e	0.500 BSC		
L	0.300	-	0.500
eee	0.080		

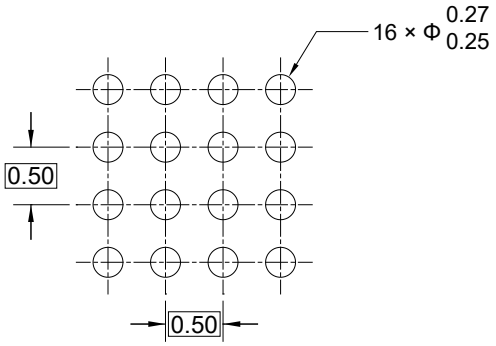
NOTE: This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

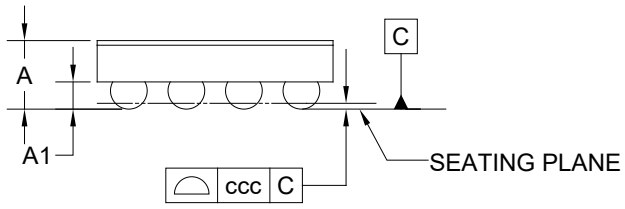
WLCSP-2.05×2.05-16B



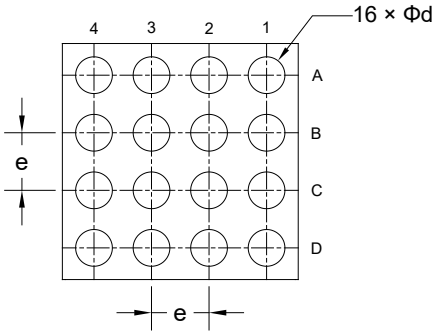
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



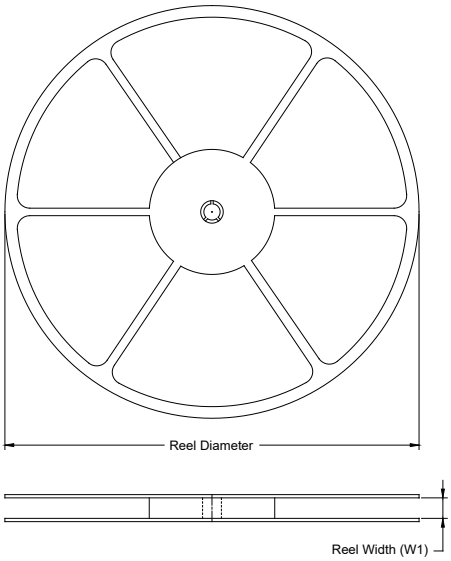
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	0.633
A1	0.216	-	0.256
D	2.020	-	2.080
E	2.020	-	2.080
d	0.289	-	0.349
e	0.500 BSC		
ccc	0.050		

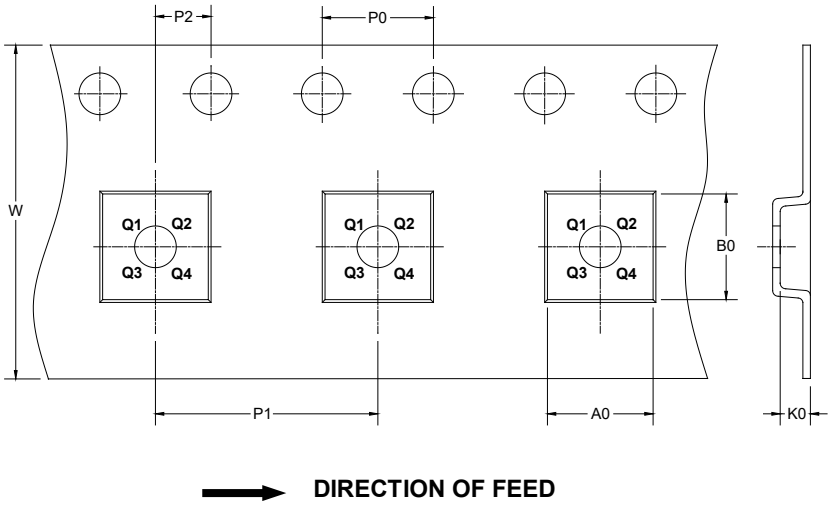
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



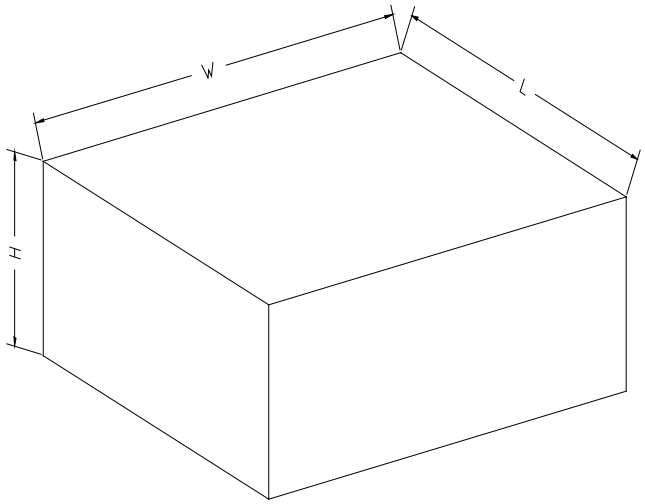
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-16	13″	12.4	6.80	5.40	1.50	4.0	8.0	2.0	12.0	Q1
TQFN-3×3-16BL	13″	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q2
WLCSP-2.05×2.05-16B	7″	9.5	2.24	2.24	0.75	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002