ESD7008, SZESD7008

ESD Protection Diode

Low Capacitance ESD Protection Diode for High Speed Data Line

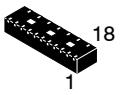
The ESD7008 ESD protection diode is designed specifically to protect four high speed differential pairs. Ultra−low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines. The flow−through style package allows for easy PCB layout and matched trace lengths necessary to maintain consistent impedance for the high speed lines.

Features

- Integrated 4 Pairs (8 Lines) High Speed Data
- Single Connect, Flow through Routing
- Low Capacitance (0.12 pF Typical, I/O to GND)
- Protection for the Following IEC Standards:
  IEC 61000−4−2 Level 4
- UL Flammability Rating of 94 V−0
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- This is a Pb−Free Device

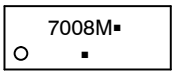
Typical Applications

- V−by−One HS
- Thunderbolt (Light Peak)
- USB 3.0
- HDMI
- Display Port
- LVDS



UDFN18
CASE 517BV

MARKING DIAGRAM



7008 = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping
ESD7008MUTAG	UDFN18 (Pb−Free)	3000 / Tape & Reel
SZESD7008MUTAG	UDFN18 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	−55 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Seconds)	T_L	260	°C
IEC 61000−4−2 Contact (ESD) IEC 61000−4−2 Air (ESD)	ESD ESD	±15 ±15	kV kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

See Application Note AND8308/D for further description of survivability specs.

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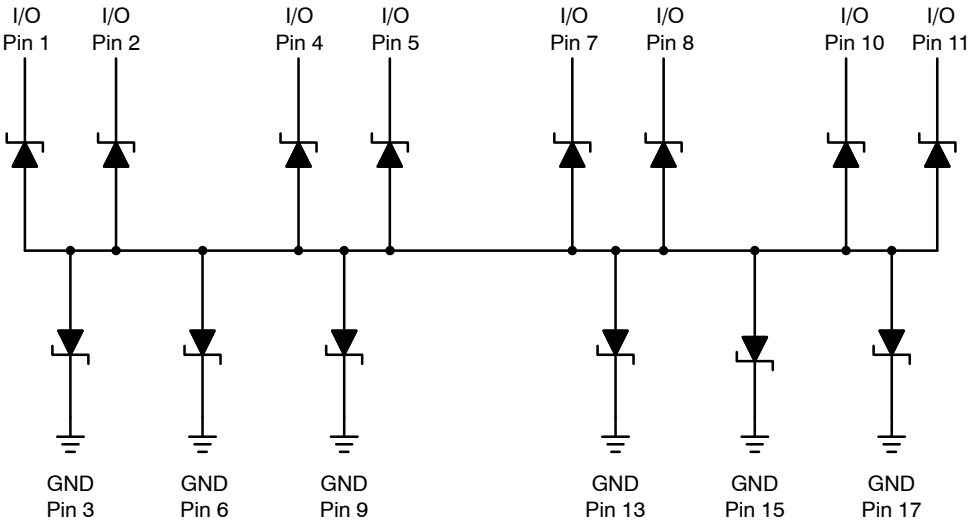


Note: Only Minimum of 1 GND connection required

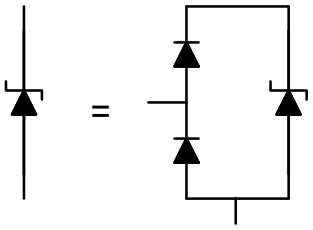


Figure 1. Pin Schematic

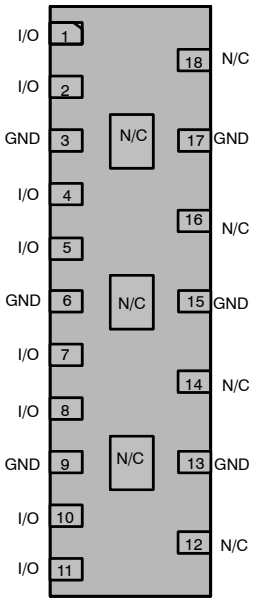


Figure 2. Pin Configuration

Note: Only minimum of one pin needs to be connected to ground for functionality of all pins. All pins labeled “N/C” should have no electrical connection.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	I/O Pin to GND (Note 1)			5.0	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, I/O Pin to GND	5.5	6.7		V
Reverse Leakage Current	I_R	V_{RWM} = 5 V, I/O Pin to GND			1.0	μA
Clamping Voltage (Note 1)	V_C	I_{PP} = 1 A, I/O Pin to GND (8 x 20 μs pulse)			10	V
Clamping Voltage (Note 2)	V_C	IEC61000−4−2, ±8 kV Contact	See Figures 3 and 4			V
Clamping Voltage TLP (Note 3) See Figures 8 through 11	V_C	I_{PP} = ±8 A I_{PP} = ±16 A		13.2 18.2		
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz between I/O Pins and GND		0.12	0.15	pF
Junction Capacitance Difference	ΔC_J	V_R = 0 V, f = 1 MHz between I/O Pins and GND		0.02		pF

1. Surge current waveform per Figure 7.
2. For test procedure see Figures 5 and 6 and application note AND8307/D.
3. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
   TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 4 ns, averaging window; t_1 = 30 ns to t_2 = 60 ns.

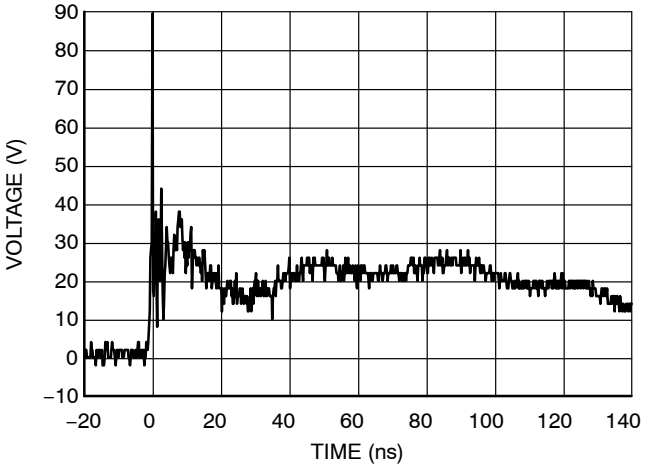


Figure 3. IEC61000−4−2 +8 KV Contact Clamping Voltage

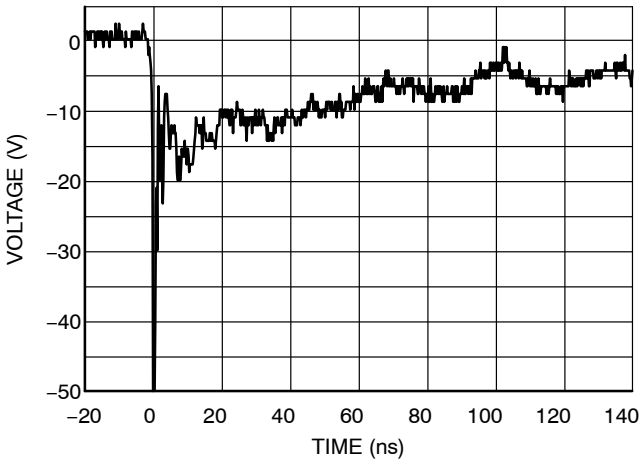


Figure 4. IEC61000−4−2 −8 KV Contact Clamping Voltage

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

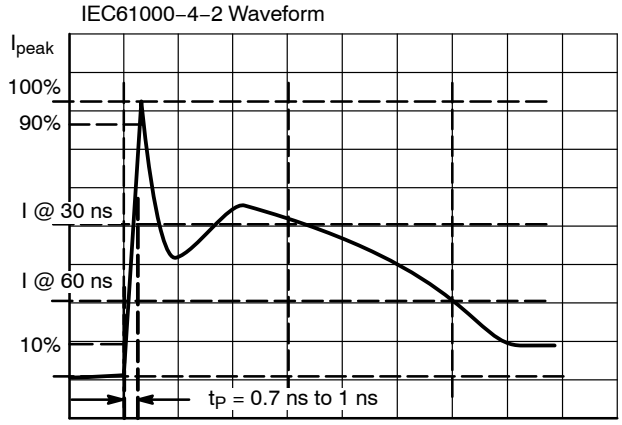


Figure 5. IEC61000−4−2 Spec

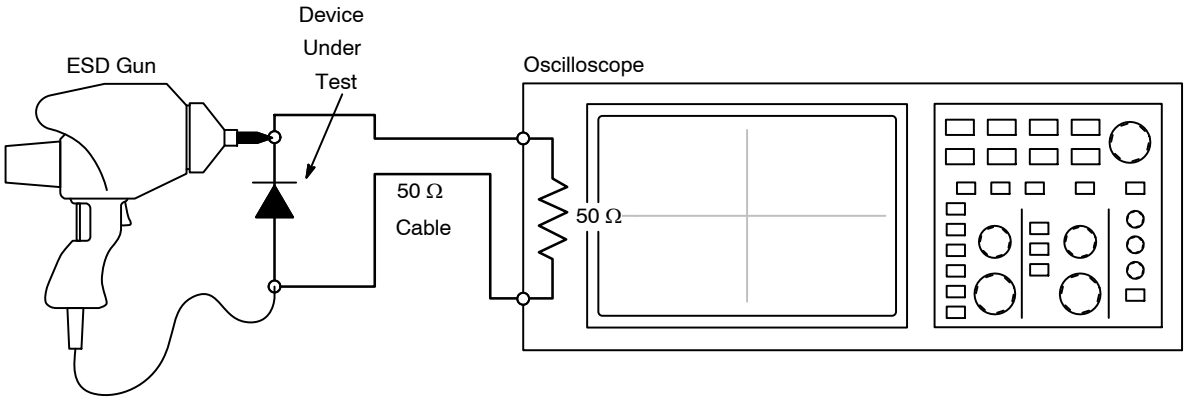


Figure 6. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

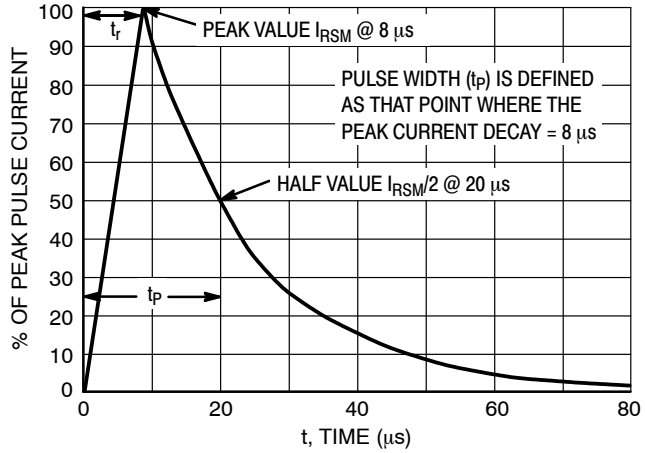


Figure 7. 8 x 20 μs Pulse Waveform

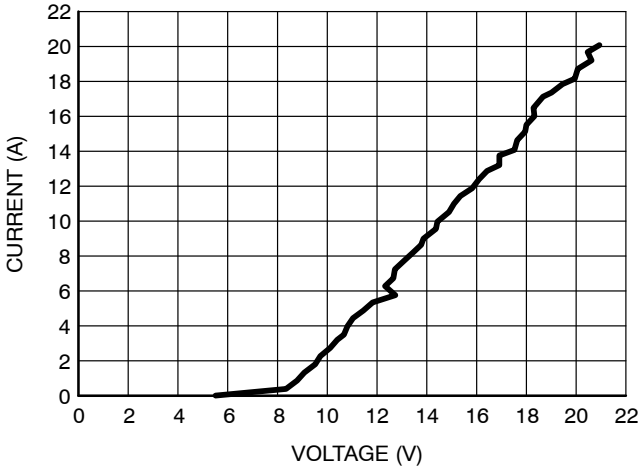


Figure 8. Positive TLP I−V Curve

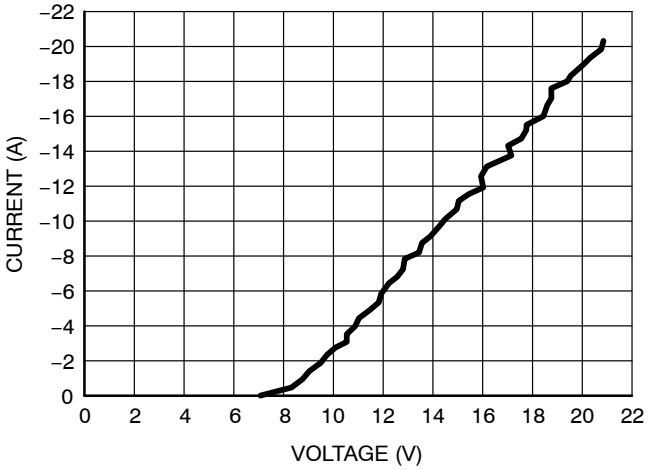


Figure 9. Negative TLP I−V Curve

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 10. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 11 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

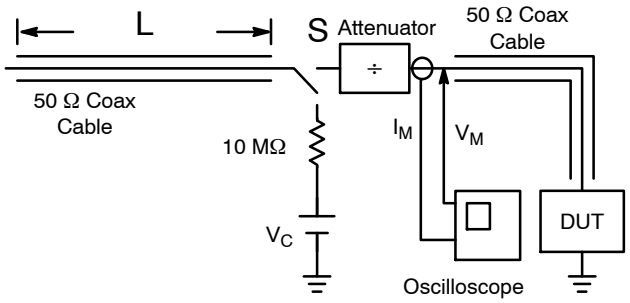


Figure 10. Simplified Schematic of a Typical TLP System

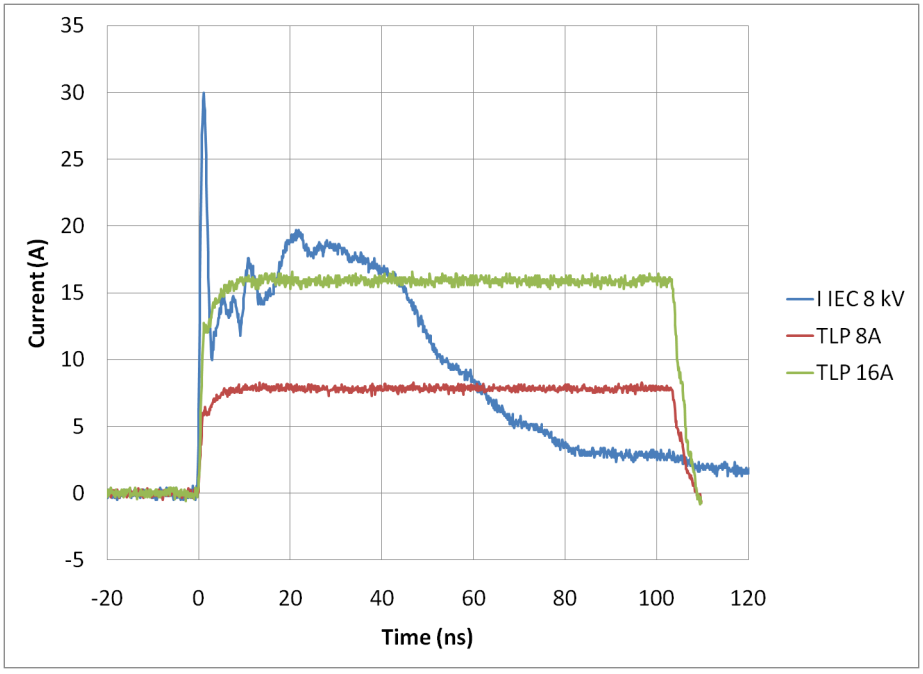
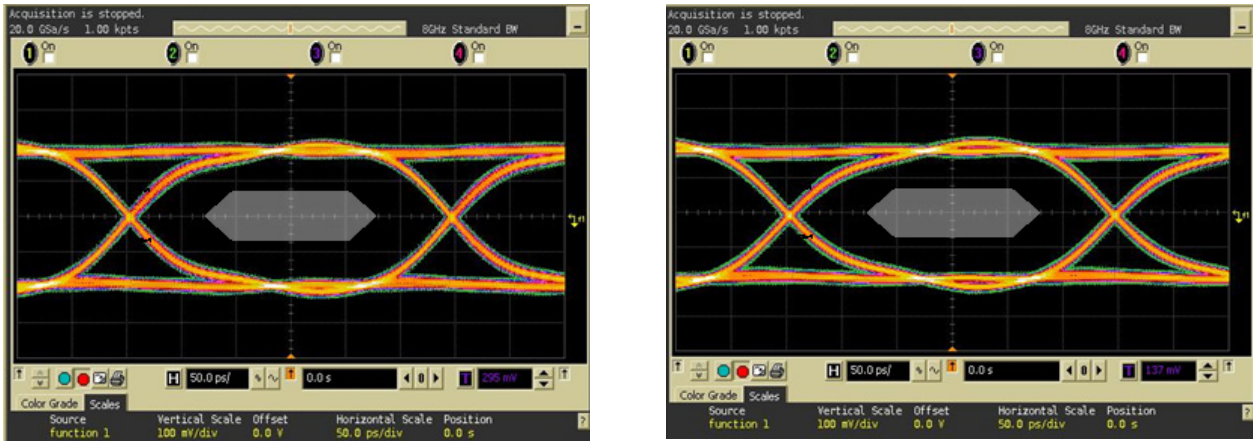


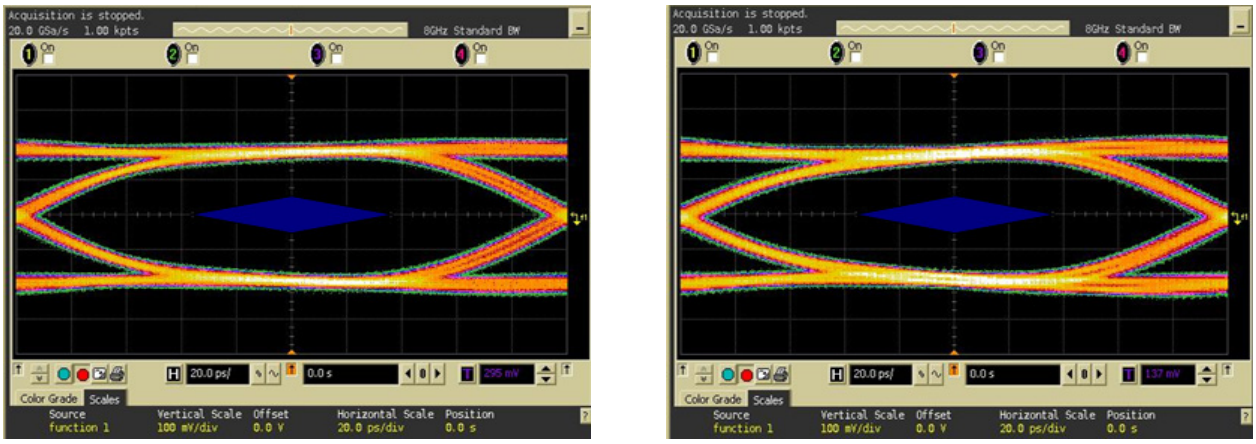
Figure 11. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms



Without ESD

With ESD7008

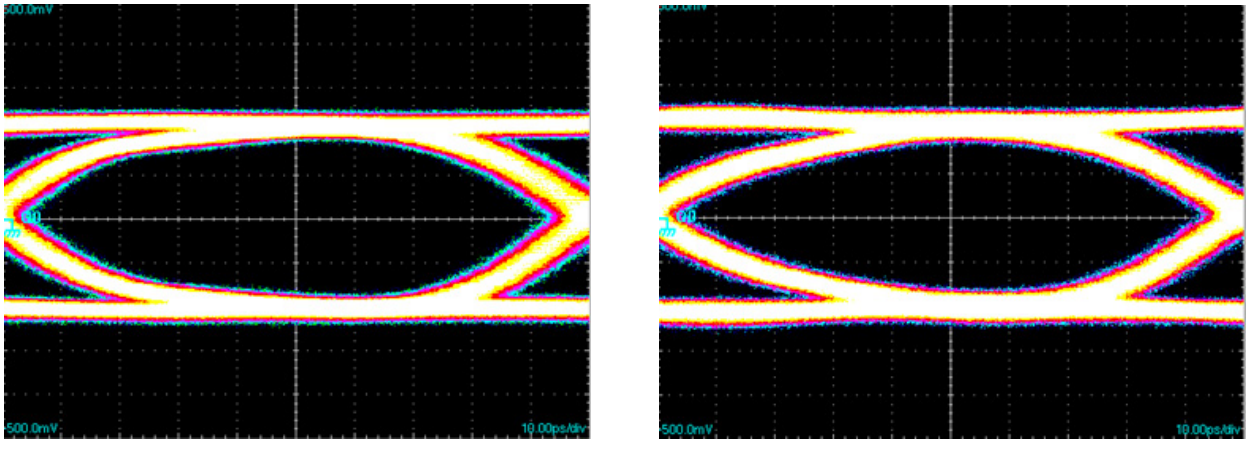
Figure 12. HDMI1.4 Eye Diagram with and without ESD7008. 3.4 Gb/s, 400 mV_{PP}



Without ESD

With ESD7008

Figure 13. USB3.0 Eye Diagram with and without ESD7008. 5.0 Gb/s, 400 mV_{PP}



Without ESD

With ESD7008

Figure 14. Thunderbolt Eye Diagram with and without ESD7008. 10 Gb/s, 400 mV_{PP}

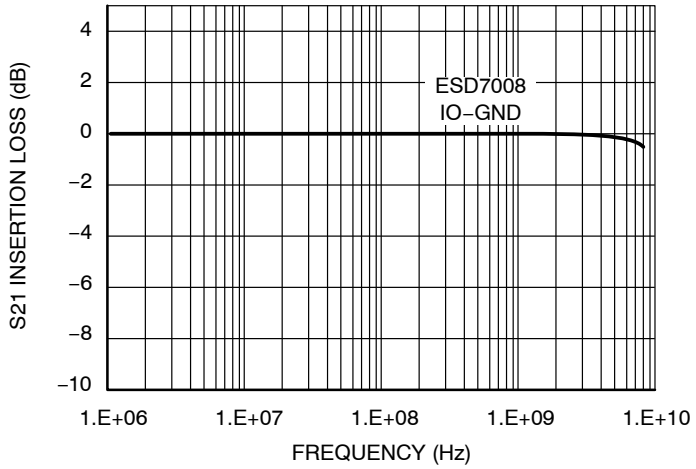


Figure 15. ESD7008 Insertion Loss

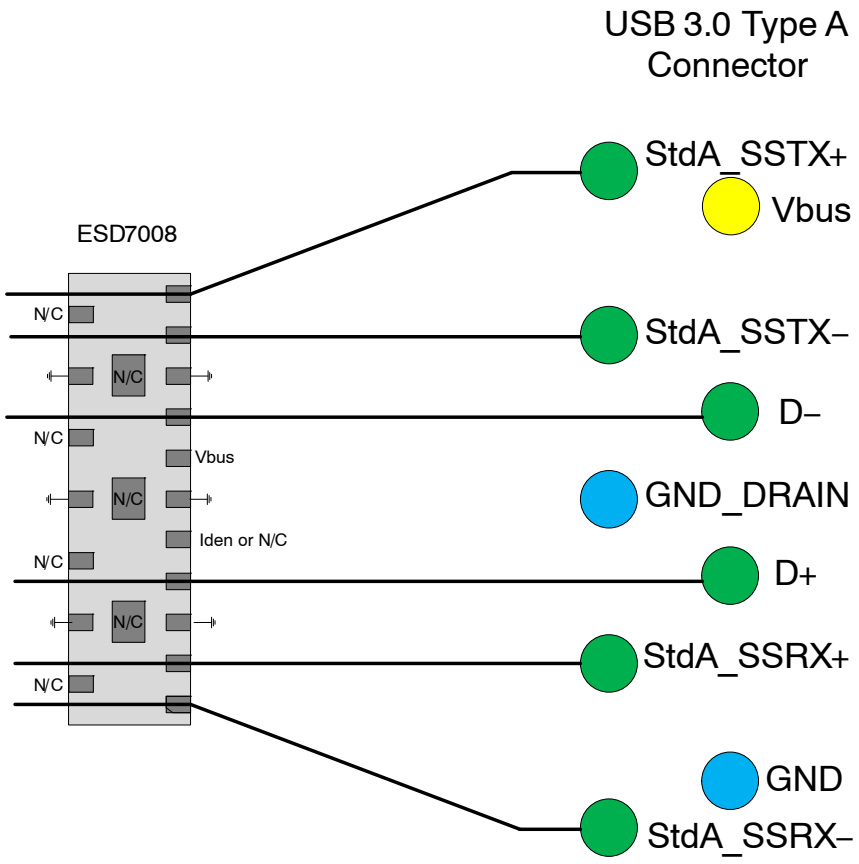


Figure 16. USB3.0 Layout Diagram

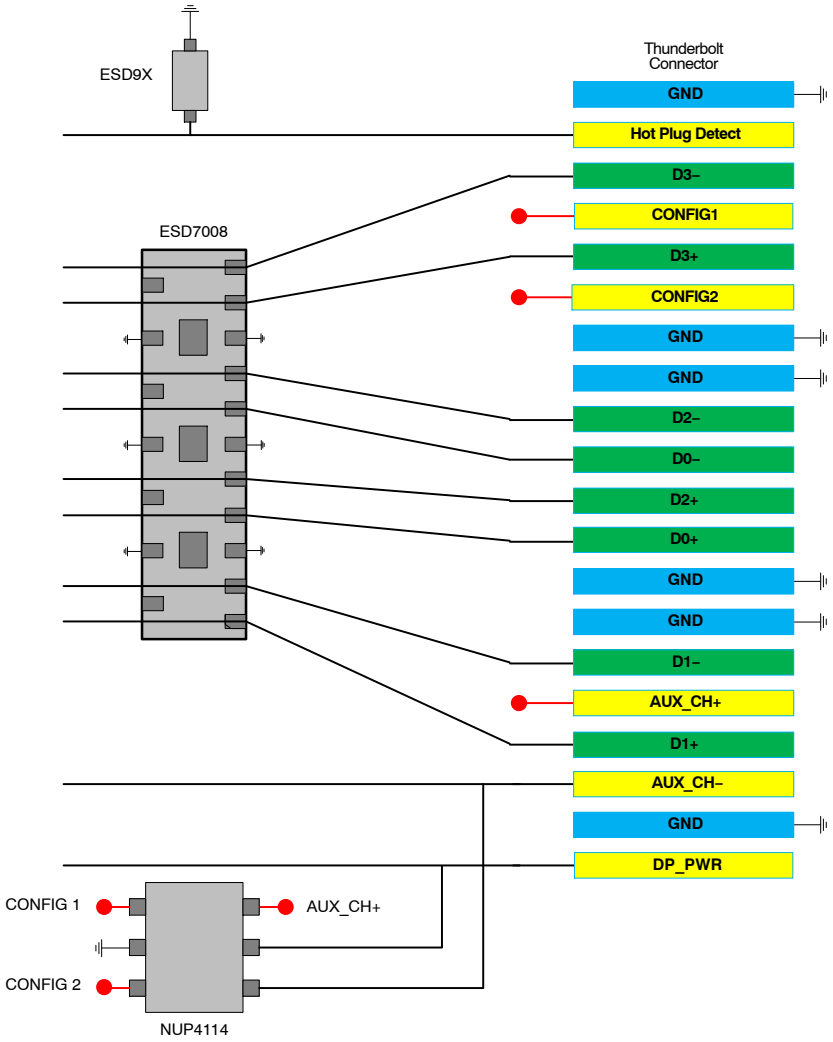


Figure 17. Thunderbolt Layout Diagram

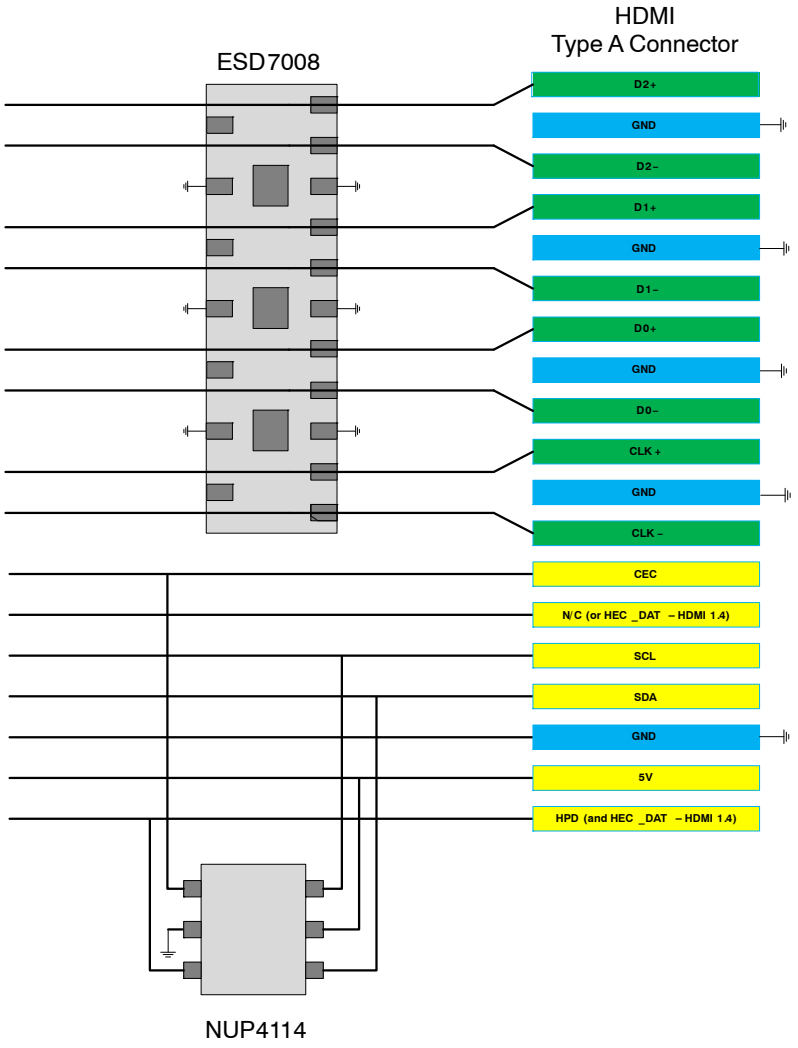


Figure 18. HDMI Layout Diagram

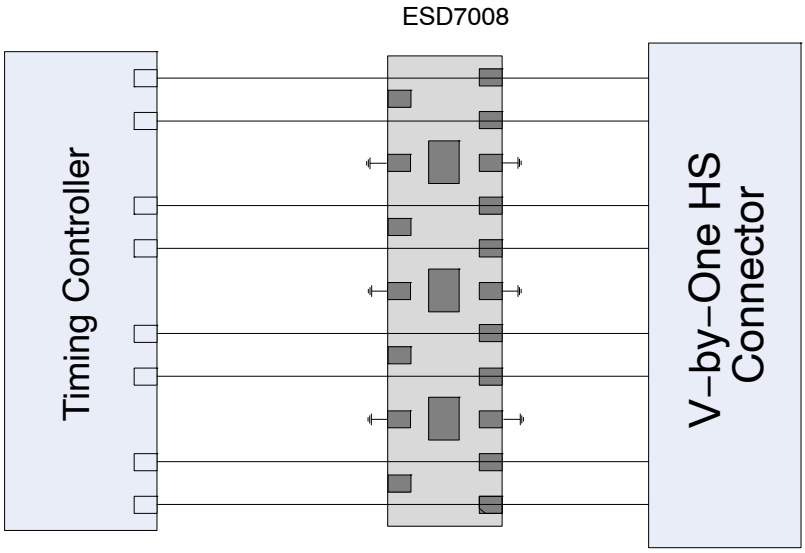


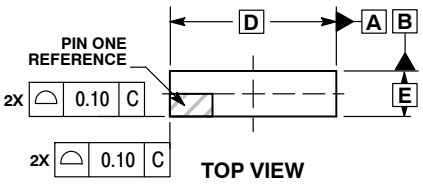
Figure 19. V−by−One HS Layout Diagram (for LCD Panel)

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

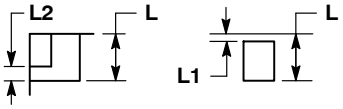
SCALE 2:1

UDFN18, 5.5x1.5, 0.5P
CASE 517BV
ISSUE A

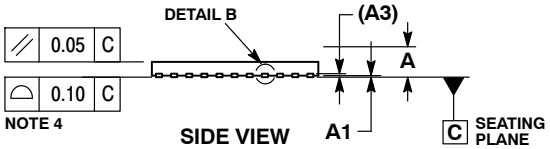
DATE 11 DEC 2012



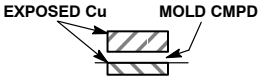
TOP VIEW



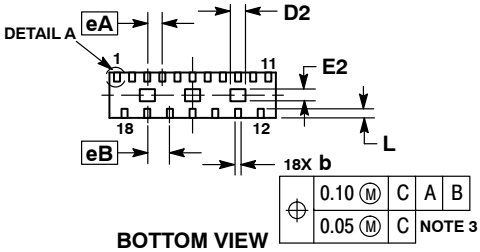
DETAIL A
OPTIONAL CONSTRUCTIONS



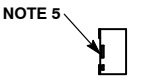
SIDE VIEW



DETAIL B
OPTIONAL CONSTRUCTION



BOTTOM VIEW

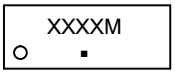


END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.10 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. EXPOSED ENDS OF TERMINALS ARE ELECTRICALLY ACTIVE.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	5.50 BSC	
D2	0.45	0.55
E	1.50 BSC	
E2	0.35	0.45
eA	0.50 BSC	
eB	0.75 BSC	
L	0.20	0.40
L1	0.00	0.05
L2	0.10 REF	

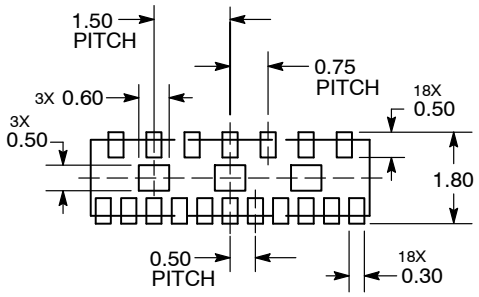
GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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