74AVC4T774-Q100

4-bit dual supply translating transceiver; 3-state

Rev. 1 — 11 May 2022 Product data sheet

1. General description

The 74AVC4T774-Q100 is a 4-bit, dual supply transceiver that enables bidirectional level translation. It features eight 1-bit input-output ports (An and Bn), four direction control inputs (DIR1, DIR2, DIR3 and DIR4), an output enable input ($\overline{OE}$) and dual supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). Both $V_{CC(A)}$ and $V_{CC(B)}$ can be supplied at any voltage between 0.8 V and 3.6 V making the device suitable for translating between any of the low voltage nodes (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V). Pins An, $\overline{OE}$ and DIRn are referenced to $V_{CC(A)}$ and pins Bn are referenced to $V_{CC(B)}$. A HIGH on DIRn allows transmission from An to Bn and a LOW on DIRn allows transmission from Bn to An. The output enable input ($\overline{OE}$) can be used to disable the outputs so the buses are effectively isolated.

The device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either $V_{CC(A)}$ or $V_{CC(B)}$ are at GND level, both An and Bn are in the high-impedance OFF-state.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range:
  - $V_{CC(A)}$: 0.8 V to 3.6 V
  - $V_{CC(B)}$: 0.8 V to 3.6 V
- Complies with JEDEC standards:
  - JESD8-12 (0.8 V to 1.3 V)
  - JESD8-11 (0.9 V to 1.65 V)
  - JESD8-7 (1.2 V to 1.95 V)
  - JESD8-5 (1.8 V to 2.7 V)
  - JESD8-B (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114E Class 3B exceeds 8000 V
  - CDM JESD22-C101C exceeds 1500 V
- Maximum data rates:
  - 380 Mbit/s (≥ 1.8 V to 3.3 V translation)
  - 200 Mbit/s (≥ 1.1 V to 3.3 V translation)
  - 200 Mbit/s (≥ 1.1 V to 2.5 V translation)
  - 200 Mbit/s (≥ 1.1 V to 1.8 V translation)
  - 150 Mbit/s (≥ 1.1 V to 1.5 V translation)
  - 100 Mbit/s (≥ 1.1 V to 1.2 V translation)
- Suspend mode
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- I_{OFF} circuitry provides partial Power-down mode operation

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AVC4T774BQ-Q100	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74AVC4T774GU-Q100	-40 °C to +125 °C	XQFN16	plastic, extremely thin quad flat package; no leads; 16 terminals; body 1.80 × 2.60 × 0.50 mm	SOT1161-1

4. Marking

Table 2. Marking codes

Type number	Marking code
74AVC4T774BQ-Q100	C4T774
74AVC4T774GU-Q100	B77

5. Functional diagram

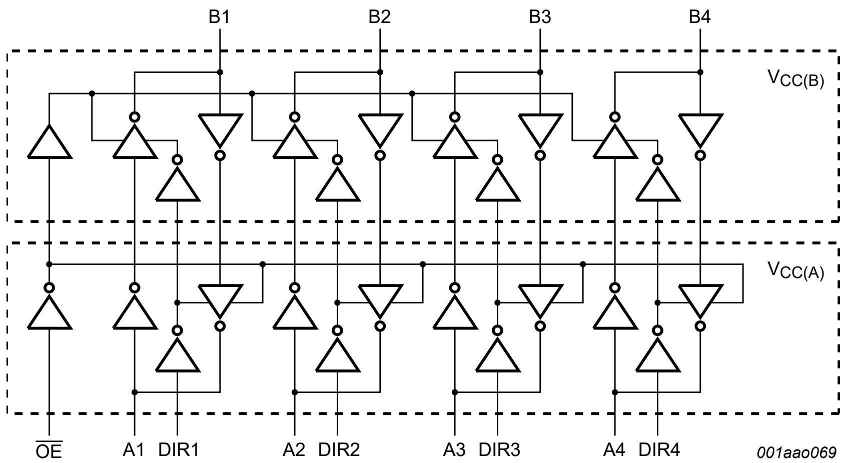


Fig. 1. Logic symbol

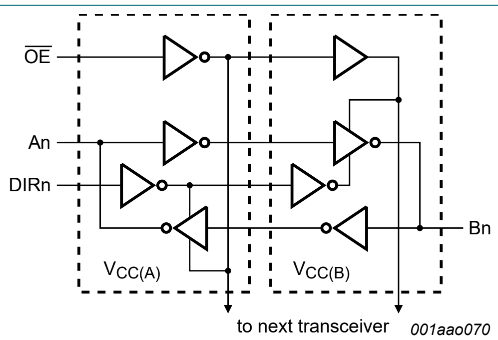
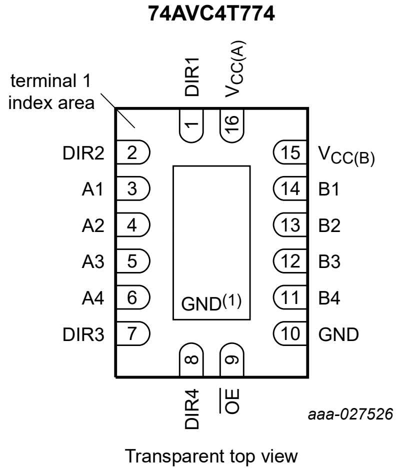


Fig. 2. Logic diagram (one 1-bit transceiver)

6. Pinning information

6.1. Pinning



(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

Fig. 3. Pin configuration SOT763-1 (DHVQFN16)

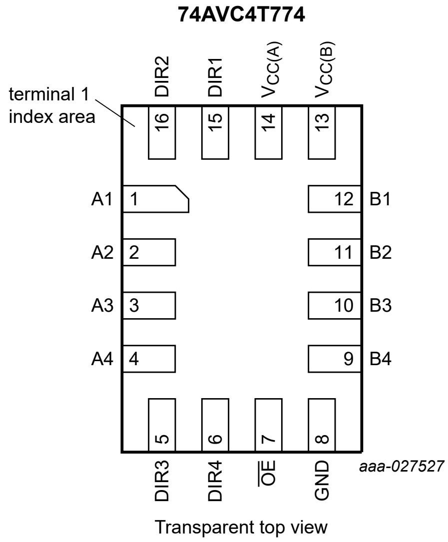


Fig. 4. Pin configuration SOT1161-1 (XQFN16)

6.2. Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT763-1	SOT1161-1	
$V_{CC(A)}$	16	14	supply voltage A (An, $\overline{OE}$ and DIRn inputs are referenced to $V_{CC(A)}$)
DIR1, DIR2, DIR3, DIR4	1, 2, 7, 8	15, 16, 5, 6	direction control input
A1, A2, A3, A4	3, 4, 5, 6	1, 2, 3, 4	data input or output
GND	10	8	ground (0 V)
B1, B2, B3, B4	14, 13, 12, 11	12, 11, 10, 9	data input or output
$\overline{OE}$	9	7	output enable input (active LOW)
$V_{CC(B)}$	15	13	supply voltage B (Bn pins are referenced to $V_{CC(B)}$)

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.
The An, DIRn and $\overline{OE}$ input circuit is referenced to $V_{CC(A)}$; The Bn input circuit is referenced to $V_{CC(B)}$.

Supply voltage	Input					Input/output	
$V_{CC(A)}$, $V_{CC(B)}$	$\overline{OE}$	DIR1	DIR2	DIR3	DIR4	An	Bn
0.8 V to 3.6 V	L	L	X	X	X	A1 = B1	input B1
0.8 V to 3.6 V	L	H	X	X	X	input A1	B1 = A1
0.8 V to 3.6 V	L	X	L	X	X	A2 = B2	input B2
0.8 V to 3.6 V	L	X	H	X	X	input A2	B2 = A2
0.8 V to 3.6 V	L	X	X	L	X	A3 = B3	input B3
0.8 V to 3.6 V	L	X	X	H	X	input A3	B3 = A3
0.8 V to 3.6 V	L	X	X	X	L	A4 = B4	input B4
0.8 V to 3.6 V	L	X	X	X	H	input A4	B4 = A4
0.8 V to 3.6 V	H	X	X	X	X	Z	Z
GND [1]	X	X	X	X	X	Z	Z

[1] If at least one of $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into suspend mode.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(A)}$	supply voltage A			-0.5	+4.6	V
$V_{CC(B)}$	supply voltage B			-0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V		-50	-	mA
V_I	input voltage		[1]	-0.5	+4.6	V
I_{OK}	output clamping current	$V_O < 0$ V		-50	-	mA
V_O	output voltage	Active mode	[1][2][3]	-0.5	V_{CCO} + 0.5	V
		Suspend or 3-state mode	[1]	-0.5	+4.6	V
I_O	output current	V_O = 0 V to V_{CCO}	[2]	-	±50	mA
I_{CC}	supply current	$I_{CC(A)}$ or $I_{CC(B)}$		-	100	mA
I_{GND}	ground current			-100	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C				
		SOT763-1 (DHVQFN16)	[4]	-	500	mW
		SOT1161-1 (XQFN16)		-	250	mW

[1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] V_{CCO} is the supply voltage associated with the output port.
[3] V_{CCO} + 0.5 V should not exceed 4.6 V.
[4] For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(A)}$	supply voltage A			0.8	3.6	V
$V_{CC(B)}$	supply voltage B			0.8	3.6	V
V_I	input voltage			0	3.6	V
V_O	output voltage	Active mode	[1]	0	V_{CCO}	V
		Suspend or 3-state mode		0	3.6	V
T_{amb}	ambient temperature			-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CCI} =0.8 V to 3.6 V	[2]	-	10	ns/V

[1] V_{CCO} is the supply voltage associated with the output port.
[2] V_{CCI} is the supply voltage associated with the input port.

10. Static characteristics

Table 7. Typical static characteristics at T_{amb} = 25 °C

V_{CCI} is the supply voltage associated with the data input port.
V_{CCO} is the supply voltage associated with the output port.
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = -1.5 mA; $V_{CC(A)} = V_{CC(B)}$ = 0.8 V		-	0.69	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 1.5 mA; $V_{CC(A)} = V_{CC(B)}$ = 0.8 V		-	0.07	-	V
I_I	input leakage current	DIRn, $\overline{OE}$ input; V_I = 0 V or 3.6 V; $V_{CC(A)} = V_{CC(B)}$ = 0.8 V to 3.6 V		-	±0.025	±0.25	μA
I_{OZ}	OFF-state output current	A or B port; V_O = 0 V or V_{CCO}; $V_{CC(A)} = V_{CC(B)}$ = 3.6 V	[1]	-	±0.5	±2.5	μA
		suspend mode A port; V_O = 0 V or V_{CCO}; $V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V	[1]	-	±0.5	±2.5	μA
		suspend mode B port; V_O = 0 V or V_{CCO}; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 3.6 V	[1]	-	±0.5	±2.5	μA
I_{OFF}	power-off leakage current	A port; V_I or V_O = 0 V to 3.6 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 0.8 V to 3.6 V		-	±0.1	±1	μA
		B port; V_I or V_O = 0 V to 3.6 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 0.8 V to 3.6 V		-	±0.1	±1	μA
C_I	input capacitance	DIRn, $\overline{OE}$ input; V_I = 0 V or 3.3 V; $V_{CC(A)} = V_{CC(B)}$ = 3.3 V		-	2.0	-	pF
$C_{I/O}$	input/output capacitance	A and B port; V_O = 3.3 V or 0 V; $V_{CC(A)} = V_{CC(B)}$ = 3.3 V		-	4.0	-	pF

[1] For I/O ports, the parameter I_{OZ} includes the input leakage current.

Table 8. Static characteristics

V_{CCI} is the supply voltage associated with the data input port.
V_{CCO} is the supply voltage associated with the output port.
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	data input					
		V_{CCI} = 0.8 V	$0.70V_{CCI}$	-	$0.70V_{CCI}$	-	V
		V_{CCI} = 1.1 V to 1.95 V	$0.65V_{CCI}$	-	$0.65V_{CCI}$	-	V
		V_{CCI} = 2.3 V to 2.7 V	1.6	-	1.6	-	V
		V_{CCI} = 3.0 V to 3.6 V	2	-	2	-	V
		DIRn, $\overline{OE}$ input					
		$V_{CC(A)}$ = 0.8 V	$0.70V_{CC(A)}$	-	$0.70V_{CC(A)}$	-	V
		$V_{CC(A)}$ = 1.1 V to 1.95 V	$0.65V_{CC(A)}$	-	$0.65V_{CC(A)}$	-	V
		$V_{CC(A)}$ = 2.3 V to 2.7 V	1.6	-	1.6	-	V
		$V_{CC(A)}$ = 3.0 V to 3.6 V	2	-	2	-	V
V_{IL}	LOW-level input voltage	data input					
		V_{CCI} = 0.8 V	-	$0.30V_{CCI}$	-	$0.30V_{CCI}$	V
		V_{CCI} = 1.1 V to 1.95 V	-	$0.35V_{CCI}$	-	$0.35V_{CCI}$	V
		V_{CCI} = 2.3 V to 2.7 V	-	0.7	-	0.7	V
		V_{CCI} = 3.0 V to 3.6 V	-	0.8	-	0.8	V
		DIRn, $\overline{OE}$ input					
		$V_{CC(A)}$ = 0.8 V	-	$0.30V_{CC(A)}$	-	$0.30V_{CC(A)}$	V
		$V_{CC(A)}$ = 1.1 V to 1.95 V	-	$0.35V_{CC(A)}$	-	$0.35V_{CC(A)}$	V
		$V_{CC(A)}$ = 2.3 V to 2.7 V	-	0.7	-	0.7	V
		$V_{CC(A)}$ = 3.0 V to 3.6 V	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = -100 μA; $V_{CC(A)} = V_{CC(B)}$ = 0.8 V to 3.6 V	V_{CCO} - 0.1	-	V_{CCO} - 0.1	-	V
		I_O = -3 mA; $V_{CC(A)} = V_{CC(B)}$ = 1.1 V	0.85	-	0.85	-	V
		I_O = -6 mA; $V_{CC(A)} = V_{CC(B)}$ = 1.4 V	1.05	-	1.05	-	V
		I_O = -8 mA; $V_{CC(A)} = V_{CC(B)}$ = 1.65 V	1.2	-	1.2	-	V
		I_O = -9 mA; $V_{CC(A)} = V_{CC(B)}$ = 2.3 V	1.75	-	1.75	-	V
		I_O = -12 mA; $V_{CC(A)} = V_{CC(B)}$ = 3.0 V	2.3	-	2.3	-	V

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 100 μA; $V_{CC(A)} = V_{CC(B)}$ = 0.8 V to 3.6 V	-	0.1	-	0.1	V
		I_O = 3 mA; $V_{CC(A)} = V_{CC(B)}$ = 1.1 V	-	0.25	-	0.25	V
		I_O = 6 mA; $V_{CC(A)} = V_{CC(B)}$ = 1.4 V	-	0.35	-	0.35	V
		I_O = 8 mA; $V_{CC(A)} = V_{CC(B)}$ = 1.65 V	-	0.45	-	0.45	V
		I_O = 9 mA; $V_{CC(A)} = V_{CC(B)}$ = 2.3 V	-	0.55	-	0.55	V
		I_O = 12 mA; $V_{CC(A)} = V_{CC(B)}$ = 3.0 V	-	0.7	-	0.7	V
I_I	input leakage current	DIRn, $\overline{OE}$ input; V_I = 0 V or 3.6 V; $V_{CC(A)} = V_{CC(B)}$ = 0.8 V to 3.6 V	-	±1	-	±5	μA
I_{OZ}	OFF-state output current	A or B port; V_O = 0 V or V_{CCO}; $V_{CC(A)} = V_{CC(B)}$ = 3.6 V [1]	-	±5	-	±30	μA
		suspend mode A port; V_O = 0 V or V_{CCO}; $V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V [1]	-	±5	-	±30	μA
		suspend mode B port; V_O = 0 V or V_{CCO}; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 3.6 V [1]	-	±5	-	±30	μA
I_{OFF}	power-off leakage current	A port; V_I or V_O = 0 V to 3.6 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 0.8 V to 3.6 V	-	±5	-	±30	μA
		B port; V_I or V_O = 0 V to 3.6 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 0.8 V to 3.6 V	-	±5	-	±30	μA

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I_{CC}	supply current	A port; V_I = 0 V or V_{CCI}; I_O = 0 A					
		$V_{CC(A)}$ = 0.8 V to 3.6 V; $V_{CC(B)}$ = 0.8 V to 3.6 V	-	10	-	55	μA
		$V_{CC(A)}$ = 1.1 V to 3.6 V; $V_{CC(B)}$ = 1.1 V to 3.6 V	-	8	-	50	μA
		$V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V	-	8	-	50	μA
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 3.6 V	-2	-	-12	-	μA
		B port; V_I = 0 V or V_{CCI}; I_O = 0 A					
		$V_{CC(A)}$ = 0.8 V to 3.6 V; $V_{CC(B)}$ = 0.8 V to 3.6 V	-	10	-	55	μA
		$V_{CC(A)}$ = 1.1 V to 3.6 V; $V_{CC(B)}$ = 1.1 V to 3.6 V	-	8	-	50	μA
		$V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V	-2	-	-12	-	μA
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 3.6 V	-	8	-	50	μA
		A plus B port ($I_{CC(A)}$ + $I_{CC(B)}$); I_O = 0 A; V_I = 0 V or V_{CCI}; $V_{CC(A)}$ = 0.8 V to 3.6 V; $V_{CC(B)}$ = 0.8 V to 3.6 V	-	20	-	70	μA
		A plus B port ($I_{CC(A)}$ + $I_{CC(B)}$); I_O = 0 A; V_I = 0 V or V_{CCI}; $V_{CC(A)}$ = 1.1 V to 3.6 V; $V_{CC(B)}$ = 1.1 V to 3.6 V	-	16	-	65	μA
ΔI_{CC}	additional supply current	V_I = 3.0 V; $V_{CC(A)}$ = $V_{CC(B)}$ = 3.6 V	-	500	-	650	μA

[1] For I/O ports, the parameter I_{OZ} includes the input leakage current.

Table 9. Typical total supply current ($I_{CC(A)}$ + $I_{CC(B)}$)

$V_{CC(A)}$	$V_{CC(B)}$							Unit
	0 V	0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	0.1	0.1	0.1	0.1	0.1	0.1	μA
0.8 V	0.1	0.1	0.1	0.1	0.1	0.3	1.6	μA
1.2 V	0.1	0.1	0.1	0.1	0.1	0.1	0.8	μA
1.5 V	0.1	0.1	0.1	0.1	0.1	0.1	0.4	μA
1.8 V	0.1	0.1	0.1	0.1	0.1	0.1	0.2	μA
2.5 V	0.1	0.3	0.1	0.1	0.1	0.1	0.1	μA
3.3 V	0.1	1.6	0.8	0.4	0.2	0.1	0.1	μA

11. Dynamic characteristics

Table 10. Typical power dissipation capacitance at $V_{CC(A)}$ = $V_{CC(B)}$ and T_{amb} = 25 °C

Voltages are referenced to GND (ground = 0 V). [1] [2]

Symbol	Parameter	Conditions	$V_{CC(A)} = V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
C_{PD}	power dissipation capacitance	A port: (direction An to Bn); output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction An to Bn); output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction Bn to An); output enabled	9.5	9.7	9.8	9.9	10.7	11.9	pF
		A port: (direction Bn to An); output disabled	0.6	0.6	0.6	0.6	0.7	0.7	pF
		B port: (direction An to Bn); output enabled	9.5	9.7	9.8	9.9	10.7	11.9	pF
		B port: (direction An to Bn); output disabled	0.6	0.6	0.6	0.6	0.7	0.7	pF
		B port: (direction Bn to An); output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		B port: (direction Bn to An); output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] f_i = 10 MHz; V_I = GND to V_{CC}; $t_r = t_f$ = 1 ns; C_L = 0 pF; $R_L = \infty\ \Omega$.

Table 11. Typical dynamic characteristics at $V_{CC(A)}$ = 0.8 V and T_{amb} = 25 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7; for waveforms see Fig. 5 and Fig. 6. [1]

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			0.8 V	**1.2 V**	**1.5 V**	**1.8 V**	**2.5 V**	**3.3 V**	
t_{pd}	propagation delay	An to Bn	14.5	7.3	6.5	6.2	5.9	6.0	ns
		Bn to An	14.5	12.7	12.4	12.3	12.1	12.0	ns
t_{dis}	disable time	$\overline{OE}$ to An	14.3	14.3	14.3	14.3	14.3	14.3	ns
		$\overline{OE}$ to Bn	17.0	9.9	9.0	9.4	9.0	9.7	ns
t_{en}	enable time	$\overline{OE}$ to An	18.2	18.2	18.2	18.2	18.2	18.2	ns
		$\overline{OE}$ to Bn	19.2	10.7	9.8	9.6	9.7	10.2	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

Table 12. Typical dynamic characteristics at $V_{CC(B)}$ = 0.8 V and T_{amb} = 25 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7; for waveforms see Fig. 5 and Fig. 6. [1]

Symbol	Parameter	Conditions	$V_{CC(A)}$						Unit
			0.8 V	**1.2 V**	**1.5 V**	**1.8 V**	**2.5 V**	**3.3 V**	
t_{pd}	propagation delay	An to Bn	14.5	12.7	12.4	12.3	12.1	12.0	ns
		Bn to An	14.5	7.3	6.5	6.2	5.9	6.0	ns
t_{dis}	disable time	$\overline{OE}$ to An	14.3	5.5	4.1	4.0	3.0	3.5	ns
		$\overline{OE}$ to Bn	17.0	13.8	13.4	13.1	12.9	12.7	ns
t_{en}	enable time	$\overline{OE}$ to An	18.2	5.6	4.0	3.2	2.4	2.2	ns
		$\overline{OE}$ to Bn	19.2	14.6	14.1	13.9	13.7	13.6	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

Table 13. Dynamic characteristics for temperature range -40 °C to +85 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7; for waveforms see Fig. 5 and Fig. 6. [1]

Symbol	Parameter	Conditions	$V_{CC(B)}$										Unit
			1.2 V ±0.1 V		1.5 V ±0.1 V		1.8 V ±0.15 V		2.5 V ±0.2 V		3.3 V ±0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.1 V to 1.3 V													
t_{pd}	propagation delay	An to Bn	2.0	10.5	1.3	7.8	1.2	6.9	1.0	5.9	0.8	5.7	ns
		Bn to An	2.0	10.5	1.5	9.9	1.5	9.7	1.4	9.4	1.4	9.3	ns
t_{dis}	disable time	$\overline{OE}$ to An	2.0	10.0	2.0	10.0	2.0	10.0	2.0	10.0	2.0	10.0	ns
		$\overline{OE}$ to Bn	2.0	11.1	2.0	8.6	1.0	8.0	0.7	7.0	1.0	8.0	ns
t_{en}	enable time	$\overline{OE}$ to An	2.0	13.5	2.0	13.5	2.0	13.5	2.0	13.5	2.0	13.5	ns
		$\overline{OE}$ to Bn	2.0	15.0	2.0	11.0	2.0	9.4	1.0	7.8	1.0	7.4	ns
$V_{CC(A)}$ = 1.4 V to 1.6 V													
t_{pd}	propagation delay	An to Bn	1.5	9.9	1.0	7.1	1.0	6.0	0.5	4.8	0.5	4.3	ns
		Bn to An	1.3	7.8	1.0	7.1	0.9	6.9	0.8	6.6	0.6	6.5	ns
t_{dis}	disable time	$\overline{OE}$ to An	1.0	6.0	1.0	6.0	1.0	6.0	1.0	6.0	1.0	6.0	ns
		$\overline{OE}$ to Bn	2.0	10.2	1.5	7.5	0.9	7.2	0.4	6.2	0.4	6.1	ns
t_{en}	enable time	$\overline{OE}$ to An	1.0	7.5	1.0	7.5	1.0	7.5	1.0	7.5	1.0	7.5	ns
		$\overline{OE}$ to Bn	2.0	14.4	1.4	7.9	1.3	7.7	1.1	6.4	1.1	5.6	ns
$V_{CC(A)}$ = 1.65 V to 1.95 V													
t_{pd}	propagation delay	An to Bn	1.5	9.7	0.9	6.9	0.8	5.7	0.5	4.5	0.3	4.0	ns
		Bn to An	1.2	6.9	1.0	6.0	0.8	5.7	0.5	5.5	0.5	5.3	ns
t_{dis}	disable time	$\overline{OE}$ to An	0.5	5.7	0.5	5.7	0.5	5.7	0.5	5.7	0.5	5.7	ns
		$\overline{OE}$ to Bn	2.0	9.9	1.5	7.0	0.8	6.9	0.2	5.8	0.2	5.9	ns
t_{en}	enable time	$\overline{OE}$ to An	1.0	6.7	1.0	6.7	1.0	6.7	1.0	6.7	1.0	6.7	ns
		$\overline{OE}$ to Bn	1.5	13.9	1.2	7.2	1.2	6.9	0.8	5.4	0.6	5.0	ns
$V_{CC(A)}$ = 2.3 V to 2.7 V													
t_{pd}	propagation delay	An to Bn	1.4	9.4	0.8	6.6	0.5	5.5	0.4	4.2	0.2	3.7	ns
		Bn to An	1.0	5.9	0.5	4.8	0.5	4.5	0.4	4.2	0.3	3.9	ns
t_{dis}	disable time	$\overline{OE}$ to An	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	ns
		$\overline{OE}$ to Bn	2.0	9.3	1.5	6.7	0.7	6.3	0.2	5.0	0.2	5.7	ns
t_{en}	enable time	$\overline{OE}$ to An	0.6	4.5	0.6	4.5	0.6	4.5	0.6	4.5	0.6	4.5	ns
		$\overline{OE}$ to Bn	1.5	13.6	1.0	6.8	1.0	6.0	0.8	4.6	0.6	4.2	ns
$V_{CC(A)}$ = 3.0 V to 3.6 V													
t_{pd}	propagation delay	An to Bn	1.4	9.3	0.6	6.5	0.5	5.3	0.3	3.9	0.2	3.5	ns
		Bn to An	0.8	5.7	0.5	4.3	0.3	4.0	0.2	3.7	0.2	3.5	ns
t_{dis}	disable time	$\overline{OE}$ to An	0.2	4.5	0.2	4.5	0.2	4.5	0.2	4.5	0.2	4.5	ns
		$\overline{OE}$ to Bn	2.0	9.0	1.5	6.4	0.7	6.1	0.2	4.8	0.2	5.6	ns
t_{en}	enable time	$\overline{OE}$ to An	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	ns
		$\overline{OE}$ to Bn	1.5	13.4	1.0	6.7	1.0	5.9	0.7	4.4	0.5	4.0	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

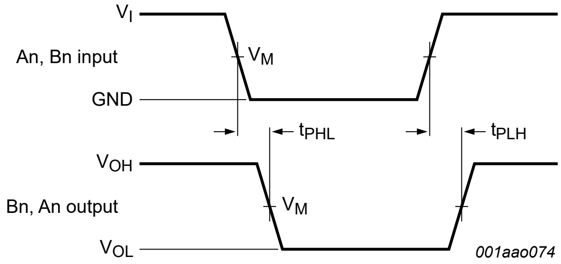
Table 14. Dynamic characteristics for temperature range -40 °C to +125 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7; for waveforms see Fig. 5 and Fig. 6. [1]

Symbol	Parameter	Conditions	$V_{CC(B)}$										Unit
			1.2 V ±0.1 V		1.5 V ±0.1 V		1.8 V ±0.15 V		2.5 V ±0.2 V		3.3 V ±0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.1 V to 1.3 V													
t_{pd}	propagation delay	An to Bn	2.0	12.1	1.3	9.0	1.2	8.0	1.0	6.8	0.8	6.6	ns
		Bn to An	2.0	12.1	1.5	11.4	1.5	11.2	1.4	10.9	1.4	10.7	ns
t_{dis}	disable time	$\overline{OE}$ to An	2.0	11.5	2.0	11.5	2.0	11.5	2.0	11.5	2.0	11.5	ns
		$\overline{OE}$ to Bn	2.0	12.8	2.0	9.9	1.0	9.2	0.7	8.1	1.0	9.2	ns
t_{en}	enable time	$\overline{OE}$ to An	2.0	15.6	2.0	15.6	2.0	15.6	2.0	15.6	2.0	15.6	ns
		$\overline{OE}$ to Bn	2.0	17.3	2.0	12.7	2.0	10.9	1.0	9.0	1.0	8.6	ns
$V_{CC(A)}$ = 1.4 V to 1.6 V													
t_{pd}	propagation delay	An to Bn	1.5	11.4	1.0	8.2	1.0	6.9	0.5	5.6	0.5	5.0	ns
		Bn to An	1.3	9.0	1.0	8.2	0.9	8.0	0.8	7.6	0.6	7.5	ns
t_{dis}	disable time	$\overline{OE}$ to An	1.0	6.9	1.0	6.9	1.0	6.9	1.0	6.9	1.0	6.9	ns
		$\overline{OE}$ to Bn	2.0	11.8	1.5	8.7	0.9	8.3	0.4	7.2	0.4	7.1	ns
t_{en}	enable time	$\overline{OE}$ to An	1.0	8.7	1.0	8.7	1.0	8.7	1.0	8.7	1.0	8.7	ns
		$\overline{OE}$ to Bn	2.0	16.6	1.4	9.1	1.3	8.9	1.1	7.4	1.1	6.5	ns
$V_{CC(A)}$ = 1.65 V to 1.95 V													
t_{pd}	propagation delay	An to Bn	1.5	11.2	0.9	8.0	0.8	6.6	0.5	5.2	0.3	4.6	ns
		Bn to An	1.2	8.0	1.0	6.9	0.8	6.6	0.5	6.4	0.5	6.1	ns
t_{dis}	disable time	$\overline{OE}$ to An	0.5	6.6	0.5	6.6	0.5	6.6	0.5	6.6	0.5	6.6	ns
		$\overline{OE}$ to Bn	2.0	11.4	1.5	8.1	0.8	8.0	0.2	6.7	0.2	6.8	ns
t_{en}	enable time	$\overline{OE}$ to An	1.0	7.8	1.0	7.8	1.0	7.8	1.0	7.8	1.0	7.8	ns
		$\overline{OE}$ to Bn	1.5	16.0	1.2	8.3	1.2	8.0	0.8	6.3	0.6	5.8	ns
$V_{CC(A)}$ = 2.3 V to 2.7 V													
t_{pd}	propagation delay	An to Bn	1.4	10.9	0.8	7.6	0.5	6.4	0.4	4.9	0.2	4.3	ns
		Bn to An	1.0	6.8	0.5	5.6	0.5	5.2	0.4	4.9	0.3	4.5	ns
t_{dis}	disable time	$\overline{OE}$ to An	0.2	4.6	0.2	4.6	0.2	4.6	0.2	4.6	0.2	4.6	ns
		$\overline{OE}$ to Bn	2.0	10.7	1.5	7.8	0.7	7.3	0.2	5.8	0.2	6.6	ns
t_{en}	enable time	$\overline{OE}$ to An	0.6	5.2	0.6	5.2	0.6	5.2	0.6	5.2	0.6	5.2	ns
		$\overline{OE}$ to Bn	1.5	15.7	1.0	7.9	1.0	6.9	0.8	5.3	0.6	4.9	ns
$V_{CC(A)}$ = 3.0 V to 3.6 V													
t_{pd}	propagation delay	An to Bn	1.4	10.7	0.6	7.5	0.5	6.1	0.3	4.5	0.2	4.1	ns
		Bn to An	0.8	6.6	0.5	5.0	0.3	4.6	0.2	4.3	0.2	4.1	ns
t_{dis}	disable time	$\overline{OE}$ to An	0.2	5.2	0.2	5.2	0.2	5.2	0.2	5.2	0.2	5.2	ns
		$\overline{OE}$ to Bn	2.0	10.4	1.5	7.4	0.7	7.1	0.2	5.6	0.2	6.5	ns
t_{en}	enable time	$\overline{OE}$ to An	0.5	4.6	0.5	4.6	0.5	4.6	0.5	4.6	0.5	4.6	ns
		$\overline{OE}$ to Bn	1.5	15.5	1.0	7.8	1.0	6.8	0.7	5.1	0.5	4.6	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

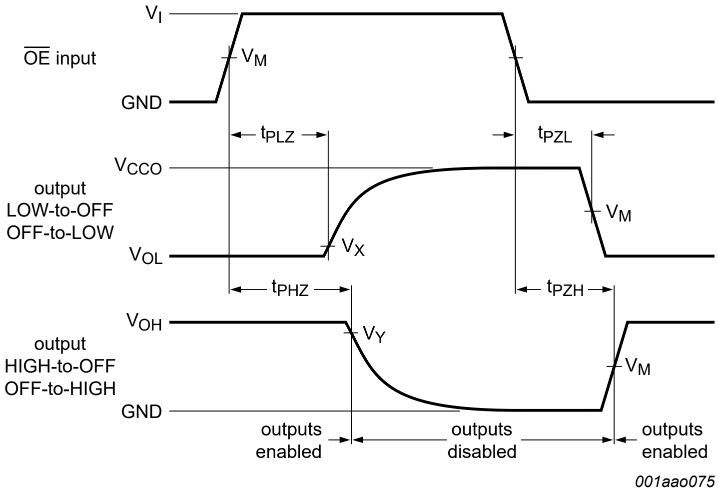
11.1. Waveforms and test circuit



Measurement points are given in Table 15.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. The data input (An, Bn) to output (Bn, An) propagation delay times



Measurement points are given in Table 15.

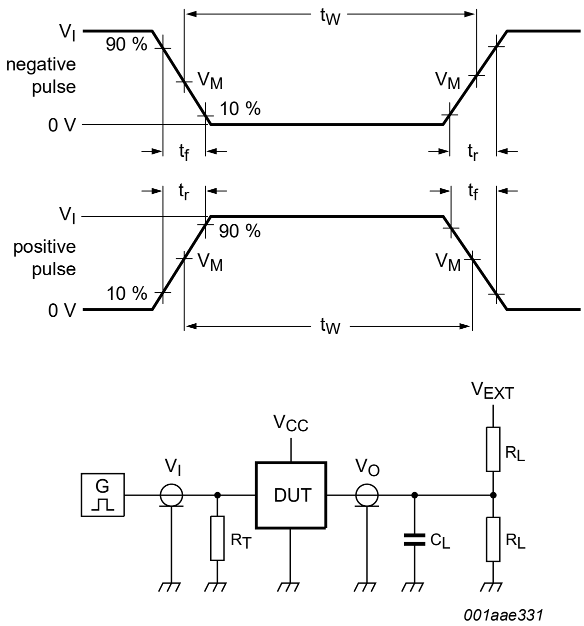
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 6. Enable and disable times

Table 15. Measurement points

Supply voltage	Input [1]	Output [2]		
$V_{CC(A)}$, $V_{CC(B)}$	V_M	V_M	V_X	V_Y
0.8 V to 1.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.1 V	V_{OH} - 0.1 V
1.65 V to 2.7 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
3.0 V to 3.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.3 V	V_{OH} - 0.3 V

[1] V_{CCI} is the supply voltage associated with the data input port.
[2] V_{CCO} is the supply voltage associated with the output port.



Test data is given in Table 16.

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator;

V_{EXT} = External voltage for measuring switching times;

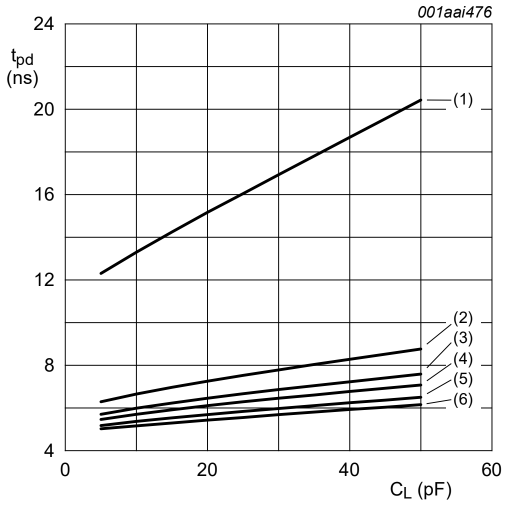
Fig. 7. Test circuit for measuring switching times

Table 16. Test data

Supply voltage	Input		Load		V_{EXT}		
$V_{CC(A)}$, $V_{CC(B)}$	V_I [1]	Δt/ΔV [2]	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ} [3]
0.8 V to 1.6 V	V_{CCI}	≤ 1.0 ns/V	15 pF	2 kΩ	open	GND	$2V_{CCO}$
1.65 V to 2.7 V	V_{CCI}	≤ 1.0 ns/V	15 pF	2 kΩ	open	GND	$2V_{CCO}$
3.0 V to 3.6 V	V_{CCI}	≤ 1.0 ns/V	15 pF	2 kΩ	open	GND	$2V_{CCO}$

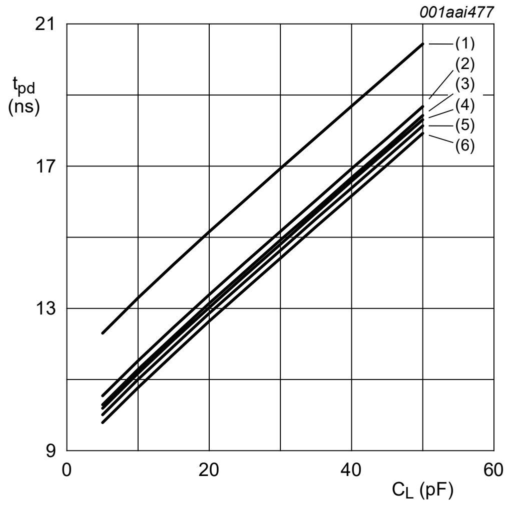
[1] V_{CCI} is the supply voltage associated with the data input port.
[2] dV/dt ≥ 1.0 V/ns.
[3] V_{CCO} is the supply voltage associated with the output port.

11.2. Typical propagation delay characteristics



a. Propagation delay (A to B); $V_{CC(A)}$ = 0.8 V

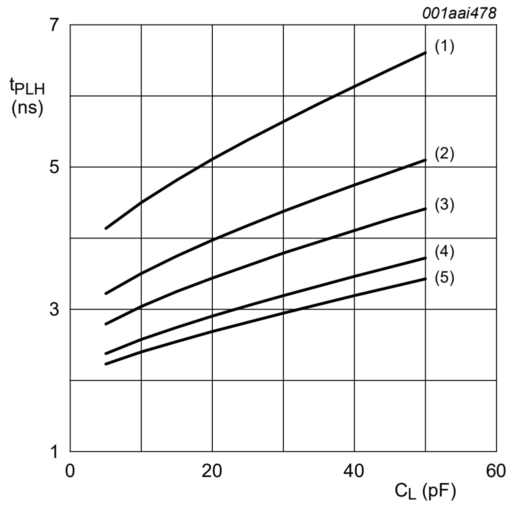
(1) $V_{CC(B)}$ = 0.8 V
(2) $V_{CC(B)}$ = 1.2 V
(3) $V_{CC(B)}$ = 1.5 V
(4) $V_{CC(B)}$ = 1.8 V
(5) $V_{CC(B)}$ = 2.5 V
(6) $V_{CC(B)}$ = 3.3 V



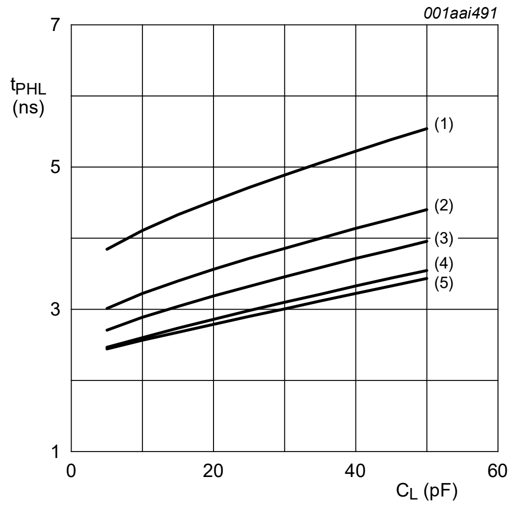
b. Propagation delay (A to B); $V_{CC(B)}$ = 0.8 V

(1) $V_{CC(A)}$ = 0.8 V
(2) $V_{CC(A)}$ = 1.2 V
(3) $V_{CC(A)}$ = 1.5 V
(4) $V_{CC(A)}$ = 1.8 V
(5) $V_{CC(A)}$ = 2.5 V
(6) $V_{CC(A)}$ = 3.3 V

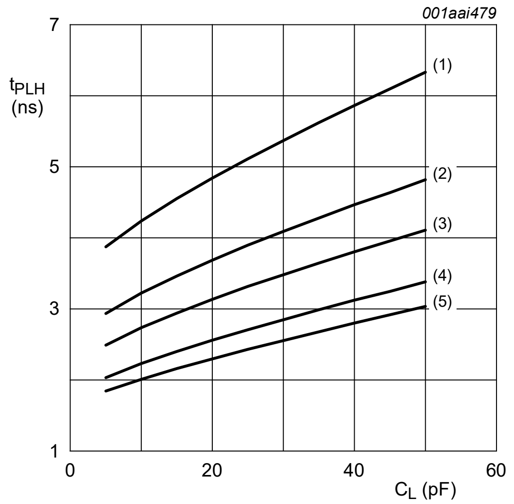
Fig. 8. Typical propagation delay versus load capacitance; T_{amb} = 25 °C



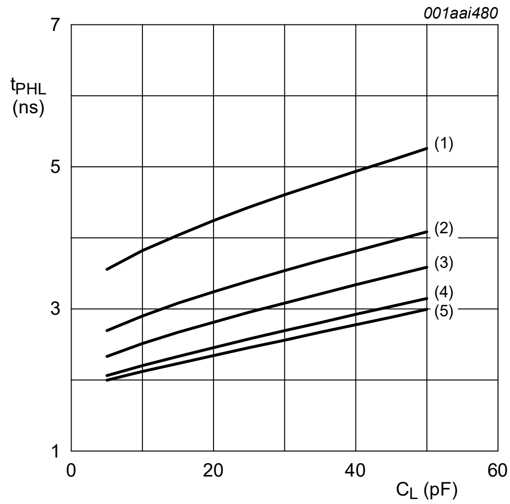
a. LOW to HIGH propagation delay (A to B); $V_{CC(A)}$ = 1.2 V



b. HIGH to LOW propagation delay (A to B); $V_{CC(A)}$ = 1.2 V



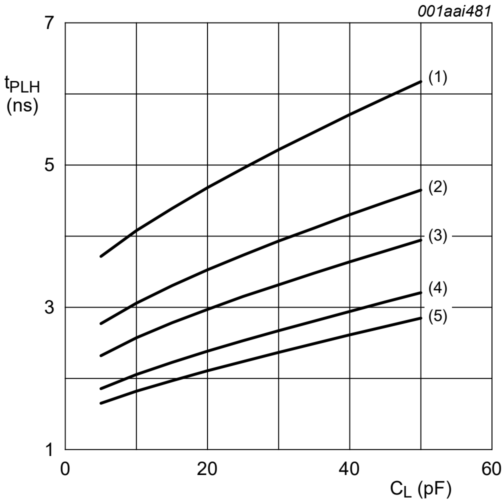
c. LOW to HIGH propagation delay (A to B); $V_{CC(A)}$ = 1.5 V



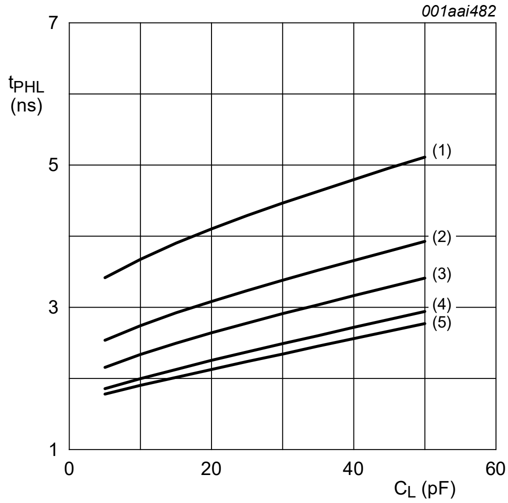
d. HIGH to LOW propagation delay (A to B); $V_{CC(A)}$ = 1.5 V

(1) $V_{CC(B)}$ = 1.2 V
(2) $V_{CC(B)}$ = 1.5 V
(3) $V_{CC(B)}$ = 1.8 V
(4) $V_{CC(B)}$ = 2.5 V
(5) $V_{CC(B)}$ = 3.3 V

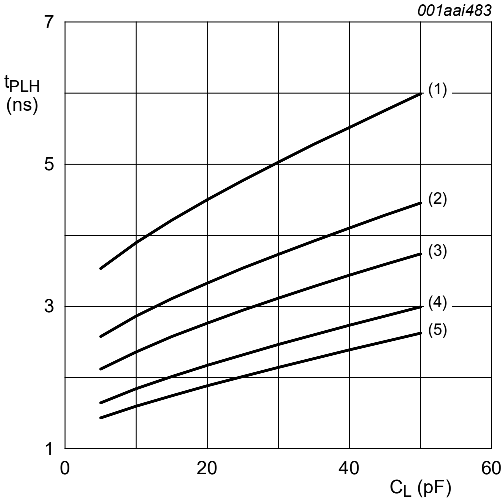
Fig. 9. Typical propagation delay versus load capacitance; T_{amb} = 25 °C



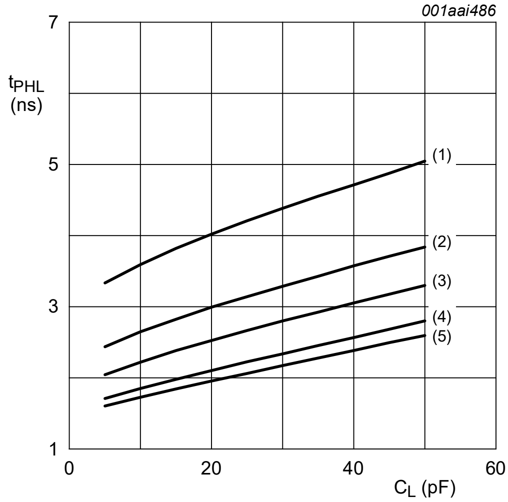
a. LOW to HIGH propagation delay (A to B); $V_{CC(A)}$ = 1.8 V



b. HIGH to LOW propagation delay (A to B); $V_{CC(A)}$ = 1.8 V



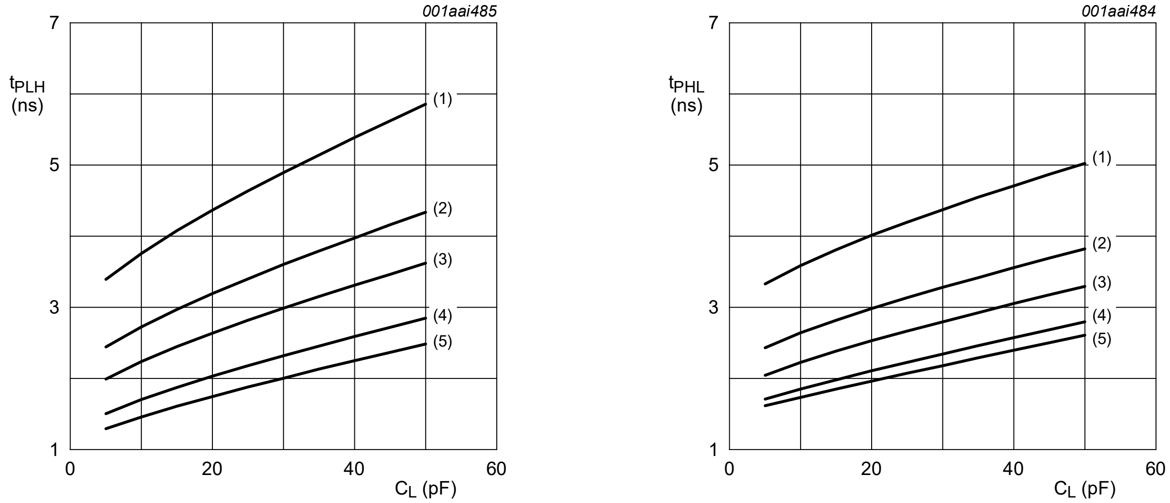
c. LOW to HIGH propagation delay (A to B); $V_{CC(A)}$ = 2.5 V



d. HIGH to LOW propagation delay (A to B); $V_{CC(A)}$ = 2.5 V

(1) $V_{CC(B)}$ = 1.2 V
(2) $V_{CC(B)}$ = 1.5 V
(3) $V_{CC(B)}$ = 1.8 V
(4) $V_{CC(B)}$ = 2.5 V
(5) $V_{CC(B)}$ = 3.3 V

Fig. 10. Typical propagation delay versus load capacitance; T_{amb} = 25 °C



a. LOW to HIGH propagation delay (A to B); $V_{CC(A)}$ = 3.3 V

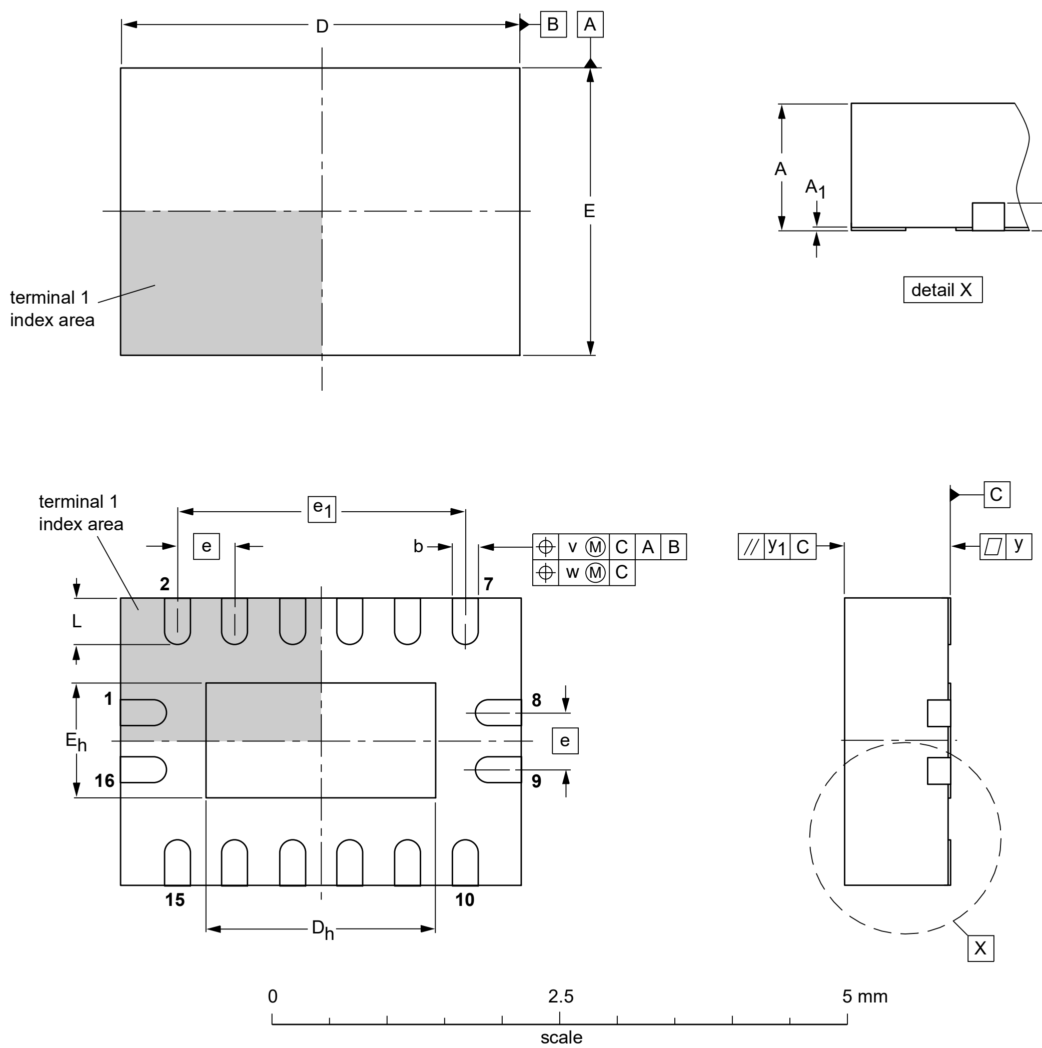
b. HIGH to LOW propagation delay (A to B); $V_{CC(A)}$ = 3.3 V

(1) $V_{CC(B)}$ = 1.2 V
(2) $V_{CC(B)}$ = 1.5 V
(3) $V_{CC(B)}$ = 1.8 V
(4) $V_{CC(B)}$ = 2.5 V
(5) $V_{CC(B)}$ = 3.3 V

Fig. 11. Typical propagation delay versus load capacitance; T_{amb} = 25 °C

12. Package outline

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

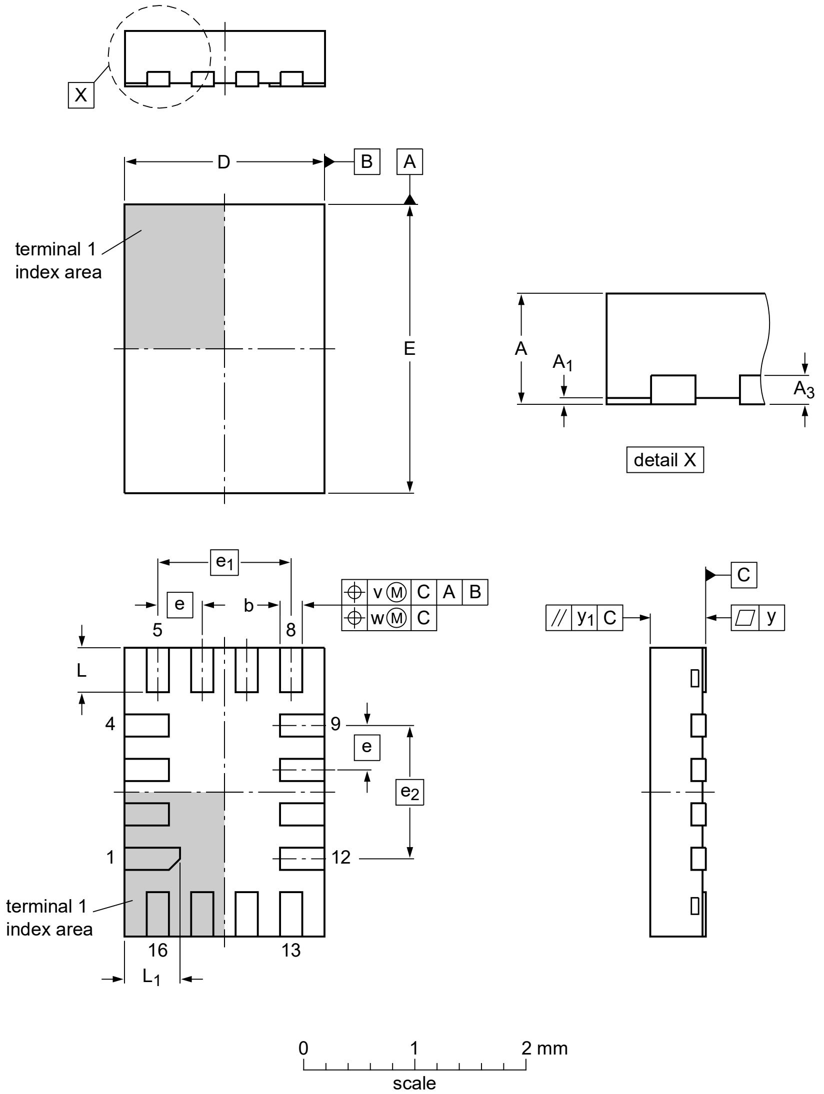
Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig. 12. Package outline SOT763-1 (DHVQFN16)

XQFN16: plastic, extremely thin quad flat package; no leads; 16 terminals; body 1.80 x 2.60 x 0.50 mm **SOT1161-1**



Dimensions

Unit(1)		A	A_1	A_3	b	D	E	e	e_1	e_2	L	L_1	v	w	y	y_1
mm	max	0.5	0.05		0.25	1.9	2.7				0.45	0.55				
	nom			0.127	0.20	1.8	2.6	0.4	1.2	1.2	0.40	0.50	0.1	0.05	0.05	0.05
	min		0.00		0.15	1.7	2.5				0.35	0.45				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1161-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1161-1	- - -	- - -	- - -			~~09-12-28~~ 09-12-29

Fig. 13. Package outline SOT1161-1 (XQFN16)

13. Abbreviations

Table 17. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

14. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AVC4T774_Q100 v.1	20220511	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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