36V/3.5A, Low IQ, Synchronous Step-Down Converter

Features

- AEC-Q100 certification in progress-Temperature grade1: -40°C to+125°C, T_A
- 2μA Low Shutdown Supply Current
- 14μA No-Load Quiescent Current
- Internal 125mΩ High-Side and 55mΩ Low-Side MOSFET
- External Soft Start (SS)
- 350kHz to 2.5MHz Programmable Switching Frequency
- Selectable External Clock Signal to Synchronize the Internal Oscillator Frequency
- 80ns Minimum on Time
- Selectable Forced PWM and PFM
- Power Good (PG) Output
- Hiccup Over-Current Protection (OCP)
- Available in a QFN-16 (3mmx4mm) Package

Application

- Factory and Building Automation Systems
- Infotainment and Cluster: Head unit, eCall
- Body Electronics and Lighting

Description

The TMI34030-Q1 regulator is an easy-to-use, synchronous, step-down DC/DC converter that delivers best-in-class efficiency for Automotive applications. The TMI34030-Q1 drives up to 3.5A of load current from an input of up to 36 V.

The TMI34030-Q1 provides high light load efficiency and output accuracy in a very small solution size. The synchronous operation and ultralow 14μA sleep mode quiescent current provide high efficiency over the output current load range, allowing the TMI34030-Q1 to be used in a variety of step-down applications in automotive input environments and battery-powered applications.

Peak-current-mode operation provides fast transient response and eases loop stabilization. Protection features include thermal shutdown, input under voltage lockout, and hiccup short-circuit protection. An open-drain power good (PG) signal indicates when the output is within 10% of its nominal voltage.

The TMI34030-Q1 requires a minimal number of readily available, standard, external components and is available in a compact QFN-16 (3mmx4mm) package.

Typical Application

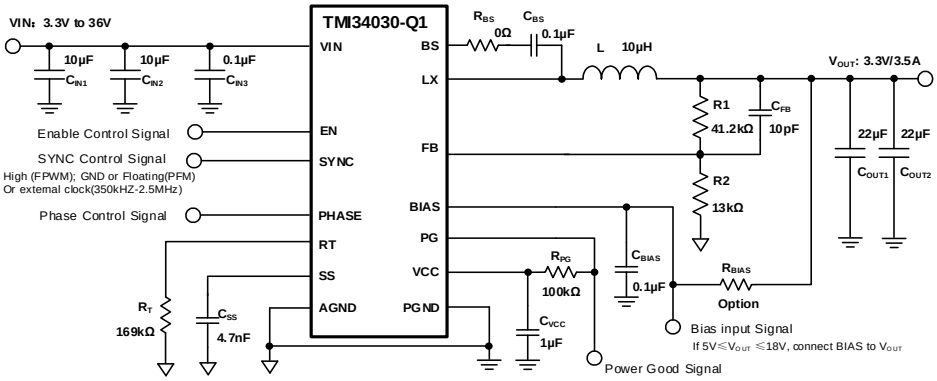
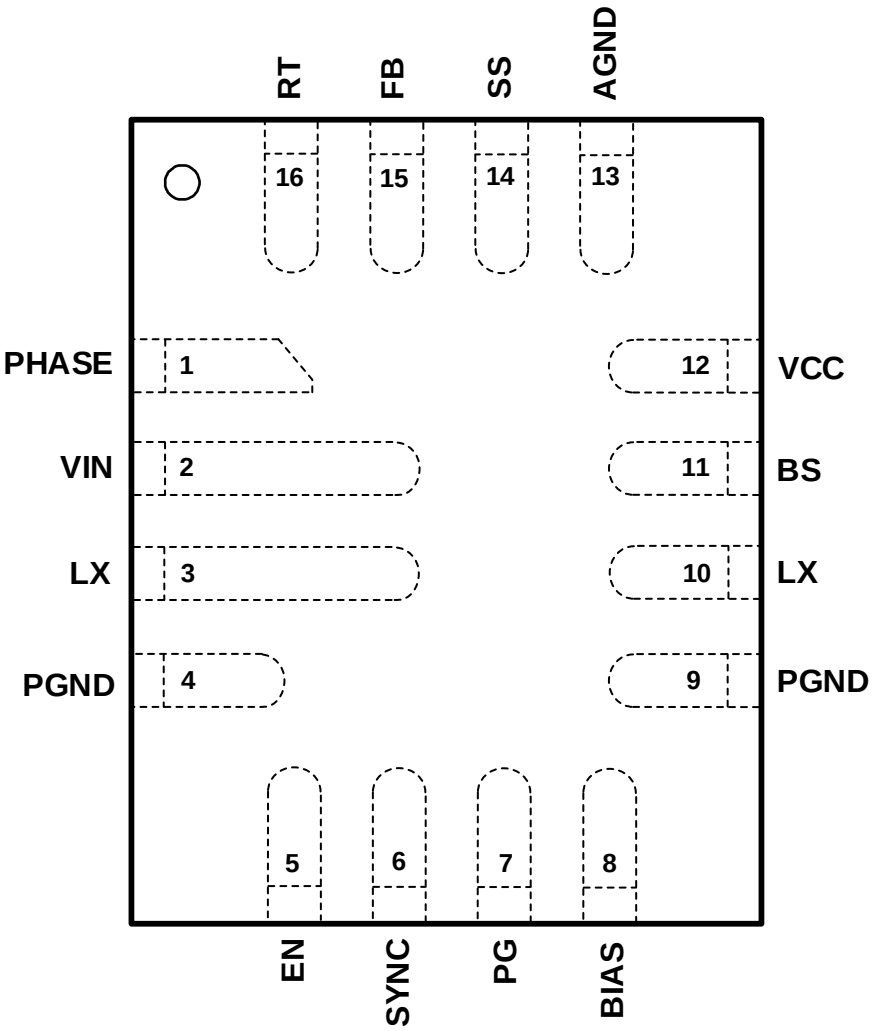


Figure 1. TMI34030-Q1 Typical Application Circuit

Package



QFN3×4-16

Top Marking: T34030-Q1/XXXXX (T34030-Q1: Device Code, XXXXX: Inside Code)

Order Information

Part Number	Package	Top Marking
TMI34030-Q1	QFN3×4-16	T34030 -Q1 XXXXX

TMI34030-Q1 devices are Pb-free and RoHS compliant.

Pin Functions

Pin	Name	Function
1	PHASE	Selectable in-phase or 180° out-of-phase of SYNC input. Pull PHASE high to be in-phase. Pull PHASE low to be 180° out-of-phase. Recommend to connect this pin to GND if not used.
2	VIN	Input power supply pin. The decoupling ceramic capacitors should be placed as close as possible from this pin to GND for better noise rejection.
3,10	LX	Switching pins. Connect to the power inductor.
4,9	PGND	Power ground pin. PGND is the reference ground of the power device and requires careful consideration during PCB layout.
5	EN	Enable. Drive this pin to a logic-high to enable the IC. Drive to a logic-low to disable the IC and shutdown.
6	SYNC	Synchronize. Apply a 350kHz to 2.5MHz clock signal to SYNC to synchronize the internal oscillator frequency to the external clock. The external clock should be at least 250kHz larger than the R_T set frequency. SYNC can also be used to select forced Pulse width mode (FPWM) or Pulse frequency mode (PFM). Before the chip starts up, drive SYNC low or leave SYNC floating to choose PFM, and drive SYNC high to external power source or pull up SYNC to VCC directly to set the part forced PWM mode.
7	PG	Power good indicator output pin. The output of PG is an open drain. Float PG if not used.
8	BIAS	Bias input. Connect BIAS to an external power supply (5V ≤ VBIAS ≤ 18V) to reduce power dissipation and increase efficiency. If not in use, float BIAS or connect BIAS to ground.
11	BS	Bootstrap. A 0.1μF capacitor connected between LX and BS pins is required to form a floating supply across the high-side switch driver.
12	VCC	Bias supply. VCC supplies power to the internal control circuit and gate drivers. A decoupling capacitor (≥1μF) to ground is required close to VCC.
13	AGND	Analog ground pin. AGND is the reference ground of the logic circuit.
14	SS	Optional external soft-start time control pin. Connect a capacitor between SS pin and AGND to set soft-start time. The default internal soft-start time is 0.7ms with SS pin floating.
15	FB	Output Voltage feedback input. Connect FB to the center point of the external resistor divider. The feedback threshold voltage is 0.8V. Place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces. For fixed output version, connect FB pin to the output directly.
16	RT	Switching frequency program. Connect a resistor from RT to ground to set the switching frequency.

Absolute Maximum Ratings (Note 1)

Items	Min	Max	Unit
VIN, EN, PG	-0.3	40	V
LX	-0.3	VIN+0.3	V
LX Voltages (<10ns transient)	-5	42	V
BS		LX+6.5	V
BIAS	-0.3	20	V
All other pins	-0.3	6	V
Continuous power dissipation (T_A=+25°C) (NOTE2)		2.6	W
Junction Temperature		150	°C
Lead Temperature		260	°C
Storage Temperature	-65	150	°C

Recommended Operating Conditions

Items	Min	Max	Unit
VIN	3.3	36	V
Operating Junction Temp (T_J)	-40	125	°C

Thermal Resistance (Note 3)

Items	Description	Value	Unit
θ_{JA}	Junction-to-ambient thermal resistance	46.8	°C/W
θ_{JC}	Junction-to-case(top) thermal resistance	11	°C/W
ψ_{JC}	Junction-to-case(top) characterization parameter	0.8	°C/W

ESD Ratings (Note 4)

Items	Description	Value	Unit
$V_{(ESD-HBM)}$	Human Body Model for all pins	±2000	V
$V_{(ESD-CDM)}$	Charged Device Model for all pins	±500	V

Note 1: Exceeding these ratings may damage the device.

Note 2: The maximum allowable power dissipation is a function of the maximum junction temperature $T_{J(MAX)}$, the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_{D(MAX)}= (T_{J(MAX)}-T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

Note 3: Measured on JESD51-7, 4-layer PCB. T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula: $T_J = T_A + P_D \times \theta_{JA}$.

Note 4: Devices are ESD sensitive. Handling precaution is recommended.

Electrical Characteristics

VIN = 12V, V_{EN} = 2V, T_J = -40°C to +125°C T_A=25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VIN						
VIN quiescent current	I_Q	V_{FB} = 0.85V, no load, no switching, T_J=+25°C		14	21	μA
		V_{FB} = 0.85V, no load, no switching			29	
VIN shutdown current	I_{SHDN}	V_{EN} = 0V		2	6	μA
VIN under-voltage lockout threshold rising	$INUV_{RISING}$		2.4	2.8	3.2	V
VIN under-voltage lockout threshold hysteresis	$INUV_{HYS}$			150		mV
Enable						
EN rising threshold	V_{EN_RISING}		0.9	1.05	1.2	V
EN threshold hysteresis	V_{EN_HYS}			120		mV
FB						
Feedback reference voltage	V_{REF}		784	800	816	mV
		T_J = +25°C	792	800	808	mV
$R_{DS(ON)}$						
HS switch on resistance	R_{ON_HS}	$V_{BS} - V_{LX}$ = 5V		125	165	mΩ
LS switch on resistance	R_{ON_LS}			55	85	mΩ
Switching Frequency and Ton						
Switching frequency	F_{SW}	R_T = 180kΩ or from sync clock	400	475	550	kHz
		R_T = 82kΩ or from sync clock	850	1000	1150	kHz
		R_T = 27kΩ or from sync clock	2250	2500	2750	kHz
Minimum on time (NOTE6)	T_{ON_MIN}			80		ns
SYNC						
SYNC input low voltage	V_{SYNC_LOW}				0.4	V
SYNC input high voltage	V_{SYNC_HIGH}		1.8			V
Current Limit						
Current limit	I_{LIMIT_HS}	Duty cycle = 40%	4.6	5.6	7.4	A
Low-side valley current limit	I_{LIMIT_LS}	V_{OUT} = 3.3V, L = 4.7μH	3.1	4.4	5.7	A
ZCD current	I_{ZCD}			0.1		A
Reverse current limit	$I_{LIMIT\_REVERSE}$			3		A
Switch leakage current	I_{SW_LKG}			0.01	1	μA
SS						
Soft-start current	I_{SS}	V_{SS} = 0.8V	5	10	15	μA

Electrical Characteristics

VIN = 12V, V_{EN} = 2V, T_J = -40°C to +125°C T_A=25°C,unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VCC						
VCC regulator	V_{CC}			5		V
VCC load regulation		I_{CC} = 5mA			3.5	%
PG						
PG rising threshold (V_{FB}/V_{REF})	PG_{RISING}	V_{FB} rising	85	90	95	%
		V_{FB} falling	105	110	115	%
PG falling threshold (V_{FB}/V_{REF})	$PG_{FALLING}$	V_{FB} falling	79	84	89	%
		V_{FB} rising	113.5	118.5	123.5	%
PG deglitch timer	$T_{PG\_DEGLITCH}$	PG from low to high		30		μs
		PG from high to low		50		μs
PG output voltage low	V_{PG_LOW}	I_{SINK} = 2mA		0.2	0.4	V
Thermal Shutdown						
Thermal Shut down (Note 6)	T_{SD}			170		ºC
Thermal Shut down Hysteresis (Note 6)	T_{HYS}			20		ºC

Note 6: Guaranteed by design.

Block Diagram

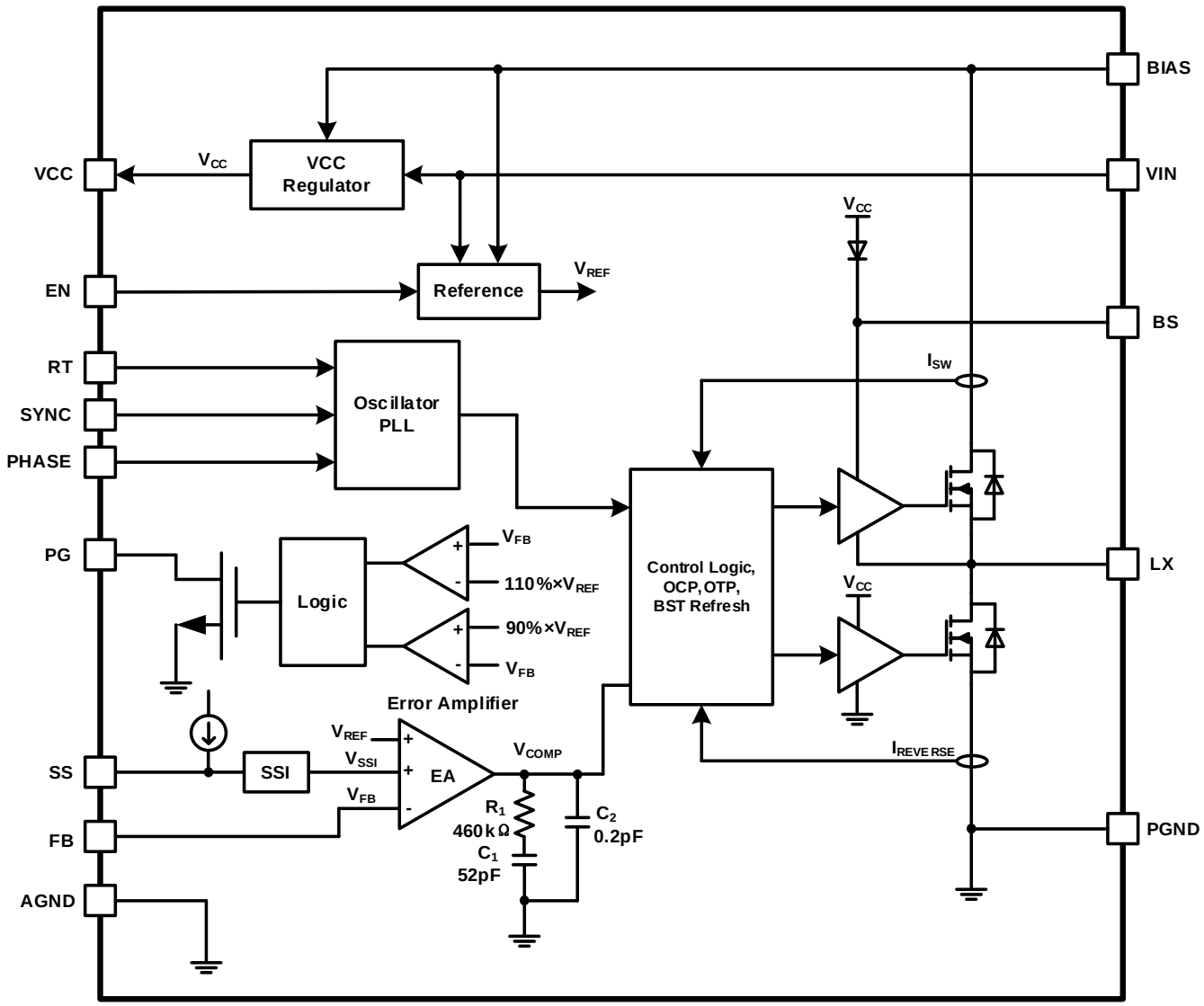


Figure 2 TMI34030-Q1 Block Diagram of Output Adjustable Version

Operation Description

Overview

The TMI34030-Q1 is a synchronous, step-down, switching regulator with integrated, internal, high-side and low-side power MOSFETs. The TMI34030-Q1 provides 3.5A of highly efficient output current with current mode control.

The TMI34030-Q1 features a wide input voltage range, switching frequency programmable from 350kHz to 2.5MHz, external soft start, and precision current limit. Its very low operational quiescent current makes it suitable for battery powered applications.

Pulse-Width Modulation (PWM) Control

At moderate-to-high output currents, the TMI34030-Q1 operates in a fixed-frequency, peak current-control mode to regulate the output voltage. A pulse-width modulation (PWM) cycle is initiated by the internal clock. At the rising edge of the clock, the high-side power MOSFET (HS-FET) is turned on and remains on until its current reaches the value set by the COMP voltage (VCOMP). If the current in the HSFET does not reach V_{COMP} in one PWM period, the HS-FET remains on, saving a turn-off operation.
When the high-side power switch is off, the low side MOSFET (LS-FET) is turned on immediately and remains on until the next cycle begins.
For each turn-on and -off in a switching cycle, the HS-FET turns on and off with a minimum on and off time limit.

Enable (EN) Control

EN is a digital control pin that turns the regulator on and off. When EN is pulled below its threshold voltage, the chip is put into the lowest shutdown current mode. Pulling EN above its threshold voltage turns on the part. Do not float EN.

Internal Regulator

Most of the internal circuitry is powered on by the 5V internal regulator. This regulator takes the VIN input and operates in the full VIN range. When VIN is greater than 5V, the output of the regulator is in full regulation. When VIN is lower than 5V, the output degrades.
For better thermal performance, connect BIAS to an external 5V source. VCC and the internal circuit are powered by BIAS. Since there is an internal diode between BIAS and the internal circuit, float BIAS or connect BIAS to GND if it is not being used.

Programmable Frequency (RT)

The TMI34030-Q1 oscillating frequency is programmed either by an external resistor (R_T) from RT to ground or by a logic level SYNC signal. The value of R_T can be calculated with Equation (1):

$$R_T(k\Omega) = \frac{170000}{f_s^{1.11}(kHz)} \quad (1)$$

The chip can be synchronized to an external clock ranging from 350kHz up to 2.5MHz through RT/SYNC.

Force Pulse width mode (FPWM) and Pulse frequency mode (PFM)

The TMI34030-Q1 employs Pulse frequency mode (PFM) functionality to optimize efficiency during light-load or no-load conditions. PFM can be enabled by connecting SYNC to a low level (<0.4V) before start-up; FPWM can be able when connecting SYNC to a high level (>1.8V) before start-up. SYNC can be used to synchronize switching again after startup.
If Force Pulse width mode (FPWM) is enabled, the device is forced to work with a fixed frequency regardless of the output load current. The advantage of FPWM is the controllable frequency and smaller output ripple, but it also has low efficiency at light load (see Figure 3).
If PFM is enabled, the TMI34030-Q1 first enters non-synchronous operation for as long as the inductor current is approaching zero at light load. If the load is further decreased or is at no load, VCOMP drops

below the PFM voltage (V_{PFM}), making the TMI34030-Q1 enter power-save mode (PSM). This puts the chip into sleep mode, which consumes very low quiescent current to further improve light-load efficiency. In PSM, the internal clock is reset whenever V_{COMP} crosses over V_{PFM}, and the crossover time is taken as the benchmark of the next clock. When the load increases, and the DC value of VCOMP is higher than V_{PFM}, the operation mode is discontinuous conduction mode (DCM) or CCM, which have a constant switching frequency.

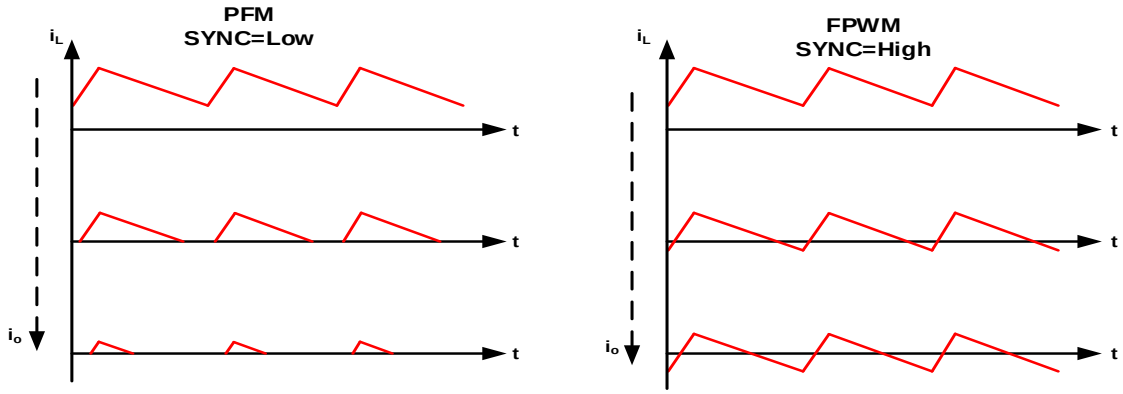


Figure 3 PFM and Forced PWM

Soft Start (SS)

Soft start (SS) is implemented to prevent the converter output voltage from overshooting during start-up. When the chip starts up, an internal current source begins charging the external soft-start capacitor. The internal SS voltage (V_{SSI}) rises with the soft-start voltage (V_{SS}), but V_{SSI} is a little different with V_{SS} due to a 0.5V offset and some delay. When V_{SS} is lower than 0.5V, V_{SSI} is 0V. VSSI rises from 0V to 0.8V during the period of V_{SS} rising from 0.5V to 1.6V. At this time, the error amplifier uses V_{SSI} as the reference, so the output voltage ramps up from 0V to the regulated value following V_{SSI} rising. When V_{SS} reaches 1.6V, V_{SSI} is 0.8V and overrides the internal V_{REF}, so the error amplifier uses the internal V_{REF} as the reference. The soft-start time (t_{SS}) set by the external SS capacitor can be calculated with Equation (2):

$$t_{ss}(ms) = \frac{C_{ss}(nF) \times 1.1V}{I_{ss}(\mu A)} \quad (2)$$

Where C_{SS} is the external SS capacitor, and I_{SS} is the internal 10μA SS charge current.
There is also an internal fixed 700μs soft start. The final SS time is determined by the longer time between 700μs and the external SS setting time. SS can be used for tracking and sequencing.

Pre-Bias Start-Up

During start-up, if V_{FB} > V_{SSI} -150mV, then the output has a pre-bias voltage, and neither the HS-FET or LS-FET turn on until V_{SSI} -150mV is higher than FB.

Bootstrap Charging

The bootstrap capacitor (0.1μF to 1μF) is charged and regulated to about 5V by the dedicated internal bootstrap regulator. When the voltage between the BS and LX nodes is lower than its regulation, a PMOS pass transistor connected from VIN to BS is turned on. The charging current path is from VIN to BS to

LX. An external circuit should provide enough voltage headroom to facilitate charging. When the HS-FET is on, VIN is about equal to LX, so the bootstrap capacitor cannot be charged.

At a higher duty cycle operation condition, the time period available to the bootstrap charging is less, so the bootstrap capacitor may not be charged sufficiently. In case the external circuit does not have sufficient voltage or time to charge the bootstrap capacitor, extra external circuitry can be used to ensure that the bootstrap voltage is in the normal operation region.

Low Dropout Operation (BS Refresh)

To improve dropout, the TMI34030-Q1 is designed to operate at close to 100% duty cycle for as long as the BS to LX voltage is greater than 2.5V. When the voltage from BS to LX drops below 2.5V, the HS-FET is turned off using an under-voltage lockout (UVLO) circuit, which allows the LS-FET to conduct and refresh the charge on the BS capacitor. In DCM or PSM, the LS-FET is forced on to refresh the BS voltage. Since the supply current sourced from the BS capacitor is low, the HS-FET can remain on for more switching cycles than are required to refresh the capacitor, making the effective duty cycle of the switching regulator high.

The effective duty cycle during the dropout of the regulator is mainly influenced by the voltage drops across the power MOSFET, inductor resistance, low-side diode and printed circuit board resistance.

SYNC and PHASE

The internal oscillator frequency can be synchronized to an external clock ranging from 350kHz up to 2.5MHz through SYNC. The external clock should be at least 250kHz larger than the R_T set frequency. Ensure that the high amplitude of the SYNC clock is higher than 1.8V and the low amplitude is lower than 0.4V. There is no pulse width requirement, but there is always parasitic capacitance of the pad, so if the pulse width is too short, a clear rising and falling edge may not be seen due to the parasitic capacitance. A pulse longer than 100ns is recommended in application.

PHASE is used when two or more TMI34030-Q1 devices are in parallel with the same SYNC clock. Pulling PHASE high forces the TMI34030-Q1 to operate in-phase of the SYNC clock. Pulling PHASE low forces the device to be 180° out of phase of the SYNC clock. By setting different voltages for PHASE, two devices can operate 180° out-of-phase to reduce the total input current ripple, so a smaller input bypass capacitor can be used (see Figure 4). The PHASE rising threshold is about 2.5V with a 400mV hysteresis.

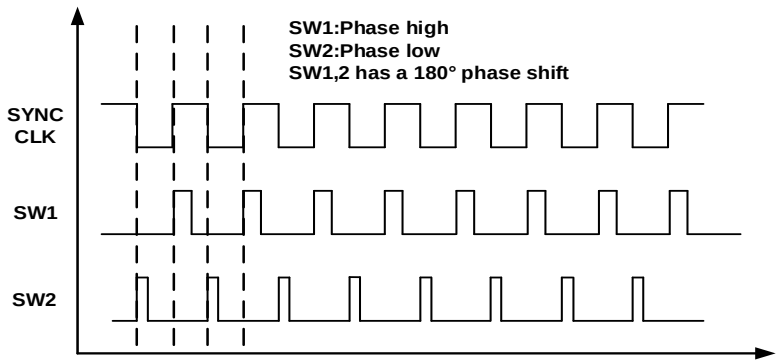


Figure 4 In-Phase and 180° Out-of-Phase

Start-Up and Shutdown

If both VIN and EN are higher than their appropriate thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the rest of the circuitries.

While the internal supply rail is up, an internal timer holds the power MOSFET off for about 50μs to blank any start-up glitches. When the soft-start block is enabled, the SS output is held low to ensure that the rest of the circuitries are ready before slowly ramping up.

Three events can shut down the chip: EN low, VIN low, and thermal shutdown. In the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

Hiccup Protection

When the output is shorted to ground, causing the output voltage to drop below 55% of its nominal output, the IC is shut down momentarily and begins discharging the soft start capacitor. The IC restarts with a full soft start when the soft-start capacitor is fully discharged. This hiccup process is repeated until the fault is removed.

Current Comparator and Current Limit

The power MOSFET current is accurately sensed via a current sense MOSFET. The current is then fed to the high-speed current comparator for current-mode control purposes. The current comparator takes this sensed current as one of its inputs. When the HS-FET is turned on, the comparator is first blanked until the end of the turn-on transition to avoid noise. Then the comparator compares the power switch current with V_{COMP}. When the sensed current is higher than V_{COMP}, the comparator outputs low to turn off the HS-FET. The maximum current of the internal power MOSFET is limited cycle-by-cycle internally.

Power Good Indicator (PG)

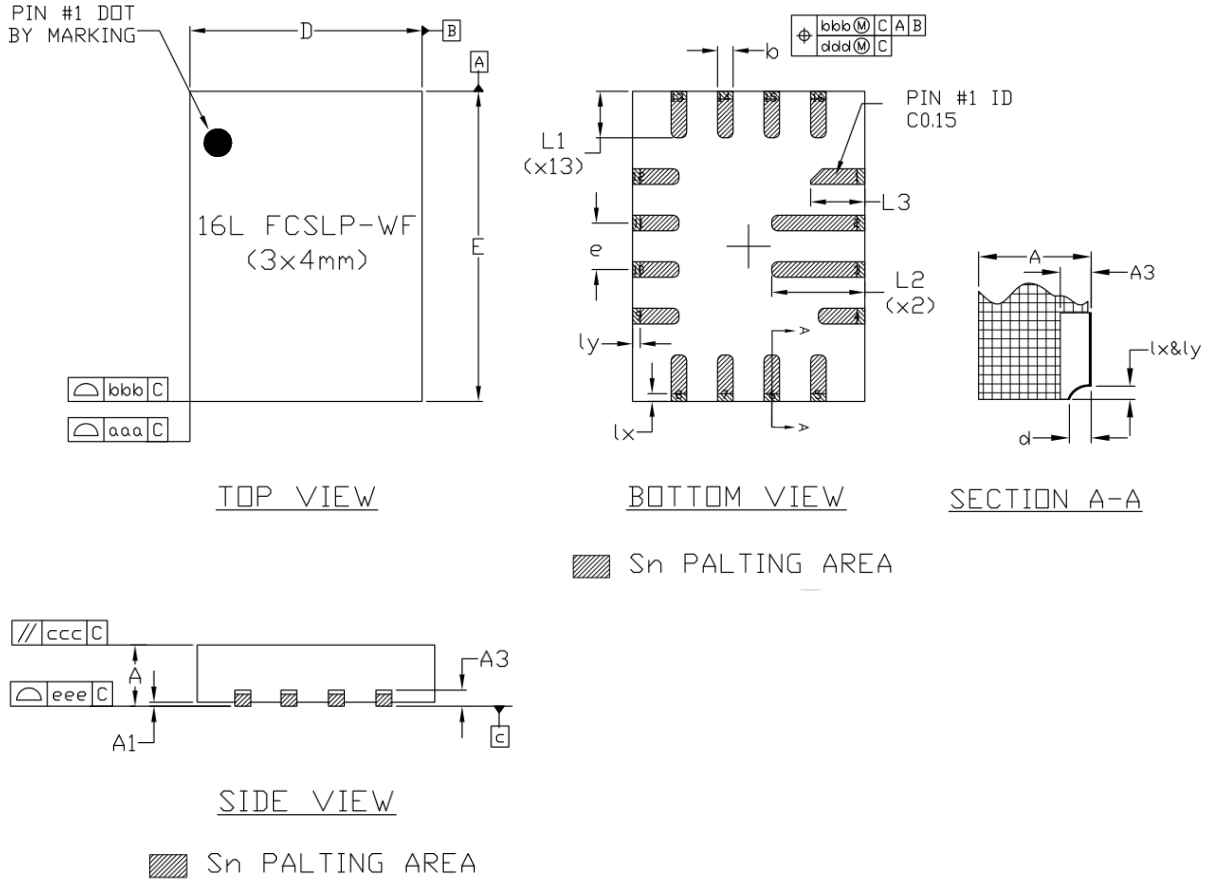
The TMI34030-Q1 includes an open-drain power good (PG) output that indicates whether the regulator output is within ±10% of its nominal output range. When the output voltage moves outside of this range, the PG output is pulled to ground.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from running away thermally. When the silicon die temperature is higher than its upper threshold, the power MOSFETs are shut down. When the temperature is lower than its lower threshold, thermal shutdown is removed and the chip is enabled again.

Tape And Reel Information

QFN3*4-16



Unit: mm

Symbol	Dimensional Ref.			Symbol	Dimensional Ref.		
	Min.	Nom.	Max.		Min.	Nom.	Max.
A	0.800	0.850	0.900	b	0.150	0.200	0.250
A1	---	---	0.050	e	0.600 BSC		
A3	0.203 Ref			L1	0.550	0.600	0.650
D	2.950	3.000	3.050	L2	1.150	1.200	1.250
E	3.950	4.000	4.050	L3	0.650	0.700	0.750
d	0.120	---	0.180	lxly	0.050	---	0.150
Tol. of Form & Position							
aaa	0.10			ddd	0.05		
bbb	0.10			eee	0.08		
ccc	0.10						

Note:

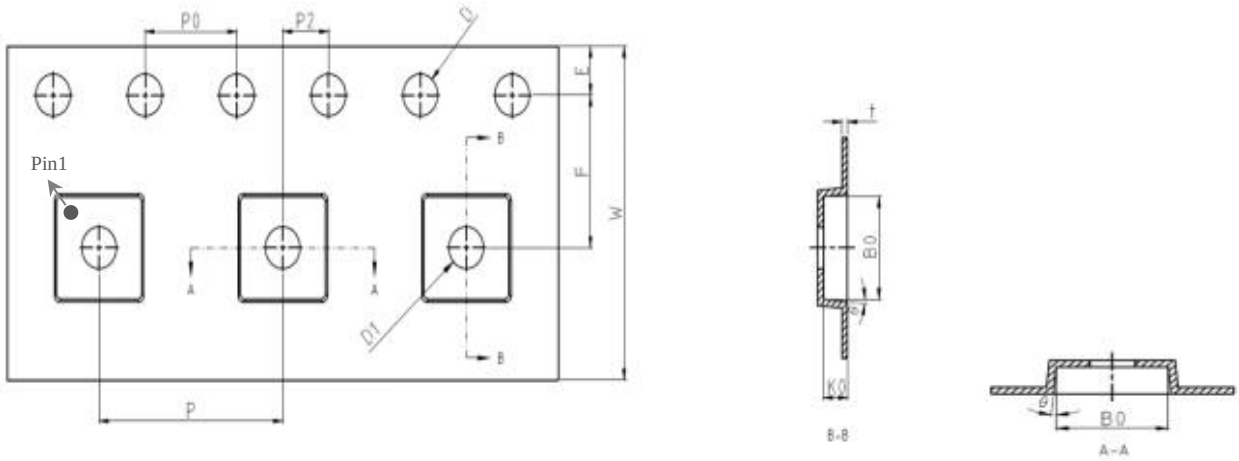
1) All dimensions are in millimeters.

2) Package length does not include mold flash, protrusion or gate burr.

3) Package width does not include inter lead flash or protrusion.

Tape And Reel Information

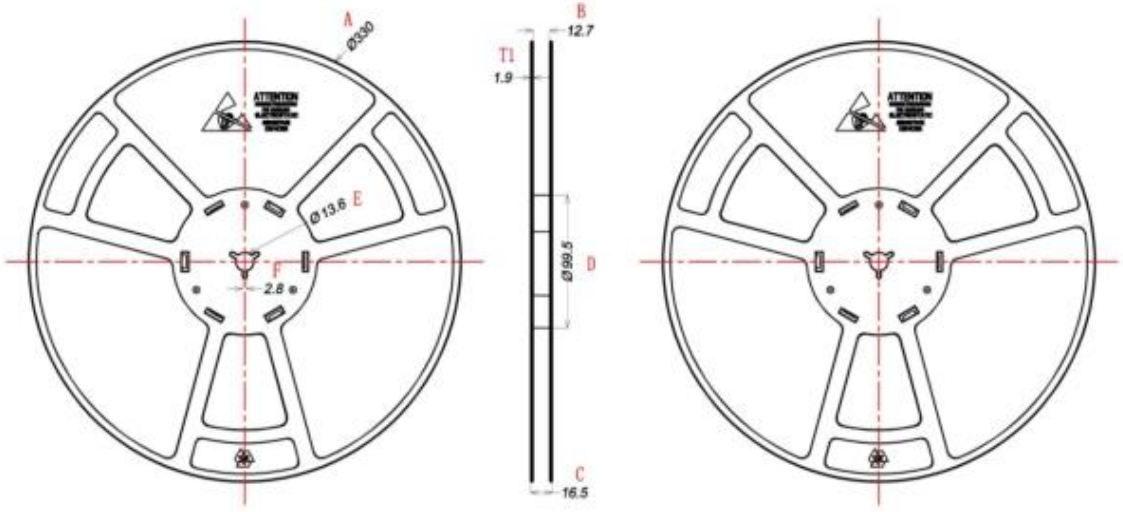
TAPE DIMENSIONS: QFN3x4-16



Unit: mm

Symbol	P	P0	P2	D	A	D1	B
Dimension (mm)	8.00±0.10	4.00±0.10	2.00±0.05	$1.5^{+0.10}_{0}$	3.70±0.10	1.50MIN	4.35±0.10
Symbol	E	F	W	K0	B0	t	θ
Dimension (mm)	1.75±0.10	5.50±0.05	$12^{+0.30}_{-0.10}$	1.05±0.10	4.35±0.10	0.25±0.03	5° TYP

REEL DIMENSIONS: QFN3x4-16



Unit: mm

A	B	C	D	E	F	T1
Ø330±1	12.7±0.5	16.5±0.3	Ø 99.5±0.5	Ø 13.6±0.2	2.8±0.2	1.9±0.2

Note:

1) All Dimensions are in Millimeter
2) Quantity of Units per Reel is 3000
3) MSL level is level 1.

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