PCA9536

4-bit I2C-bus and SMBus I/O port

Rev. 6 — 7 November 2017   **Product data sheet**

1. General description

The PCA9536 is an 8-pin CMOS device that provides 4 bits of General Purpose parallel Input/Output (GPIO) expansion for I2C-bus/SMBus applications and was developed to enhance the NXP Semiconductors family of I2C-bus I/O expanders. I/O expanders provide a simple solution when additional I/O is needed for ACPI power switches, sensors, push buttons, LEDs, fans, etc.

The PCA9536 consists of a 4-bit Configuration register (input or output selection), 4-bit Input Port register, 4-bit Output Port register and a 4-bit Polarity Inversion register (active HIGH or active LOW operation). The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input Port or Output Port register. The polarity of the read register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The power-on reset sets the registers to their default values and initializes the device state machine.

The I2C-bus address is fixed and allows only one device on the same I2C-bus/SMBus.

2. Features and benefits

- 4-bit I2C-bus GPIO
- Operating power supply voltage range of 2.3 V to 5.5 V
- 5 V tolerant I/Os
- Polarity Inversion register
- Low standby current
- Noise filter on SCL/SDA inputs
- No glitch on power-up
- Internal power-on reset
- 4 I/O pins which default to 4 inputs with 100 kΩ internal pull-up resistor
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO8, TSSOP8 (MSOP8), HVSON8

3. Ordering information

| Type number	Topside mark	Package		Version
		Name	**Description**	
PCA9536D	PCA9536	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCA9536DP	9536	TSSOP8[1]	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1
PCA9536TK	9536	HVSON8	plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 × 3 × 0.85 mm	SOT908-1

[1]   Also known as MSOP8.

3.1 Ordering options

Table 2.   Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCA9536D	PCA9536D,112	SO8	STANDARD MARKING * IC'S TUBE - DSC BULK PACK	2000	T_{amb} = −40 °C to +85 °C
	PCA9536D,118	SO8	REEL 13" Q1/T1 *STANDARD MARK SMD	2500	T_{amb} = −40 °C to +85 °C
PCA9536DP	PCA9536DP,118	TSSOP8[1]	REEL 13" Q1/T1 *STANDARD MARK SMD	2500	T_{amb} = −40 °C to +85 °C
PCA9536TK	PCA9536TK,118	HVSON8	REEL 13" Q1/T1 *STANDARD MARK SMD	6000	T_{amb} = −40 °C to +85 °C

4. Block diagram

All I/Os are set to inputs at reset.

Fig 1.   Block diagram of PCA9536
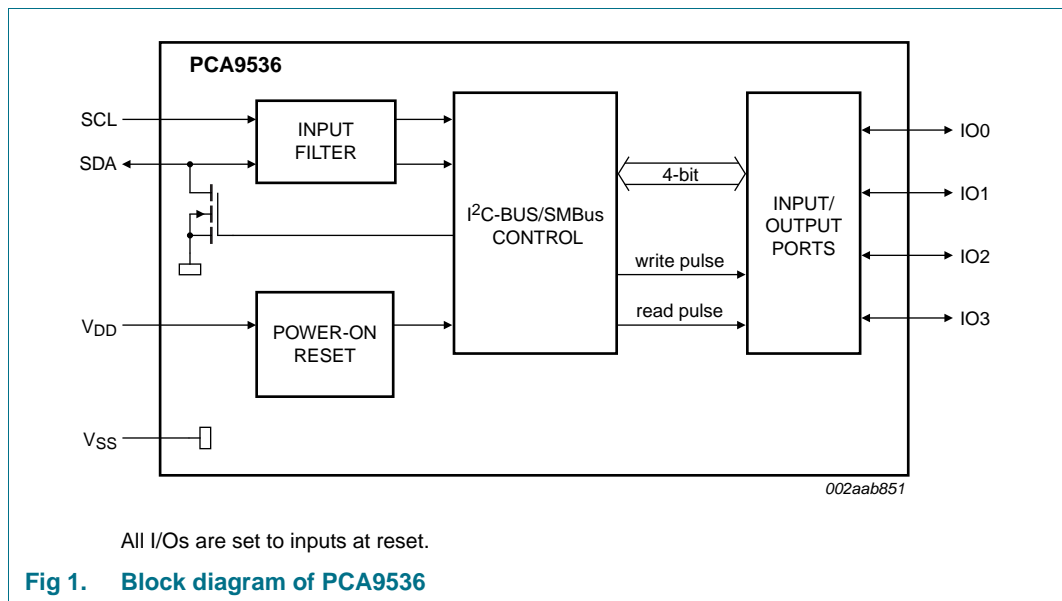
5. Pinning information

5.1 Pinning
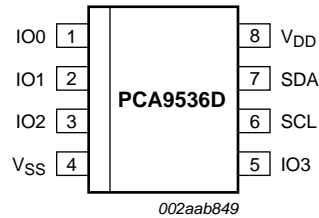
Fig 2.   Pin configuration for SO8
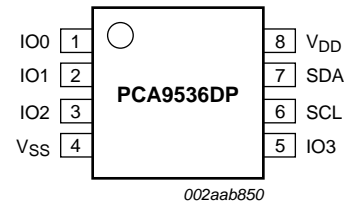
Fig 3.   Pin configuration for TSSOP8

Transparent top view
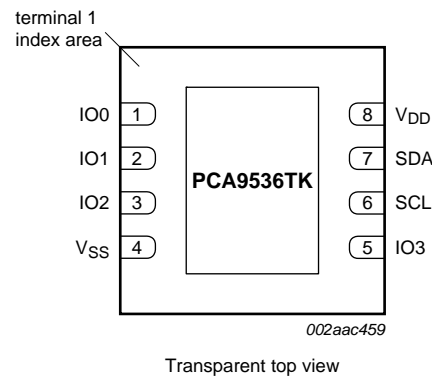
Fig 4.   Pin configuration for HVSON8

5.2 Pin description

Table 3.   Pin description

Symbol	Pin	Description
IO0	1	input/output 0
IO1	2	input/output 1
IO2	3	input/output 2
V_{SS}	4	supply ground
IO3	5	input/output 3
SCL	6	serial clock line
SDA	7	serial data line
V_{DD}	8	supply voltage

6. Functional description

Refer to Figure 1 "Block diagram of PCA9536".

6.1 Registers

6.1.1 Command byte

Table 4.   Command byte

Command	Protocol	Function
0	read byte	Input Port register
1	read/write byte	Output Port register
2	read/write byte	Polarity Inversion register
3	read/write byte	Configuration register

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

6.1.2 Register 0 - Input Port register

This register is a read-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

The default 'X' is determined by the externally applied logic level, normally logic 1 when no external signal externally applied because of the internal pull-up resistors.

Table 5.   Register 0 - Input Port register bit description
*Legend: * default value*

Bit	Symbol	Access	Value	Description
7	I7	read only	1*	not used
6	I6	read only	1*	
5	I5	read only	1*	
4	I4	read only	1*	
3	I3	read only	X	determined by externally applied logic level
2	I2	read only	X	
1	I1	read only	X	
0	I0	read only	X	

6.1.3 Register 1 - Output Port register

This register reflects the outgoing logic levels of the pins defined as outputs by Register 3. Bit values in this register have no effect on pins defined as inputs. Reads from this register return the value that is in the flip-flop controlling the output selection, **not** the actual pin value.

'Not used' bits can be programmed with either logic 0 or logic 1.

Table 6.   Register 1 - Output Port register bit description
*Legend: * default value*

Bit	Symbol	Access	Value	Description
7	O7	R	1*	not used
6	O6	R	1*	
5	O5	R	1*	
4	O4	R	1*	
3	O3	R	1*	reflects outgoing logic levels of pins defined as outputs by Register 3
2	O2	R	1*	
1	O1	R	1*	
0	O0	R	1*	

6.1.4 Register 2 - Polarity Inversion register

This register allows the user to invert the polarity of the Input Port register data. If a bit in this register is set (written with '1'), the corresponding Input Port data is inverted. If a bit in this register is cleared (written with a '0'), the Input Port data polarity is retained.

'Not used' bits can be programmed with either logic 0 or logic 1.

Table 7.   Register 2 - Polarity Inversion register bit description
*Legend: * default value*

Bit	Symbol	Access	Value	Description
7	N7	R/W	0*	not used
6	N6	R/W	0*	
5	N5	R/W	0*	
4	N4	R/W	0*	
3	N3	R/W	0*	inverts polarity of Input Port register data
2	N2	R/W	0*	0 = Input Port register data retained (default value)
1	N1	R/W	0*	
0	N0	R/W	0*	1 = Input Port register data inverted

6.1.5 Register 3 - Configuration register

This register configures the directions of the I/O pins. If a bit in this register is set, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. At reset, the I/Os are configured as inputs with a weak pull-up to V_{DD}.

'Not used' bits can be programmed with either logic 0 or logic 1.

Table 8.   Register 3 - Configuration register bit description
*Legend: * default value*

Bit	Symbol	Access	Value	Description
7	C7	R/W	1*	not used
6	C6	R/W	1*	
5	C5	R/W	1*	
4	C4	R/W	1*	
3	C3	R/W	1*	configures the directions of the I/O pins
2	C2	R/W	1*	0 = corresponding port pin enabled as an output
1	C1	R/W	1*	1 = corresponding port pin configured as input (default value)
0	C0	R/W	1*	

6.2 Power-on reset

When power is applied to V_{DD}, an internal Power-On Reset (POR) holds the PCA9536 in a reset condition until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA9536 registers and state machine will initialize to their default states. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

For a power reset cycle, V_{DD} must be lowered below 0.2 V and then restored to the operating voltage.

6.3 I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input with a weak pull-up (100 kΩ typical) to V_{DD}. The input voltage may be raised above V_{DD} to a maximum of 5.5 V.

If the I/O is configured as an output, then either Q1 or Q2 is enabled, depending on the state of the Output Port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low-impedance paths that exist between the pin and either V_{DD} or V_{SS}.
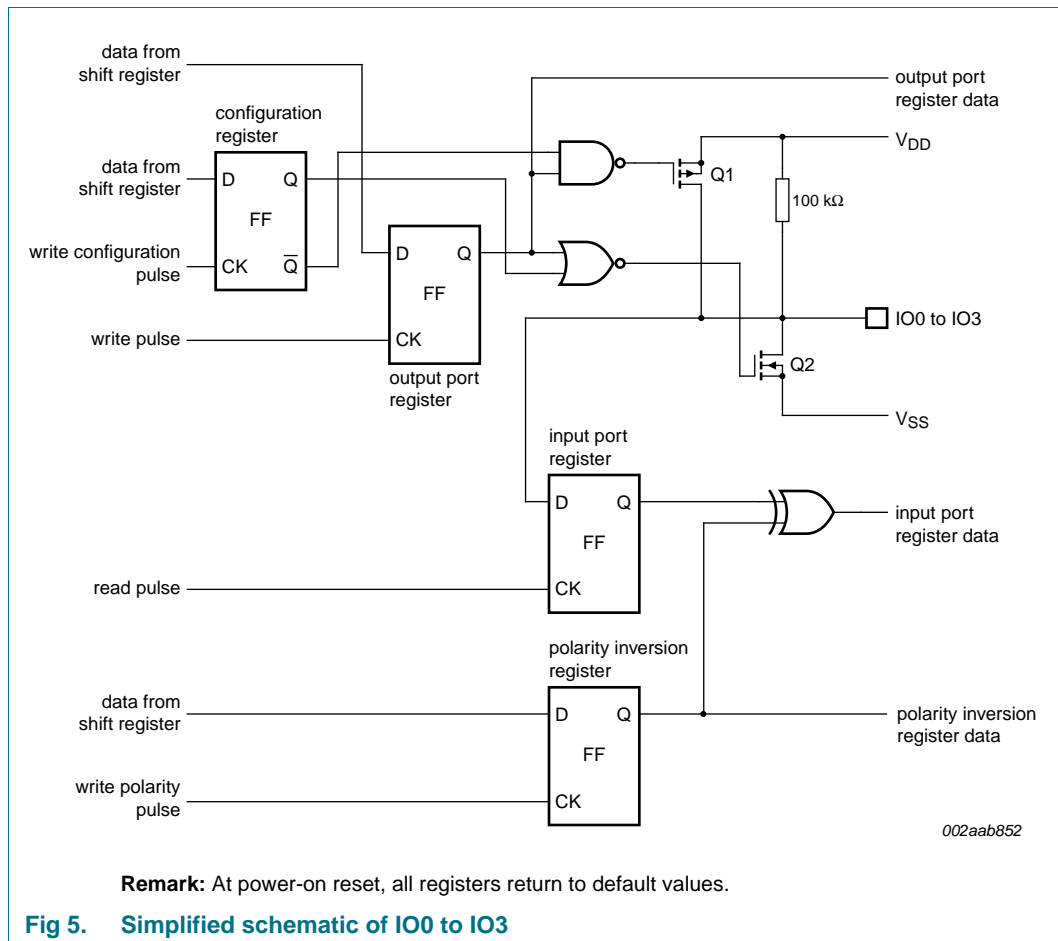
Remark: At power-on reset, all registers return to default values.

Fig 5.   Simplified schematic of IO0 to IO3

6.4 Device address
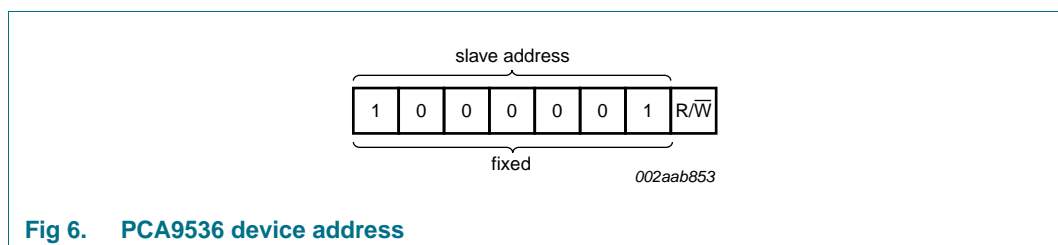
Fig 6.   PCA9536 device address

6.5 Bus transactions

Data is transmitted to the PCA9536 registers using the Write mode as shown in Figure 7 and Figure 8. Data is read from the PCA9536 registers using the Read mode as shown in Figure 9 and Figure 10. These devices do not implement an auto-increment function, so once a command byte has been sent, the register which was addressed will continue to be accessed by reads until a new command byte has been sent.

Fig 7.   Write to Output Port register

Fig 8.   Write to Configuration register or Polarity Inversion register

Fig 9.   Read from register
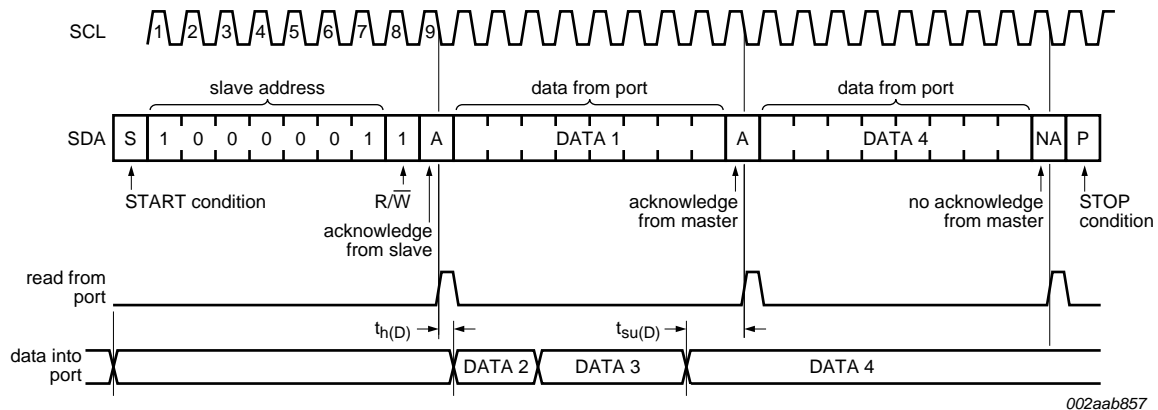
This figure assumes the command byte has previously been programmed with 00h.

Transfer of data can be stopped at any moment by a STOP condition.
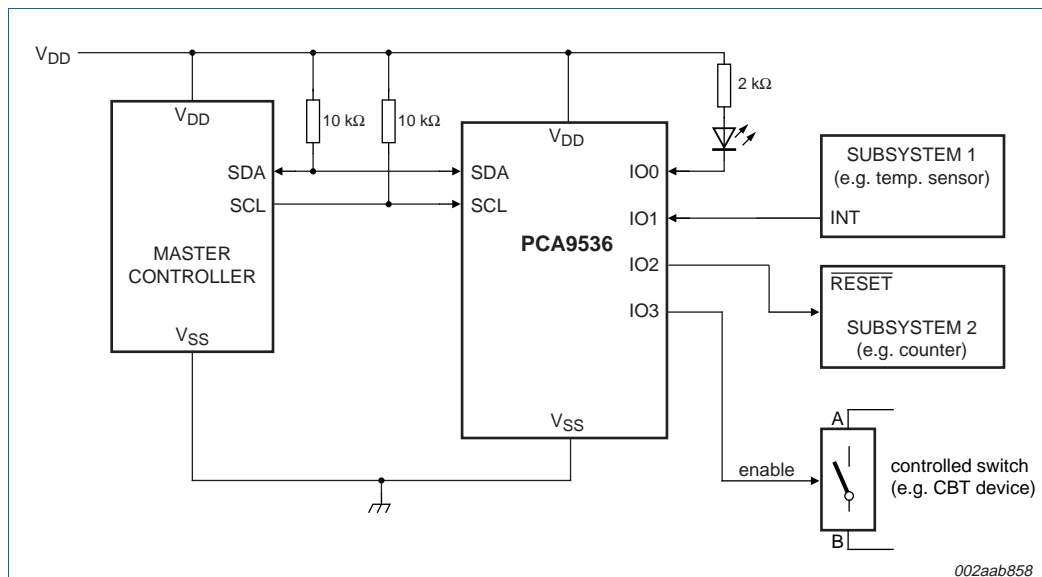
Fig 10. Read Input Port register

7. Application design-in information

Device address is 1000 001X; IO0, IO2, IO3 configured as outputs; IO1 configured as input.

Fig 11. Typical application

8. Limiting values

Table 9.   Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			-0.5	$+6.0$	V
I_I	input current			-	±20	mA
$V_{I/O}$	voltage on an input/output pin			$V_{SS} - 0.5$	5.5	V
$I_{O(IOn)}$	output current on pin IOn			-	±50	mA
I_{DD}	supply current			-	85	mA
I_{SS}	ground supply current			-	100	mA
P_{tot}	total power dissipation			-	200	mW
T_{stg}	storage temperature			-65	$+150$	°C
T_{amb}	ambient temperature			-40	$+85$	°C
$T_{j(max)}$	maximum junction temperature			-	$+125$	°C

9. Static characteristics

Table 10. Static characteristics

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage			2.3	-	5.5	V
I_{DD}	supply current	operating mode; V_{DD} = 5.5 V; no load; f_{SCL} = 100 kHz		-	290	400	µA
I_{stb}	standby current	Standby mode; V_{DD} = 5.5 V; no load; V_I = V_{SS}; f_{SCL} = 0 kHz; I/O = inputs		-	225	350	µA
		Standby mode; V_{DD} = 5.5 V; no load; V_I = V_{DD}; f_{SCL} = 0 kHz; I/O = inputs		-	0.25	1	µA
V_{POR}	power-on reset voltage		[1]	-	1.7	2.2	V
Input SCL; input/output SDA							
V_{IL}	LOW-level input voltage			−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		3	6	-	mA
I_L	leakage current	V_I = V_{DD} = V_{SS}		−1	-	+1	µA
C_i	input capacitance	V_I = V_{SS}		-	6	10	pF
I/Os							
V_{IL}	LOW-level input voltage			−0.5	-	+0.8	V
V_{IH}	HIGH-level input voltage			2.0	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.5 V; V_{DD} = 2.3 V	[2]	8	10	-	mA
		V_{OL} = 0.7 V; V_{DD} = 2.3 V	[2]	10	13	-	mA
		V_{OL} = 0.5 V; V_{DD} = 3.0 V	[2]	8	14	-	mA
		V_{OL} = 0.7 V; V_{DD} = 3.0 V	[2]	10	19	-	mA
		V_{OL} = 0.5 V; V_{DD} = 4.5 V	[2]	8	17	-	mA
		V_{OL} = 0.7 V; V_{DD} = 4.5 V	[2]	10	24	-	mA
V_{OH}	HIGH-level output voltage	I_{OH} = −8 mA; V_{DD} = 2.3 V	[3]	1.8	-	-	V
		I_{OH} = −10 mA; V_{DD} = 2.3 V	[3]	1.7	-	-	V
		I_{OH} = −8 mA; V_{DD} = 3.0 V	[3]	2.6	-	-	V
		I_{OH} = −10 mA; V_{DD} = 3.0 V	[3]	2.5	-	-	V
		I_{OH} = −8 mA; V_{DD} = 4.75 V	[3]	4.1	-	-	V
		I_{OH} = −10 mA; V_{DD} = 4.75 V	[3]	4.0	-	-	V
I_{LIH}	HIGH-level input leakage current	V_{DD} = 3.6 V; V_I = V_{DD}		-	-	1	µA
I_{LIL}	LOW-level input leakage current	V_{DD} = 5.5 V; V_I = V_{SS}		-	-	−100	µA
C_i	input capacitance			-	3.7	5	pF
C_o	output capacitance			-	3.7	5	pF

[1] V_{DD} must be lowered to 0.2 V in order to reset part.

[2]   Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 100 mA.

[3]   The total current sourced by all I/Os must be limited to 85 mA.

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10. Dynamic characteristics

Table 11. Dynamic characteristics

Symbol	Parameter	Conditions		Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
				Min	Max	Min	Max	
f_{SCL}	SCL clock frequency			0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition			4.7	-	1.3	-	µs
$t_{HD;STA}$	hold time (repeated) START condition			4.0	-	0.6	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			4.7	-	0.6	-	µs
$t_{SU;STO}$	set-up time for STOP condition			4.0	-	0.6	-	µs
$t_{HD;DAT}$	data hold time			0	-	0	-	µs
$t_{VD;ACK}$	data valid acknowledge time	[1]		0.3	3.45	0.1	0.9	µs
$t_{VD;DAT}$	data valid time	[2]		300	-	50	-	ns
$t_{SU;DAT}$	data set-up time			250	-	100	-	ns
t_{LOW}	LOW period of the SCL clock			4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock			4.0	-	0.6	-	µs
t_r	rise time of both SDA and SCL signals			-	1000	$20 + 0.1C_b$[3]	300	ns
t_f	fall time of both SDA and SCL signals			-	300	$20 + 0.1C_b$[3]	300	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter			-	50	-	50	ns
Port timing								
$t_{v(Q)}$	data output valid time			-	200	-	200	ns
$t_{su(D)}$	data input set-up time			100	-	100	-	ns
$t_{h(D)}$	data input hold time			1	-	1	-	µs

[1] $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.

[2] $t_{VD;DAT}$ = minimum time for SDA data output to be valid following SCL LOW.

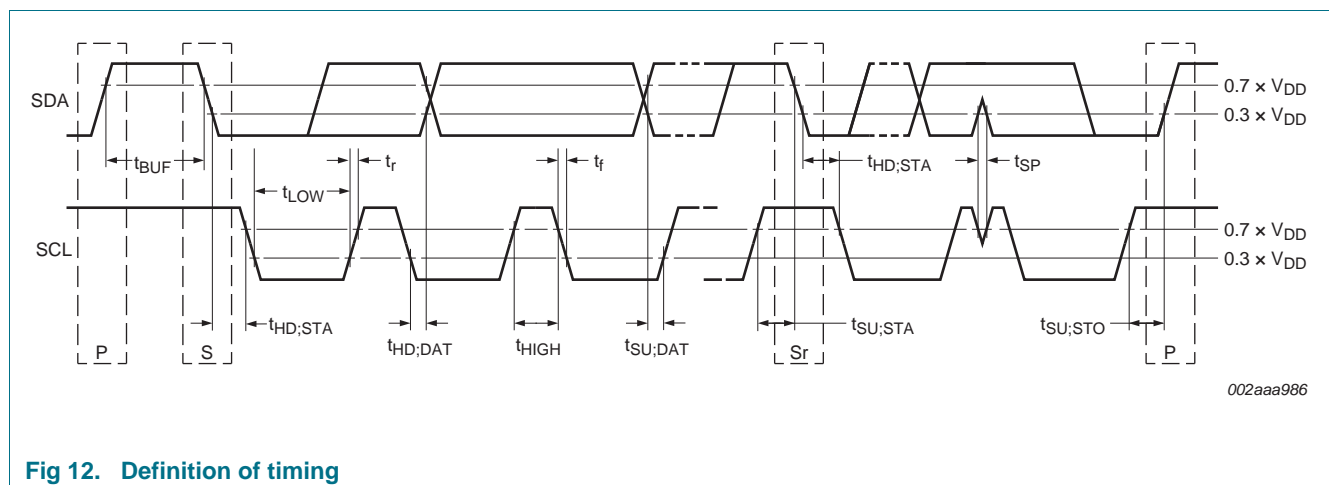[3] C_b = total capacitance of one bus line in pF.
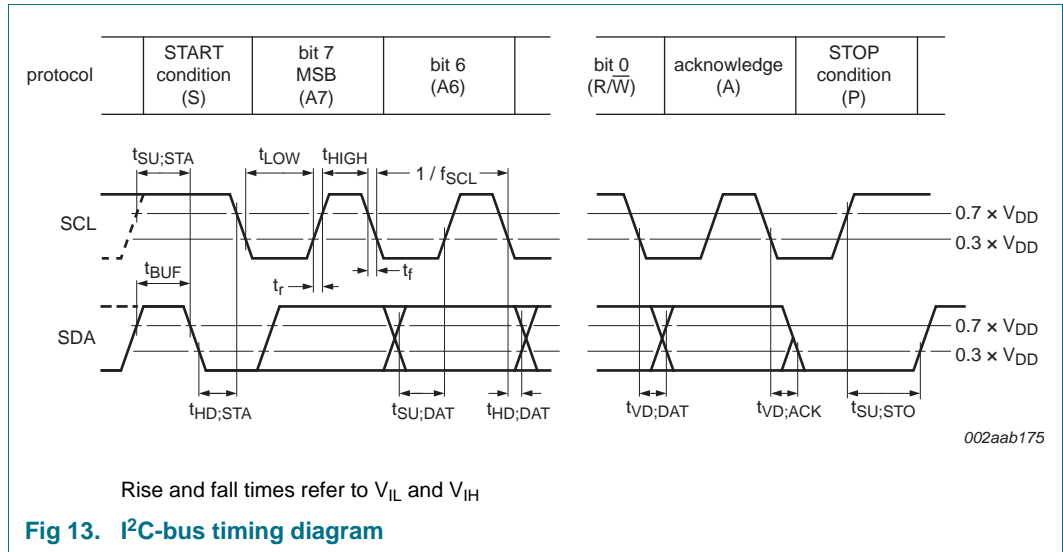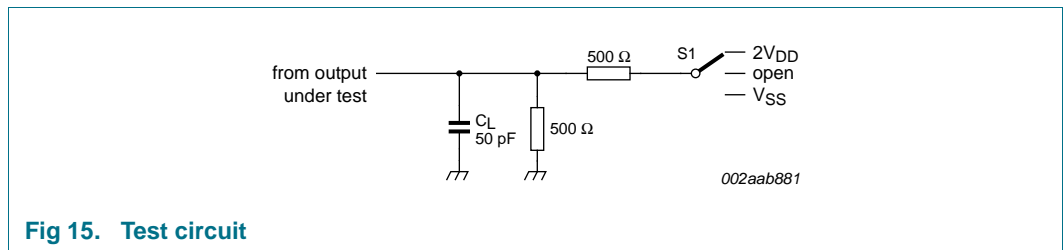

Fig 12. Definition of timing

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Rise and fall times refer to V_{IL} and V_{IH}

Fig 13. I²C-bus timing diagram

11. Test information

R_L = load resistor.

C_L = load capacitance includes jig and probe capacitance.

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generators.

Fig 14. Test circuitry for switching times

Fig 15. Test circuit

Table 12.   Test data

Test	Load		Switch
	C_L	R_L	
$t_{V(Q)}$	50 pF	500 Ω	$2V_{DD}$

12. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D[1]	E[2]	e	HE	L	Lₚ	Q	v	w	y	Z[1]	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

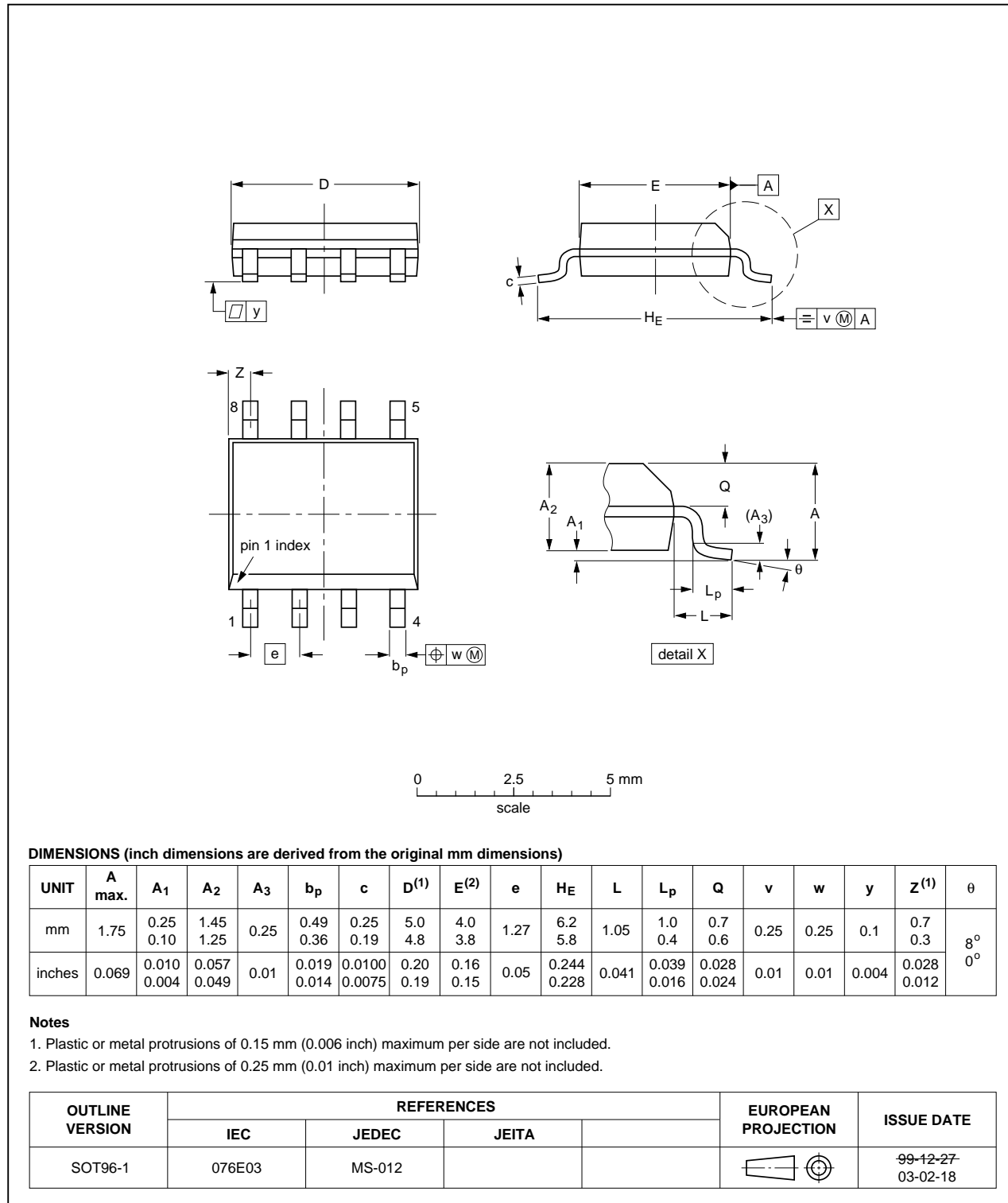| OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 16. Package outline SOT96-1 (SO8)

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm   **SOT505-1**

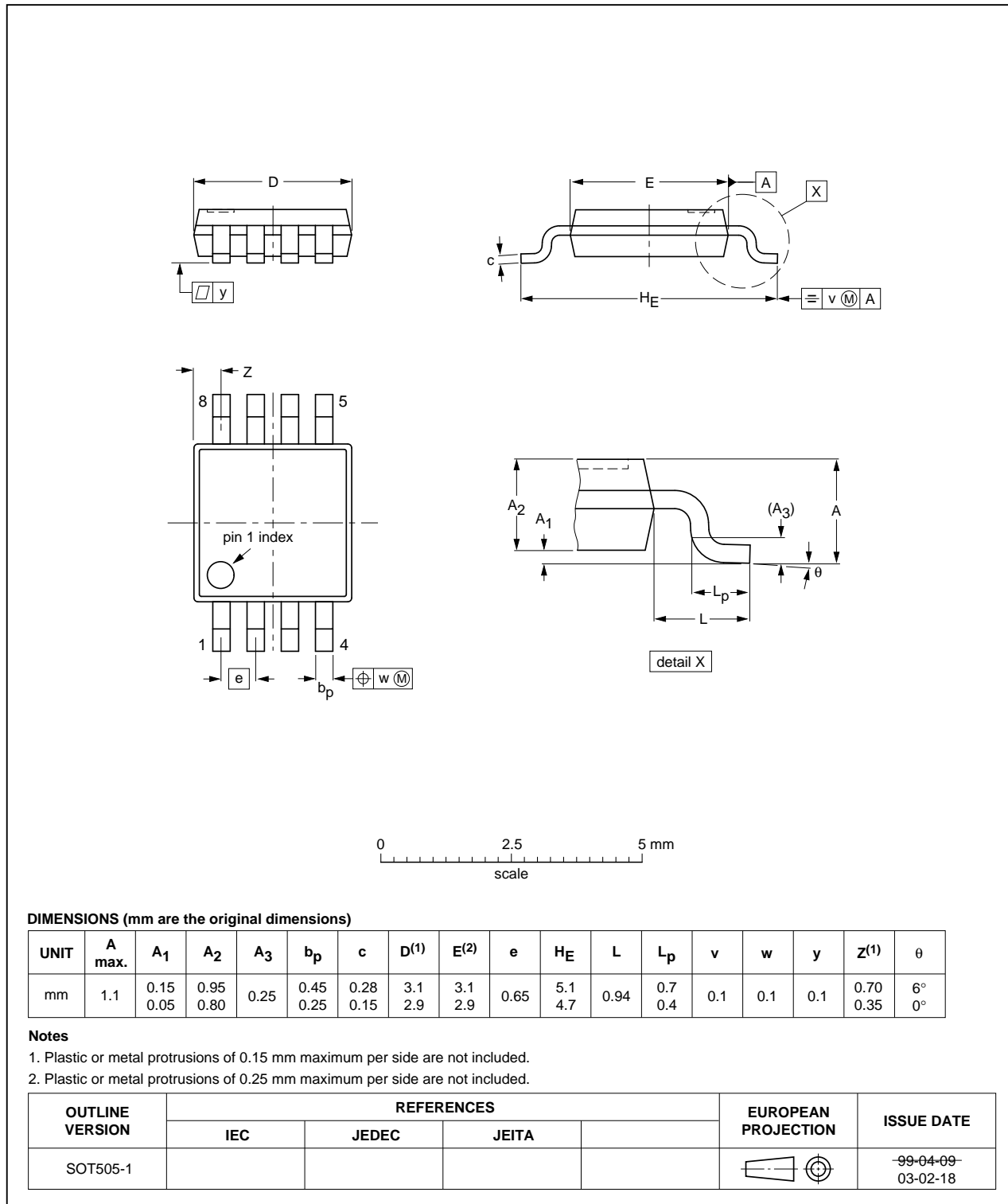**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A₁	A₂	A₃	bp	c	D[1]	E[2]	e	HE	L	Lp	v	w	y	Z[1]	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

Fig 17. Package outline SOT505-1 (TSSOP8)

HVSON8: plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 x 3 x 0.85 mm

SOT908-1

DIMENSIONS (mm are the original dimensions)

UNIT	A$^{(1)}$ max.	A$_1$	b	c	D$^{(1)}$	D$_h$	E$^{(1)}$	E$_h$	e	e$_1$	L	v	w	y	y$_1$
mm	1	0.05 0.00	0.3 0.2	0.2	3.1 2.9	2.25 1.95	3.1 2.9	1.65 1.35	0.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT908-1		MO-229				05-09-26 05-10-05
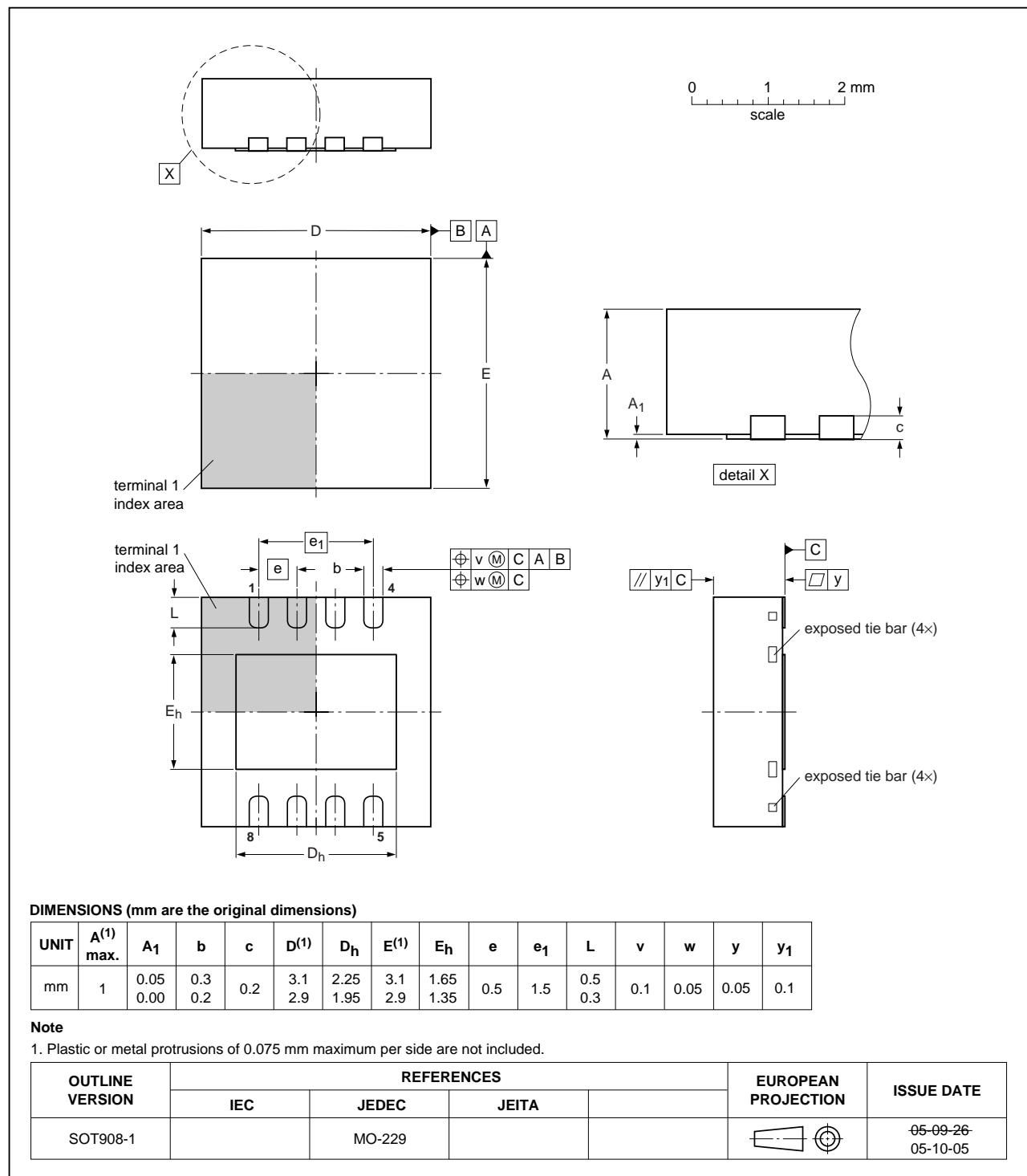
Fig 18. Package outline SOT908-1 (HVSON8)

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13. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 19) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 13 and 14

Table 13. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	$\geq$ 350
< 2.5	235	220
$\geq$ 2.5	220	220

Table 14. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 19.

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Fig 19. Temperature profiles for large and small components

MSL: Moisture Sensitivity Level
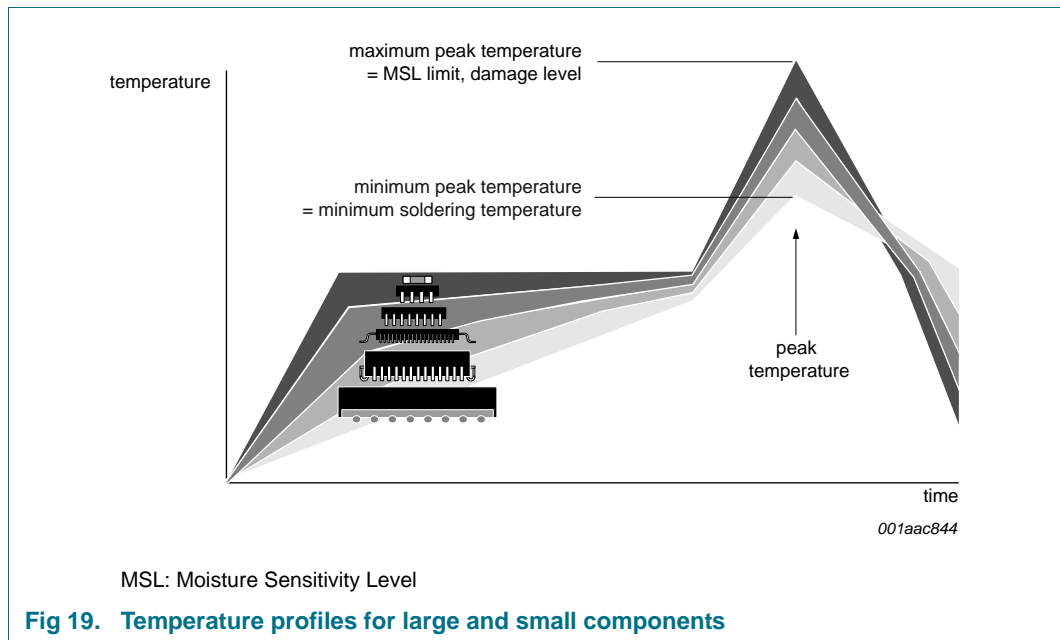
For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

15. Abbreviations

Table 15.   Abbreviations

Acronym	Description
ACPI	Advanced Configuration and Power Interface
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
GPIO	General Purpose Input/Output
HBM	Human Body Model
I²C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LED	Light-Emitting Diode
MM	Machine Model
POR	Power-On Reset
SMBus	System Management Bus

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16. Revision history

Table 16.   Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9536 v.6	20171107	Product data sheet	201710002I	PCA9536_5
Modifications:	• Table 10 "Static characteristics": Corrected V_{POR} typ and max limit • Added Section 3.1 "Ordering options"			
PCA9536_5	20100125	Product data sheet	-	PCA9536_4

Modifications:	• Table 10 "Static characteristics", sub-section "Supplies":
	  – I_{DD} Typical value changed from "104 μA" to "290 μA"
	  – I_{DD} Maximum value changed from "175 μA" to "400 μA"
	• Table 11 "Dynamic characteristics": Unit for "t_f, fall time of both SDA and SCL signals" changed from "μs" to "ns"
	
	Remark: The changes made in this revision are to correct typographical errors only. There is no change in the performance of the device.			

PCA9536_4	20070911	Product data sheet	-	PCA9536_3
PCA9536_3	20061009	Product data sheet	-	PCA9536_2
PCA9536_2 (9397 750 14124)	20040930	Objective data sheet	-	PCA9536_1
PCA9536_1 (9397 750 12895)	20040820	Objective data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1]   Please consult the most recently issued document before initiating or completing a design.

[2]   The term 'short data sheet' is explained in section "Definitions".

[3]   The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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