2-Bit Bi-Directional Level Shifter with Automatic Sensing & Ultra Tiny Package

Description

The LXS0102 is a 2-bit configurable dual supply bidirectional auto sensing translator that does not require a directional control pin. The A and B ports are designed to track two different power supply rails, V_{CCA} and V_{CCB} respectively. This allows bidirectional translation between lower and higher logic signal levels.

When the OE pin is low, all I/Os are configured to be high-impedance state.

Power-off protection is implemented to prevent current passing through the device when it is powered-down.

Application(s)

- I2C, SMBus, MDIO
- Low Voltage ASIC Level Translation
- Mobile Phones, PDAs, Cameras

Block Diagram

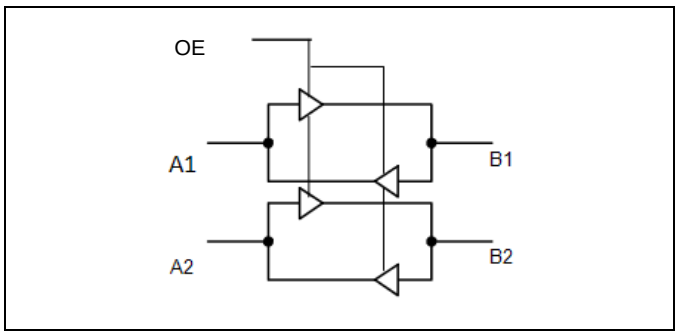


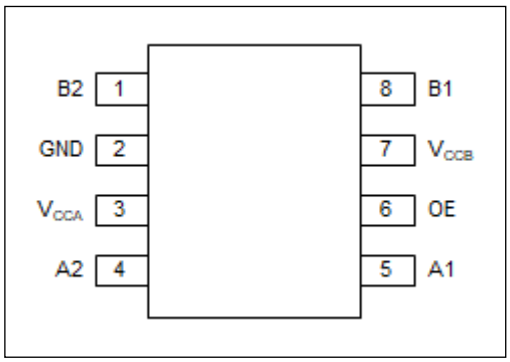
Figure 1. Block Diagram

Features

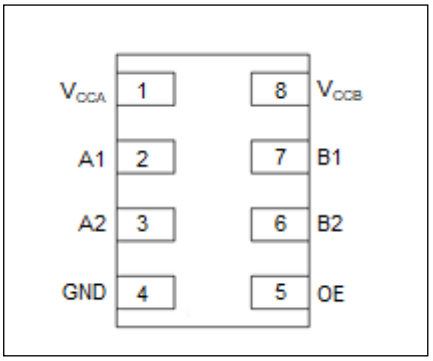
- High–Speed with 24Mb/s Data Rate for push-pull applications
- High–Speed with 2Mb/s Data Rate for open-drain applications
- 1.65V to 3.6V on A Port and 2.3V to 5.5V on B Port
- V_{CCA} must be less than or equal to V_{CCB}
- No Direction-Control Signal Needed
- Low Bit-to-Bit Skew
- Non-preferential Power-up Sequencing
- ESD protection exceeds JESD22-A114
  - A Port: 2000V HBM
  - B Port: 5KV HBM – V, SS, HK
    7KV HBM – GBA only
- Integrated 10kΩ Pull-up Resistors
- Packaging (Pb-free & Green):
  - 8-DFN1x1.4 (HK)
  - 8-VSSOP (V)
  - 8-SSOP (SS)
  - 8-WLCSP (GBA)
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. “Green” Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

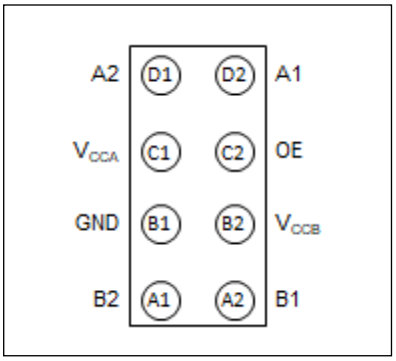
Pin Configuration



SSOP-8/VSSOP-8 (TOP VIEW)



UDFN-8 (TOP VIEW)



WLCSP (BOTTOM VIEW)

Pin Description

Pin Name	Pin Number			Type	Description
	SSOP VSSOP	DFN	WLCSP		
V_{CCA}	3	1	C1	Power	A-port supply voltage.1.65V ≤ V_{CCA} ≤ 3.6V
V_{CCB}	7	8	B2	Power	B-port supply voltage. 2.3V ≤ V_{CCB} ≤ 5.5V
A1	5	2	D2	I/O	Input/output A. Referenced to V_{CCA}.
A2	4	3	D1	I/O	Input/output A. Referenced to V_{CCA}
B1	8	7	A2	I/O	Input/output B. Referenced to V_{CCB}
B2	1	6	A1	I/O	Input/output B. Referenced to V_{CCB}
OE	6	5	C2	Input	Output enable (active High). Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}
GND	2	4	B1	GND	Ground.

Maximum Ratings

Storage Temperature .....-65°C to +150°C
DC Supply Voltage Port B.....-0.5V to +6.5V
DC Supply Voltage Port A.....-0.5V to +4.6V
Vi(A) Referenced DC Input Voltage .....-0.5V to +4.6V
Vi(B) Referenced DC Input Voltage.....-0.5V to +6.5V
Enable Control Pin DC Input Voltage.....-0.5V to +4.6V
Continuous Output Current, I/O 45mA

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CCA}	V_{CCA} Positive DC Supply Voltage	1.65		3.6	V
V_{CCB}	V_{CCB} Positive DC Supply Voltage	2.3		5.5	V
V_{OE}	Enable Control Pin Voltage	GND		3.6	V
V_{IO}	I/O Pin Voltage (A1, A2)	GND		VCCA	V
	I/O Pin Voltage (B1, B2)	GND		VCCB	V
Δt / Δv	Input transition rise or fall time				
	A or B port Push-Pull Driving, (V_{CCA} = 1.65V to 3.6V, V_{CCB} = 2.3V to 5.5V)			10	ns/V
	OE (V_{CCA} = 1.65V to 3.6V, V_{CCB} = 2.3V to 5.5V)			10	ns/V
T_A	Operating Temperature Range	−40		+85	°C

DC Electrical Characteristics

V_{CCI} is the supply voltage associated with the input port. V_{CCO} is the supply voltage associated with the output port.

Symbol	Parameter	Test Conditions	V_{CCA}	V_{CCB}	Temp.	Min	Typ	Max	Unit
V_{IHB}	B port Input HIGH Voltage	I_{OHA} = -20uA, V_{IA} = V_{CCA} x 0.67	1.65V to 3.6V	2.3V to 5.5V	-40 to 85°C	V_{CCI} – 0.4			V
V_{ILB}	B port Input LOW Voltage	I_{OLA} = 1mA, V_{IA} = 0.4V	1.65V to 3.6V	2.3V to 5.5V	-40 to 85°C			0.15	V
V_{IHA}	A port Input HIGH Voltage	I_{OHB}= -20uA, V_{IB} = V_{CCB} x 0.67	1.65V to 1.95V	2.3V to 5.5V	-40 to 85°C	V_{CCI} – 0.2			V
			1.65V to 3.6V	2.3V to 5.5V		V_{CCI} – 0.4			V
V_{ILA}	A port Input LOW Voltage	I_{OLB} = 1mA, V_{IB} = 0.4V	1.65V to 3.6V	2.3V to 5.5V	-40 to 85°C			0.15	V
V_{IH}	Control Pin Input HIGH Voltage		1.65V to 3.6V	2.3V to 5.5V	-40 to 85°C	V_{CCA}x0.65			V
V_{IL}	Control Pin Input LOW Voltage		1.65V to 3.6V	2.3V to 5.5V	-40 to 85°C			V_{CCA}x0.35	V
V_{OHB}	B port Output HIGH Voltage	I_{OHB} = -20uA, $V_{IA} \geq V_{CCA}$–0.4V	1.65V to 3.6V	2.3V to 5.5V	-40 to 85°C	0.67xV_{CCB}			V
V_{OLB}	B port Output LOW Voltage	I_{OLB} = 1mA, $V_{IA} \leq$ 0.15V	1.65V to 3.6V	2.3V to 5.5V	-40 to 85°C			0.4	V
V_{OHA}	A port Output HIGH Voltage	I_{OHA} = -20uA, $V_{IB} \geq V_{CCB}$–0.4V	1.65V to 3.6V	2.3V to 5.5V	-40 to 85°C	0.67*V_{CCA}			V
V_{OLA}	A port Output LOW Voltage	I_{OLA} = 1mA, $V_{IB} \leq$ 0.15V	1.65V to 3.6V	2.3V to 5.5V	-40 to 85°C			0.4	V
I_I	Input Leakage	OE	1.65V to	2.3V to 5.5V	25°C			±1	µA

Symbol	Parameter	Test Conditions	V_{CCA}	V_{CCB}	Temp.	Min	Typ	Max	Unit
	Current		3.6V		-40 to 85°C			±2	
I_{OFF}	Partial Power Down Current	A port	0V	0V to 5.5V	25°C			±1	µA
					-40 to 85°C			±2	
		B port	0V to 5.5V	0V	25°C			±1	
					-40 to 85°C			±2	
I_{OZ}	Off-state Leakage Current	A or B port	1.65V to 3.6V	2.3V to 5.5V	25°C			±1	µA
					-40 to 85°C			±2	
I_{QVCCA}	V_{CCA} Supply Current	$V_I = V_O$ = open, $I_O = 0$	1.65V to 3.6V	2.3V to 5.5V	-40 to 85°C			2.8	µA
			3.6V	0V	-40 to 85°C			2.2	
			0V	5.5V	-40 to 85°C			-1	
I_{QVCCB}	V_{CCB} Supply Current	$V_I = V_O$ = open, $I_O = 0$	1.65V to 3.6V	2.3V to 5.5V	-40 to 85°C			12	µA
			3.6V	0V	-40 to 85°C			-1	
			0V	5.5V	-40 to 85°C			1	
I_{QVCCA} + I_{QVCCB}	Total Supply Current	$V_I = V_O$ = open, $I_O = 0$	1.65V to 3.6V	2.3V to 5.5V	-40 to 85°C			14.4	µA
C_I	Input Capacitance	OE	3.3V	3.3V	25°C		2.5		pF
					-40 to 85°C			4.8	
C_{IO}	Input-to-output Capacitance	A or B port	3.3V	3.3V	25°C		10		pF
					-40 to 85°C				
		A port	0V	0V	25°C		5		
					-40 to 85°C		6		
		B port	0V	0V	25°C		6		
					-40 to 85°C		7.5		

AC Electrical Characteristics

(Unless otherwise specified, -40°C ≤ T_A ≤ 85°C)
I/O test circuits of Figures 2, 3, 4 & 5, C_{LOAD} = 15pF, R_{LOAD} = 1MΩ, input pulse generator having the following characteristics: Z_O = 50Ω, PRR ≤ 10MHz, dv/dt ≥ 1V / ns
V_{CCA} = 1.8V ± 0.15V

Symbol	Parameter	Test Conditions	V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		V_{CCB} = 5.0V ± 0.5V		Unit
			Min	Max	Min	Max	Min	Max	
$t_{PHL-A-B}$	High to Low propagation delay	Push-pull driving		5.3		5.4		6.8	ns
		Open-Drain driving		8.8		9.6		10	
$t_{PLH-A-B}$	Low to High propagation delay	Push-pull driving		6.8		7.1		7.5	ns
		Open-Drain driving		260		208		198	
$t_{PHL-B-A}$	High to Low propagation delay	Push-pull driving		4.4		4.5		4.7	ns
		Open-Drain driving		5.3		4.4		4	
$t_{PLH-B-A}$	Low to High propagation delay	Push-pull driving		5.3		4.5		0.5	ns
		Open-Drain driving		175		140		102	
ten	Enable Time	OE to A or B		200		200		200	ns
tdis	Disable Time	OE to A or B		230		230		230	ns
t_{RA}	A port Rise Time	Push-pull driving	3.2	9.5	2.3	9.3	2	7.6	ns
		Open-Drain driving	32.8	165	27.9	132	20.5	95	
t_{RB}	B port Rise Time	Push-pull driving	2.8	10.8	2.7	9.1	2.1	7.6	ns
		Open-Drain driving	30	145	23	106	10	58	
t_{FA}	A port Fall Time	Push-pull driving	2	5.9	1.9	6	1.7	13.3	ns
		Open-Drain driving	3	6.9	3	6.4	3.1	6.1	
t_{FB}	B port Fall Time	Push-pull driving	2.9	13.8	2.8	16.2	2.8	16.2	ns
		Open-Drain driving	3.1	13.8	3.2	16.2	3.9	16.2	
t_{PPSKEW}	Channel-to-Channel Skew			0.7		0.7		0.7	ns
f_{DATA}	Maximum Data Rate	Push-pull driving	21		22		24		Mbps
		Open-Drain driving	2		2		2		

V_{CCA} = 2.5V ± 0.2V

Symbol	Parameter	Test Conditions	V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		V_{CCB} = 5.0V ± 0.5V		Unit
			Min	Max	Min	Max	Min	Max	
$t_{PHL-A-B}$	High to Low propagation delay	Push-pull driving		3.2		3.7		3.8	ns
		Open-Drain driving		6.3		6		5.8	
$t_{PLH-A-B}$	Low to High propagation delay	Push-pull driving		3.5		4.1		4.4	ns
		Open-Drain driving		250		206		190	
$t_{PHL-B-A}$	High to Low propagation delay	Push-pull driving		3		3.6		4.3	ns
		Open-Drain driving		4.7		4.2		4	
$t_{PLH-B-A}$	Low to High propagation delay	Push-pull driving		3.4		1.6		1	ns
		Open-Drain driving		170		140		103	
ten	Enable Time	OE to A or B		200		200		200	ns
tdis	Disable Time	OE to A or B		230		230		230	ns
t_{RA}	A port Rise Time	Push-pull driving	2.8	7.4	2.6	6.6	1.8	5.6	ns
		Open-Drain driving	24.9	149	22.8	121	18.4	89	
t_{RB}	B port Rise Time	Push-pull driving	2.7	8.3	2.4	7.2	2	6.1	ns
		Open-Drain driving	25.5	151	20.5	112	12	64	
t_{FA}	A port Fall Time	Push-pull driving	1.9	5.7	1.9	5.5	1.8	5.3	ns
		Open-Drain driving	2.9	6.9	2.9	6.2	2.9	5.8	
t_{FB}	B port Fall Time	Push-pull driving	2.2	7.8	2.4	6.7	2.6	6.6	ns
		Open-Drain driving	3	8.8	2.9	9.4	3.1	10.4	
t_{PPSKEW}	Channel-to-Channel Skew			0.7		0.7		0.7	ns
f_{DATA}	Maximum Data Rate	Push-pull driving	20		22		24		Mbps
		Open-Drain driving	2		2		2		

V_{CCA} = 3.3V ± 0.3V

Symbol	Parameter	Test Conditions	V_{CCB} = 3.3V ± 0.3V		V_{CCB} = 5.0V ± 0.5V		Unit
			Min	Max	Min	Max	
$t_{PHL-A-B}$	High to Low propagation delay	Push-pull driving		2.4		3.1	ns
		Open-Drain driving		4.2		4.6	
$t_{PLH-A-B}$	Low to High propagation delay	Push-pull driving		4.2		4.4	ns
		Open-Drain driving		204		165	
$t_{PHL-B-A}$	High to Low propagation delay	Push-pull driving		2.5		3.3	ns
		Open-Drain driving		124		97	
$t_{PLH-B-A}$	Low to High propagation delay	Push-pull driving		2.5		2.6	ns
		Open-Drain driving		139		105	
ten	Enable Time	OE to A or B		200		200	ns
tdis	Disable Time	OE to A or B		230		230	ns
t_{RA}	A port Rise Time	Push-pull driving	2.3	5.6	1.9	4.8	ns
		Open-Drain driving	17.4	116	15.4	85	
t_{RB}	B port Rise Time	Push-pull driving	2.5	6.4	2.1	7.4	ns
		Open-Drain driving	17.7	116	11.8	72	
t_{FA}	A port Fall Time	Push-pull driving	2	5.4	1.9	5	ns
		Open-Drain driving	2.8	6.1	2.8	5.7	
t_{FB}	B port Fall Time	Push-pull driving	2.3	7.4	2.4	7.6	ns
		Open-Drain driving	2.8	7.6	2.9	8.3	
t_{PPSKEW}	Channel-to-Channel Skew			0.7		0.7	ns
f_{DATA}	Maximum Data Rate	Push-pull driving	23		24		Mbps
		Open-Drain driving	2		2		

Test Circuits

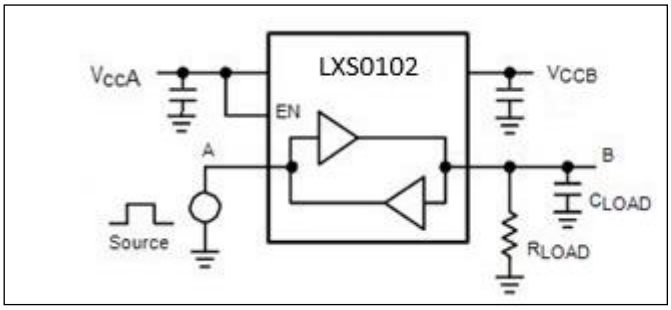


Figure 2. Push-Pull Driving A

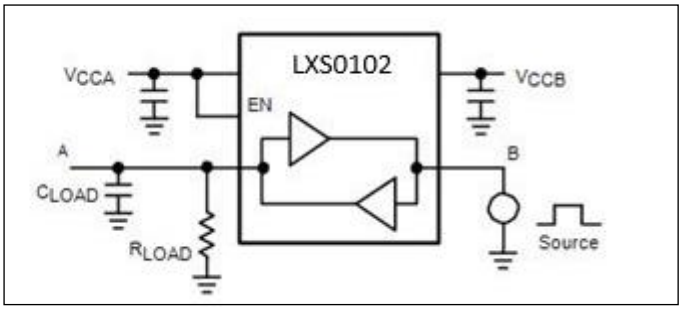


Figure 3. Push-Pull Driving B

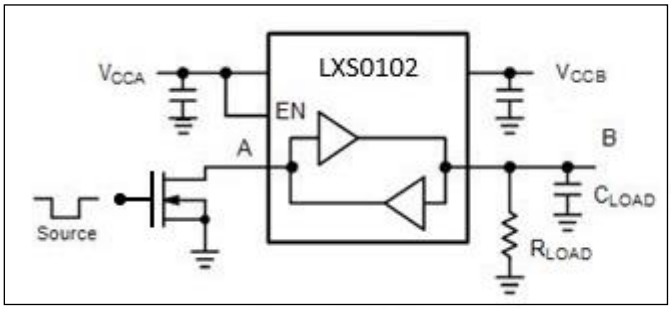


Figure 4. Open-Drain Driving A

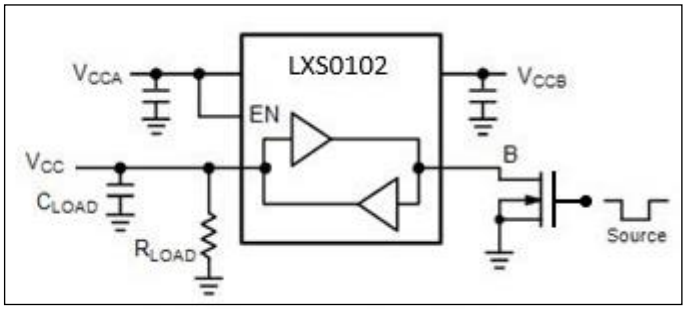
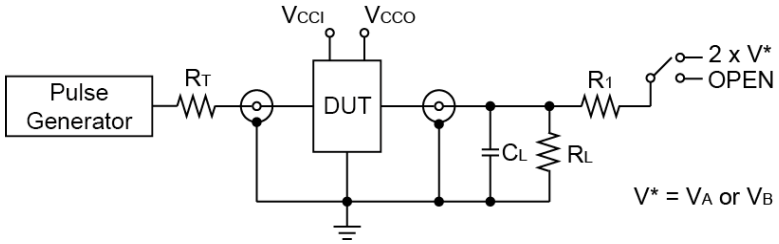


Figure 5. Open-Drain Driving B



Test	Switch
t_{PZH}, t_{PHZ}	Open
t_{PZL}, t_{PLZ}	2 x V*

C_L = 15pF
$R_L = R_1$ = 50kΩ
$R_T = Z_{OUT}$ of pulse generator (Typically 50Ω)
V* = V_A or V_B for A or B measurements, respectively.

Figure 6. Test Circuit for Enable/Disable Time Measurement

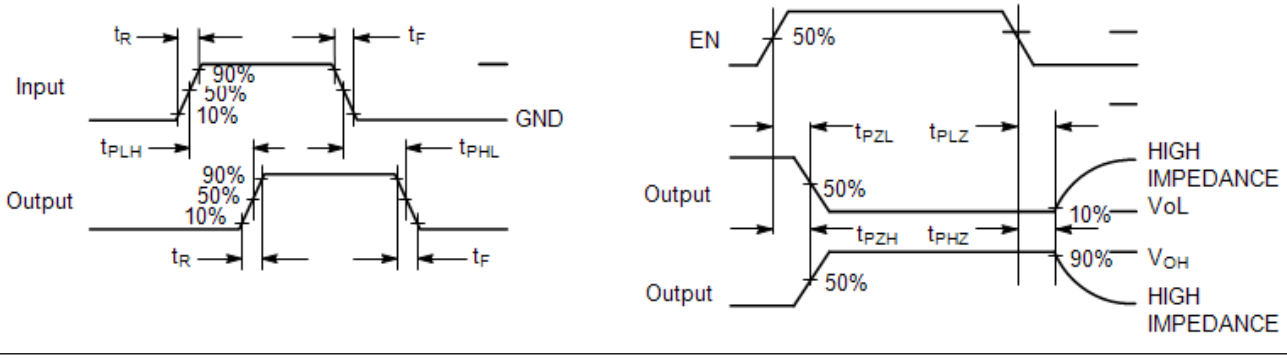


Figure 7. Timing Definitions for Propagation Delays and Enable/Disable Measurement

Functional Description

Level Translator Architecture

The LXS0102 is a 2-bit configurable dual supply bidirectional auto sensing translator that does not require a directional control pin. The A port operating voltage range is from 1.65 V to 3.6 V, and the B port operating voltage range is from 2.3 V to 5.5 V. Figure 8 shows its architecture.

The translator has integrated a 10 kΩ pull−up resistor on each I/O line. The integrated pull-up resistors are used to pull the I/O lines to either V_{CCA} or V_{CCB}. When OE goes low, the pull-up resistors are disabled. There is a NMOS transistor that connects the A-port and B-port. In addition, each output has integrated an one-shot rising edge detector to turn on the PMOS transistor within a short duration to improve the low-to-high transition.

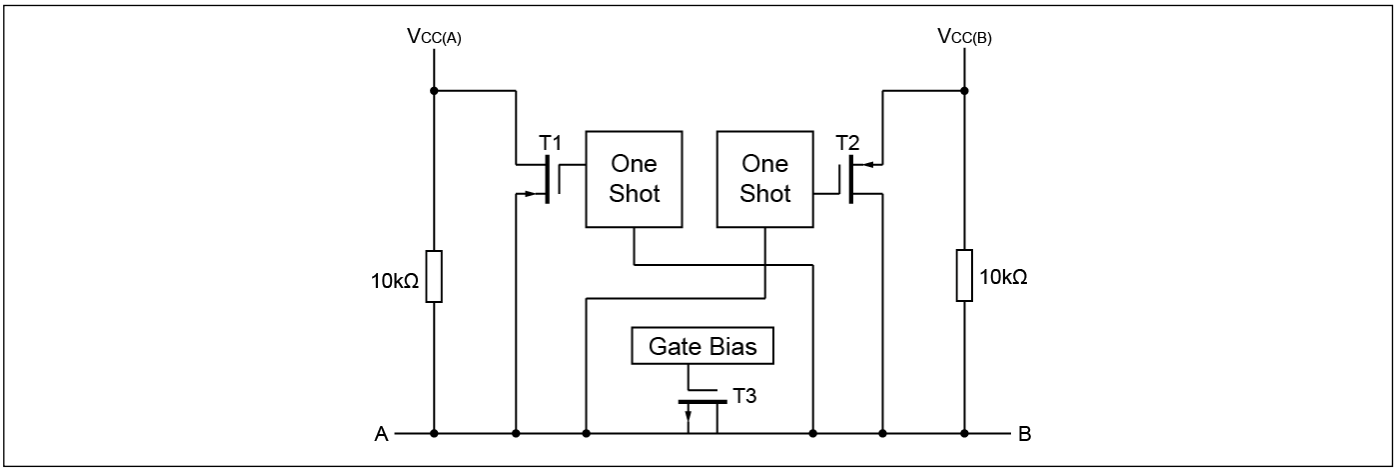


Figure 8. Architecture of LXS0102 I/O Cell (one channel)

Input Driver Requirements

The rise (t_R) and fall (t_F) timing parameters of the open drain outputs depend on the magnitude of the pull−up resistors. In addition, the propagation times (t_{PD}) and maximum data rate depend on the impedance of the device that is connected to the translator. The timing parameters listed in the data sheet assume that the output impedance of the drivers connected to the translator is less than 50 Ω.

Output Enable and Disable (OE)

The LXS0102 has an Output Enable pin (OE) that enables the device by setting HIGH. Driving the Output Enable pin to a low logic level will minimize the power consumption of the device and set all I/Os in high-impedance OFF state. Normal translation operation occurs when the OE pin is equal to a logic high signal. The OE pin is referenced to the V_{CCA} supply.

Power Supply Guidelines

During normal operation, supply voltage V_{CCA} must be less than or equal to V_{CCB}. The sequencing of the power supplies will not damage the device during the power up operation. For optimal performance, 0.01 µF to 0.1 µF decoupling capacitors should be used on the V_{CCA} and V_{CCB} power supply pins. Ceramic capacitors are a good design choice to filter and bypass any noise signals on the voltage lines to the ground plane of the PCB. The noise immunity will be maximized by placing the capacitors as close as possible to the supply and ground pins, along with minimizing the PCB connection traces.

Part Marking

HK Package

L: LXS0102HKE
X: One Character Shorted Date Code

V Package

xR: LXS0102VE
1st Y: Die Rev
2nd Y: Date Code (Year)
W: Date Code (Workweek)
Bar above W means Cu wire

SS Package

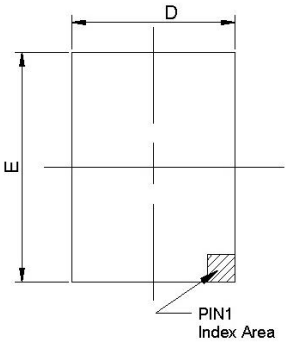
xR: LXS0102SSE
1st Y: Die Rev
2nd Y: Date Code (Year)
W: Date Code (Workweek)
1st X: Assembly Site Code
2nd X: Fab Site Code
Bar above 2nd "X" means Cu wire

GBA Package

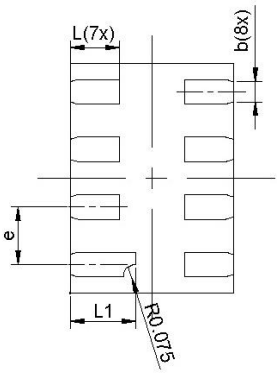
xR: LXS0102GBAE
Y: Date Code (Year)
W: Date Code (Workweek)

Packaging Mechanical

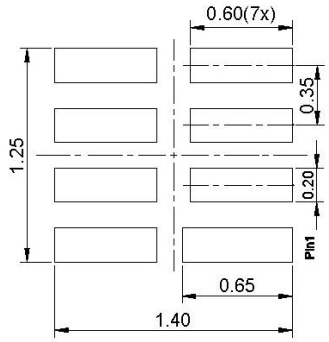
8-DFN (HK)



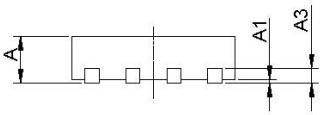
TOP VIEW



Bottom VIEW



RECOMMENDED LAND PATTERN(unit:mm)



SIDE VIEW

PKG. DIMENSIONS(MM)			
SYMBOL	Min	Nom	Max
A	0.36	0.40	0.43
A1	0	0.02	0.05
A3		0.13 REF	
D	0.95	1.00	1.05
E	1.35	1.40	1.45
b	0.12	0.15	0.20
e		0.35 BSC	
L	0.25	0.30	0.35
L1	0.35	0.40	0.45

Notes:
1. Ref: JEDEC MO-288
2. LAND PATTERN REFERENCE DIODES X2-DFN1410-8 PACKAGE INFORMATION

DATE: 12/10/20

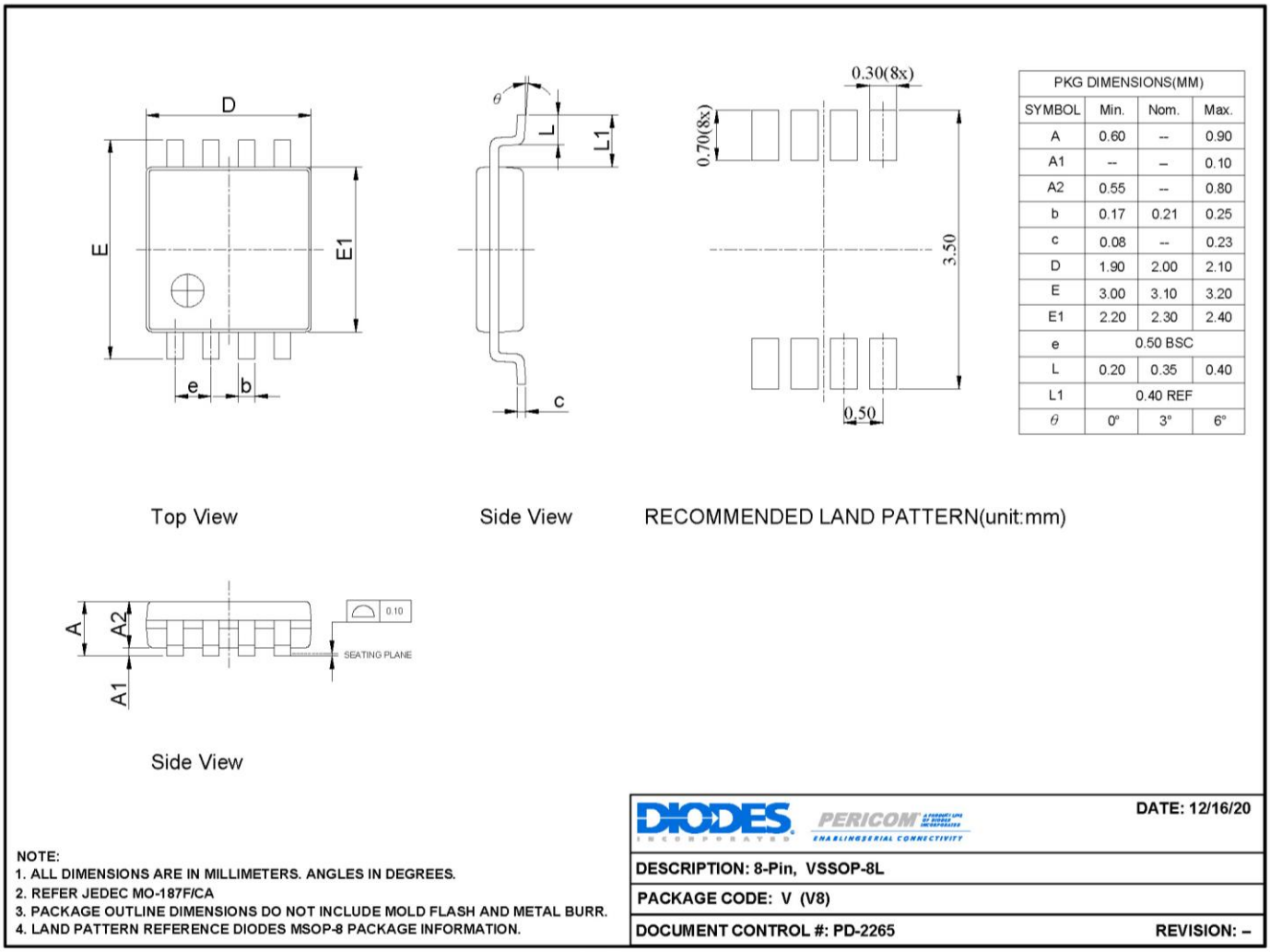
DESCRIPTION: 8-Pin, X1-DFN1410-8

PACKAGE CODE: HK (HK8)

DOCUMENT CONTROL#: PD-2264 REVISION:--

20-0540

8-VSSOP (V)



PKG DIMENSIONS(MM)			
SYMBOL	Min.	Nom.	Max.
A	0.60	--	0.90
A1	--	--	0.10
A2	0.55	--	0.80
b	0.17	0.21	0.25
c	0.08	--	0.23
D	1.90	2.00	2.10
E	3.00	3.10	3.20
E1	2.20	2.30	2.40
e	0.50 BSC		
L	0.20	0.35	0.40
L1	0.40 REF		
θ	0°	3°	6°

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES IN DEGREES.
2. REFER JEDEC MO-187F/CA
3. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR.
4. LAND PATTERN REFERENCE DIODES MSOP-8 PACKAGE INFORMATION.

DATE: 12/16/20

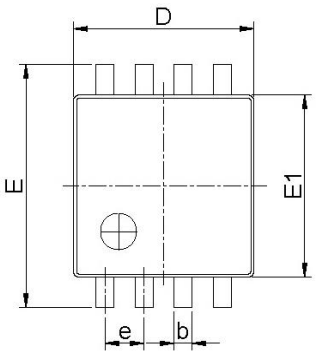
DESCRIPTION: 8-Pin, VSSOP-8L

PACKAGE CODE: V (V8)

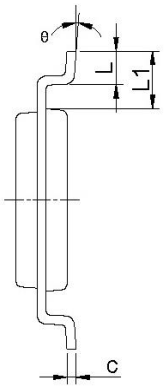
DOCUMENT CONTROL #: PD-2265 REVISION: –

20-0546

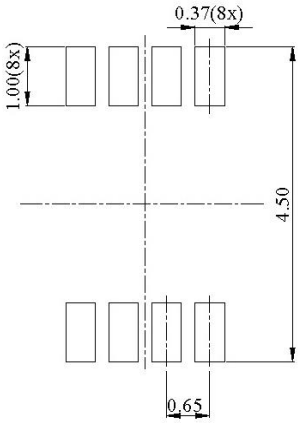
8-SSOP (SS)



Top View

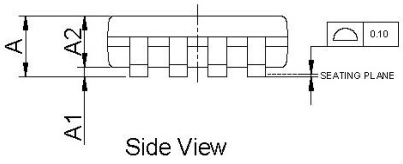


Side View



RECOMMENDED LAND PATTERN(unit:mm)

PKG DIMENSIONS(MM)			
SYMBOL	Min.	Nom.	Max.
A	--	--	1.30
A1	0.05	–	0.15
A2	0.95	1.05	1.20
b	0.15	0.23	0.30
C	0.08	--	0.23
D	2.75	2.95	3.15
E	3.75	4.00	4.25
E1	2.70	2.80	2.90
e	0.65 BSC		
L	0.20	0.40	0.60
L1	0.60 REF		
θ	0°	4°	8°



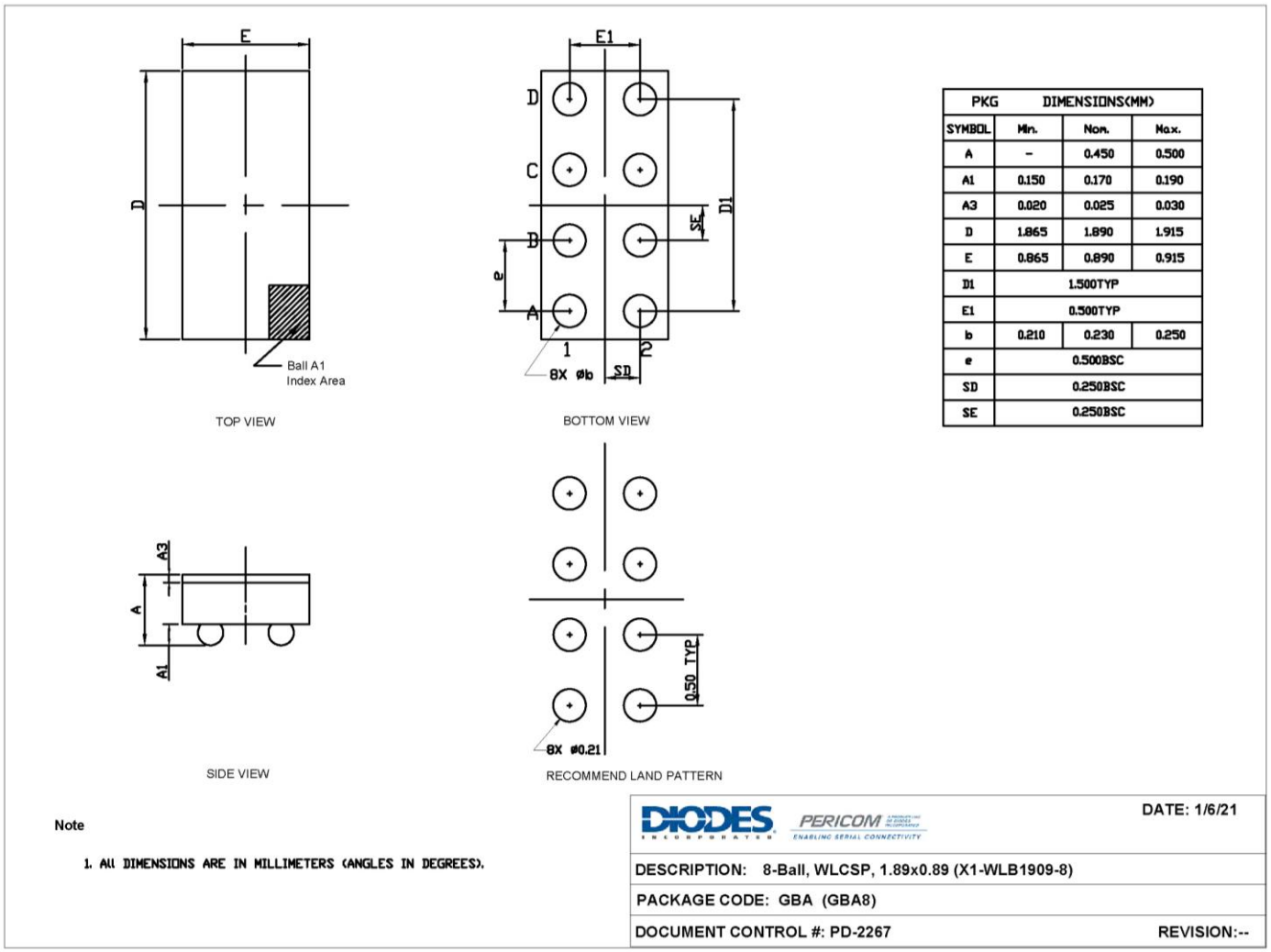
Side View

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES IN DEGREES.
2. REFER JEDEC MO-187F/DA
3. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR.
4. LAND PATTERN REFERENCE DIODES MSOP-8 PACKAGE INFORMATION.

DIODES INCORPORATED / PERICOM ENABLING SERIAL CONNECTIVITY	DATE: 03/02/21
DESCRIPTION: 8-Pin, SSOP-8L	
PACKAGE CODE: SS (SS8)	
DOCUMENT CONTROL #: PD-2266	REVISION: A

21-1374

8-WLCSP (GBA)



PKG	DIMENSIONS(MM)		
SYMBOL	Min.	Nom.	Max.
A	-	0.450	0.500
A1	0.150	0.170	0.190
A3	0.020	0.025	0.030
D	1.865	1.890	1.915
E	0.865	0.890	0.915
D1	1.500TYP		
E1	0.500TYP		
b	0.210	0.230	0.250
e	0.500BSC		
SD	0.250BSC		
SE	0.250BSC		

Note

1. All DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

DATE: 1/6/21

DESCRIPTION: 8-Ball, WLCSP, 1.89x0.89 (X1-WLB1909-8)

PACKAGE CODE: GBA (GBA8)

DOCUMENT CONTROL #: PD-2267 REVISION:--

21-0560

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Orderable Part Number	Package Code	Package Description
LXS0102HKEX	HK	8-pin, 1x1.4, X1-DFN1410-8 (DFN)
LXS0102VEX	V	8-pin (VSSOP)
LXS0102SSEX	SS	8-pin (SSOP)
LXS0102GBAEX	GBA	8-ball, 1.89x0.89 (WLCSP) (X1-WLB1909-8)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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