Wide Vin 50V Non-synchronous Boost/Flyback/SEPIC Controller

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- Wide Input Voltage Range: 3.1V-50V
- Low Shutdown Current 3.9uA
- Low Quiescent Operating Current: 540uA
- +/- 1.5% Feedback Reference Voltage
- Adjustable Switching Frequency: 100KHz to 2.2MHz
- Integrated Frequency Dither for EMI Mitigation
- External Frequency Synchronic
- External Compensation
- Pulse Skipping Mode
- Supports additional Slope Compensation
- Adjustable Soft-start Time
- Power Good Indicator
- Integrated Protection Feature
  - Constant Peak-Current Protection Threshold Over Input Voltage
  - Output Overvoltage Protection
  - Adjustable Under-voltage Lockout
  - Hiccup Over Load Protection
  - Thermal Shutdown Protection:165°C
- TQFN-12L(2mm*3mm)

APPLICATIONS

- Multi-output Flyback
- LED Bias Supply
- Portable Speaker Supply
- Battery Powered Boost/Flyback/SEPIC application

DESCRIPTION

The SCT81623Q device is a wide input, non-synchronous boost controller. The device can be used in Boost, SEPIC and Flyback converters.

The switching frequency of the SCT81623Q device can be adjusted to any value between 100kHz and 2.2MHz by using a single external resistor or by synchronizing it to an external clock. Current mode control provides superior bandwidth and transient response in addition to cycle-by-cycle current limiting. Current limit is adjustable through an external resistor.

The SCT81623Q is an Electromagnetic Interference (EMI) friendly controller with implementing optimized design for EMI reduction. The SCT81623Q features Frequency Spread Spectrum (FSS) with ±6% jittering span of the switching frequency and modulation rate 1/512 of switching frequency to reduce the conducted EMI.

The SCT81623Q device has built-in protection features such as thermal shutdown, short-circuit protection and overvoltage protection. Power-saving shutdown mode reduces the total supply current to 3.9 µA. Integrated current slope compensation simplifies the design and, if needed for specific applications, can be increased using a single resistor.

The device is available in a TQFN-12L(2mm*3mm) Package.

TYPICAL APPLICATION

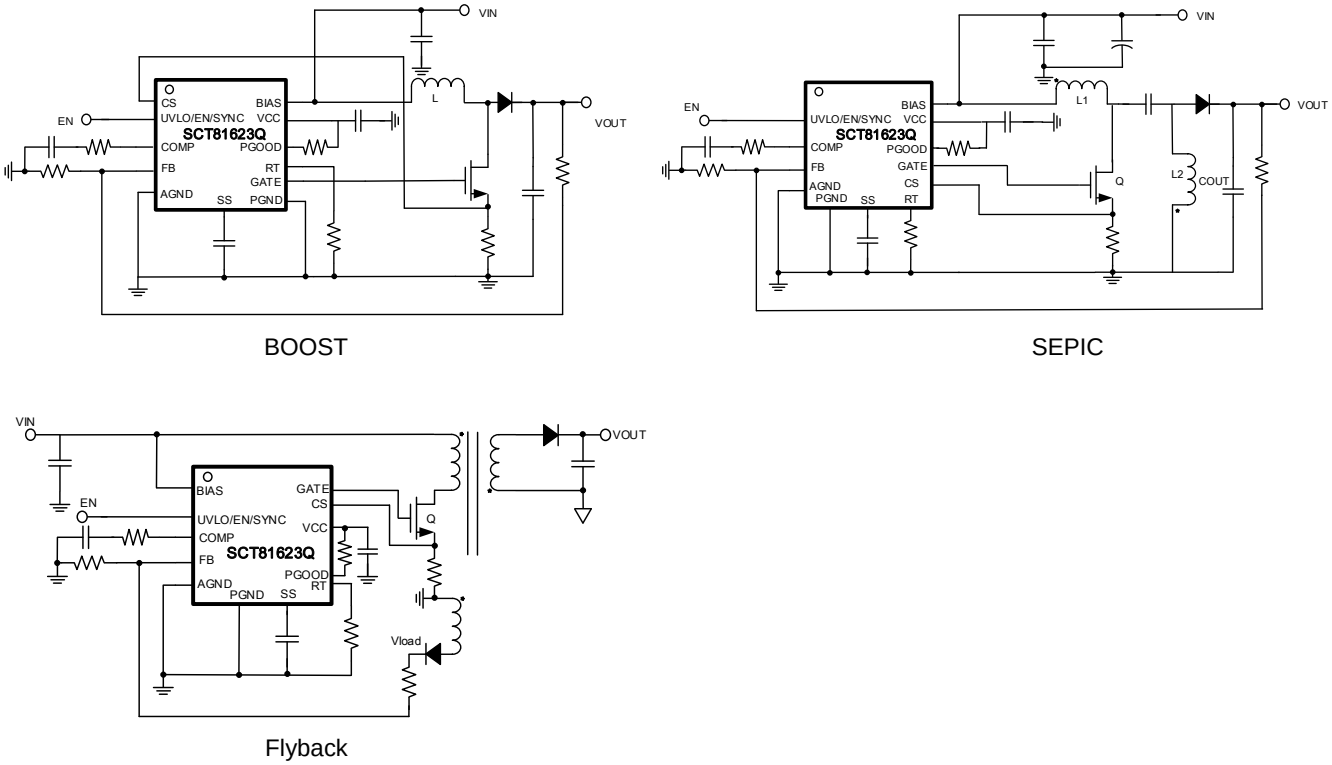


Figure 1. Typical Application Diagram

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version

Revision 0.8: Customer Sample

Revision 0.81: Update Package Information

Revision 0.82: Update Device Order Information

DEVICE ORDER INFORMATION

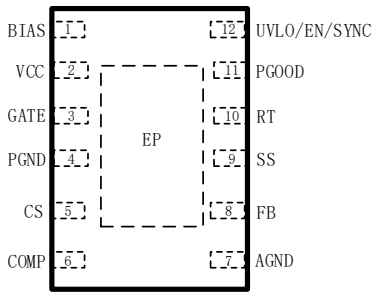
ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT81623QDPAR	Tape & Reel	5000	1623Q	12	TQFN-12L 2mm×3mm

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
BIAS, UVLO/EN/SYNC	-0.3	62	V
VCC, GATE	-1	6.6	V
CS, COMP, FB, RT	-5	5.5	V
Peak Driver Output Current		1(2)	A
Junction temperature(2)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

PIN CONFIGURATION



Top View: 12-Lead Plastic TQFN 2mmx3mm

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
(2) Guaranteed by design, not tested in productions.
(3) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 170°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	DESCRIPTION
BIAS	1	Power supply input pin. Connect a bypass capacitor from this pin to PGND.
VCC	2	Output of the internal VCC regulator and supply voltage input of the MOSFET driver. Connect a ceramic bypass capacitor from this pin to PGND.
GATE	3	N-channel MOSFET gate drive output. Connect directly to the gate of the N-channel MOSFET through a short, low inductance path.
PGND	4	Power ground pin. Connect directly to the ground connection of the sense resistor through a low inductance wide and short path.
CS	5	Current sense input pin. Connect to the positive side of the current sense resistor through a short path.
COMP	6	Output of the internal transconductance error amplifier. Connect the loop compensation components between this pin and ground.
AGND	7	Analog ground pin. Connect to the analog ground plane through a wide and short path.

FB	8	Inverting input of the error amplifier. Connect a voltage divider from the output to this pin to set output voltage. The device regulates FB voltage to the internal reference value of 1V typical.

PIN FUNCTIONS (continued)

NAME	NO.	DESCRIPTION
SS	9	Slow-start and Tracking. An external capacitor connected to this pin sets the output rise time. Since the voltage on this pin overrides the internal reference, it can be used for tracking and sequencing.
RT	10	Switching frequency setting pin. The switching frequency is programmed by a single resistor between RT and AGND.
PGOOD	11	Power Good indicator. This pin is an open-drain output. A high state indicates that the voltage at the FB pin is within a specified tolerance window centered.
UVLO/EN/ SYNC	12	Undervoltage lockout programming pin. The converter start-up and shutdown levels can be programmed by connecting this pin to the supply voltage through a resistor divider. The internal clock can be synchronized to an external clock signal into the UVLO/EN/SYNC pin. This pin must not be left floating. Connect to BIAS pin if not used.
EP	-	Exposed pad of the package. The exposed pad must be connected to AGND and the large ground copper plane to decrease thermal resistance.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{BIAS}	Input voltage range	3.1	50	V
V_{CC}	VCC voltage range	3.1	6.1	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per AEC-Q100-002	-2	+2	kV
	Charged Device Model(CDM), per AEC-Q100-011	-1	+1	kV

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	DFN-12L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	52.74	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.66	
Ψ_{JB}	Junction-to-board characterization parameter(1)	24.44	
$R_{\theta JC\ (top)}$	Junction to case (top) thermal resistance(1)	80.56	
$R_{\theta JC\ (bot)}$	Junction to case (bottom) thermal resistance(1)	6.9	
$R_{\theta JB}$	Junction to board thermal resistance(1)	25.44	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT81623Q is mounted, thermal pad size, and external environmental factors. The PCB board is a heat

sink that is soldered to the leads and thermal pad of the SCT81623Q. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

V_{BIAS}=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{BIAS}	Operating input voltage		3.1		50	V
V_{BIAS_UVLO}	BIAS Input UVLO Hysteresis	V_{BIAS} rising		2.82 160	3	V mV
I_{SD}	Shutdown current	V_{UVLO}=0		3.9	8	uA
I_Q	Quiescent current from VBIAS	no load, no switching, V_{FB}=1V		540		uA
I_{SUPPLY}(1)	Supply Current	R_{RT}=47.5kΩ, switching, no load and without external MOSFET		2		mA
VCC Power						
V_{CC}	Internal linear regulator	V_{BIAS}>7V		6.1		V
V_{CC_UVLO}				2.85		V
$V_{CC\_UVLO\_HYS}$				75		mV
IV_{CC}	VCC Sourcing current limit		20	70		mA
UVLO/EN/SYNC						
V_{UVLO_RISING}	UVLO/SYNC threshold	V_{UVLO} ramping up	1.425	1.5	1.575	V
$V_{UVLO\_FALLING}$	UVLO/SYNC threshold	V_{UVLO} ramping down	1.37	1.45	1.52	V
V_{UVLO_HYS}	UVLO/SYNC Hystersis			50		mV
I_{UVLO}	UVLO source current		3.15	4.95	6.5	uA
V_{EN_RISING}	EN rising threshold	V_{EN} ramping down	0.4	0.5	0.6	V
$V_{EN\_FALLING}$	EN falling threshold	V_{EN} ramping down	0.36	0.46	0.56	V
Reference and Control Loop						
V_{REF}	Reference voltage of FB		0.985	1	1.015	V
I_{FB}	FB pin leakage current	V_{FB}=1V			100	nA
G_{EA}	Error amplifier trans-conductance	V_{COMP}=1.5V	1.4	2	2.8	mA/V
I_{COMP_SRC}	Error amplifier maximum source current	V_{FB}=V_{REF}-200mV, V_{COMP}=1.5V	135	180	220	uA
I_{COMP_SNK}	Error amplifier maximum sink current	V_{FB}=V_{REF}+200mV, V_{COMP}=1.5V	135	180	220	uA
V_{COMP_H}	COMP high clamp	V_{FB}=0.8V	1.9	2.55	3.2	V
V_{COMP_L}	COMP low clamp	V_{FB}=1.7V	0.4	0.88	1.2	V
Gate Driver						
R_{DSON_TOP}	Driver switch on resistance(top)	I_{DR}=0.1A		2.5		Ω
R_{DSON_LOW}	Driver switch on resistance(bottom)	I_{DR}=0.1A		1.5		Ω

ELECTRICAL CHARACTERISTICS (continued)

V_{BIAS}=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Current Sense						
V_{CS_THR}	Current sense threshold		82	100	118	mV
V_{SL}(2)	Internal compensation Ramp voltage			90		mV
$C_{HICC-DEL}$	Hiccup mode activation delay	Clock cycles with current limiting before hiccup off-time activated (SS_done)		64		cycles
C_{HICCUP}	Hiccup mode off-time after activation	Clock cycles with no switching followed by SS release		32768		cycles
Soft start						
I_{SS}	Soft-start Current		7	10	14	μA
R_{SS}	SS pull-down switch R_{dson}			65		Ω
PGOOD						
R_{PG}	PG pulldown switch resistance	1mA sinking		120		Ω
V_{UVTH}	PG under-voltage threshold	FB rinsing(Reference to VREF)	92	95	98	%
		FB falling(Reference to VREF)	87	90	93	%
Switching Frequency						
F_{SW}	Switching frequency	R_{RT}=47.5kΩ	345	400	455	kHz
F_{SS}	Frequency Spread Range			6		%
D_{MAX}	Maximum Duty Cycle	R_{RT}=47.5kΩ	85	91		%
t_{ON_MIN}	Minimum on-time	Fsw=400kHz		250		ns
Protection						
V_{OVTH}	FB overvoltage threshold	FB rising	107	110	113	%
		FB falling		105		%
T_{SD}(1)	Thermal shutdown threshold	T_J rising		165		°C
	Hysteresis			25		°C

(1) Guaranteed by design and bench, not tested in production.
(2) Guaranteed by design, not tested in production.

TYPICAL CHARACTERISTICS

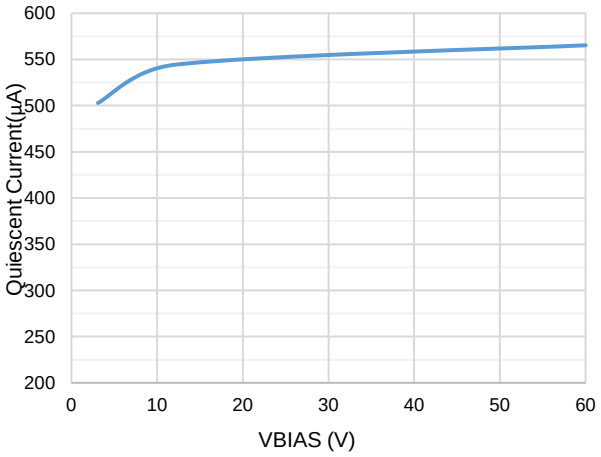


Figure 2. I_{SD} vs. Input Voltage

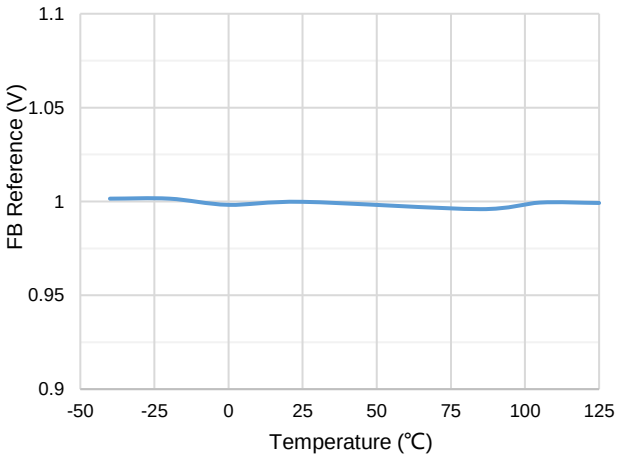


Figure 3. FB Reference vs. Temperature

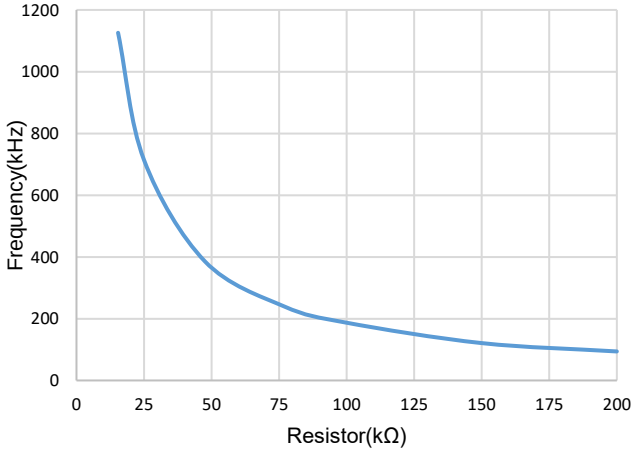


Figure 4. Switching Frequency vs. RT

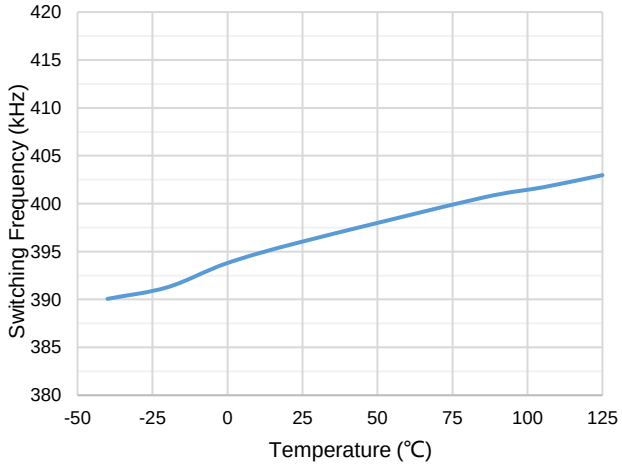


Figure 5. Switching Frequency vs. Temperature

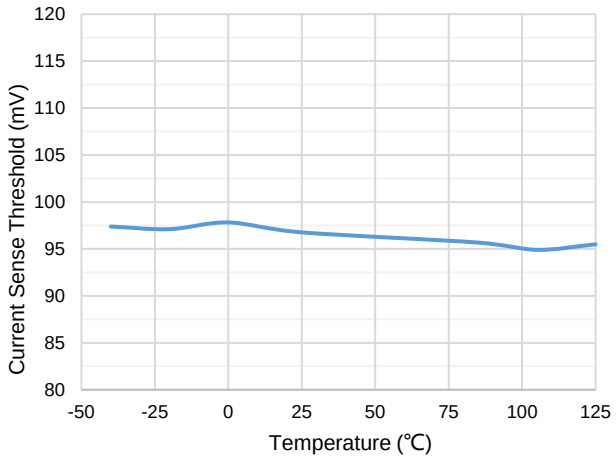


Figure 6. Current Limit Threshold vs. Temperature

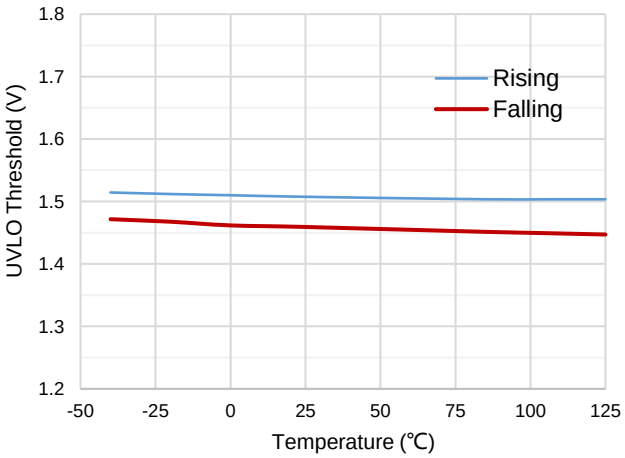


Figure 7. UVLO Threshold vs. Temperature

TYPICAL CHARACTERISTICS

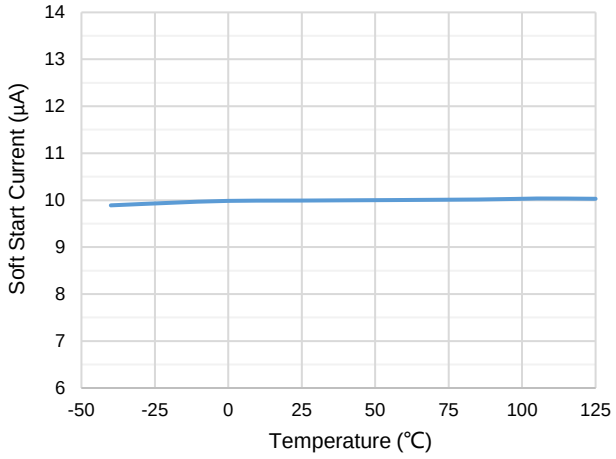


Figure 8. I_{SS} vs Temperature

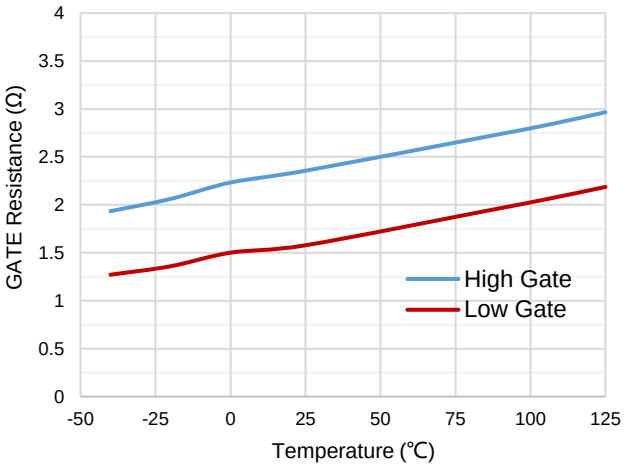


Figure 9. GATE Resistance vs. Temperature

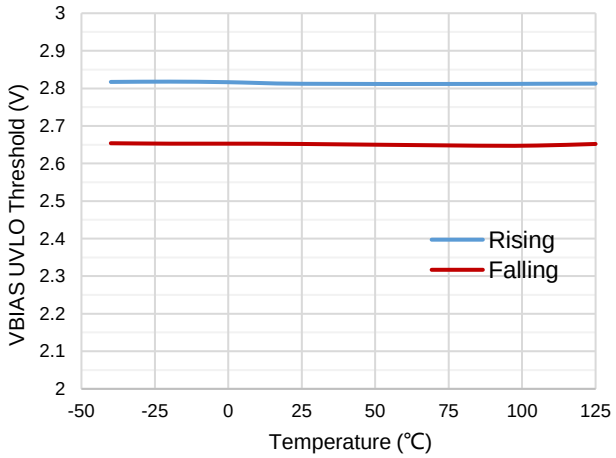


Figure 10. UVLO Threshold vs Temperature

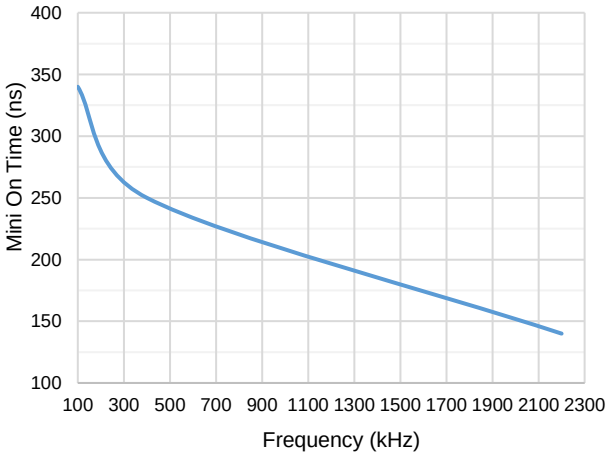


Figure 11. tON(MIN) vs Frequency

FUNCTIONAL BLOCK DIAGRAM

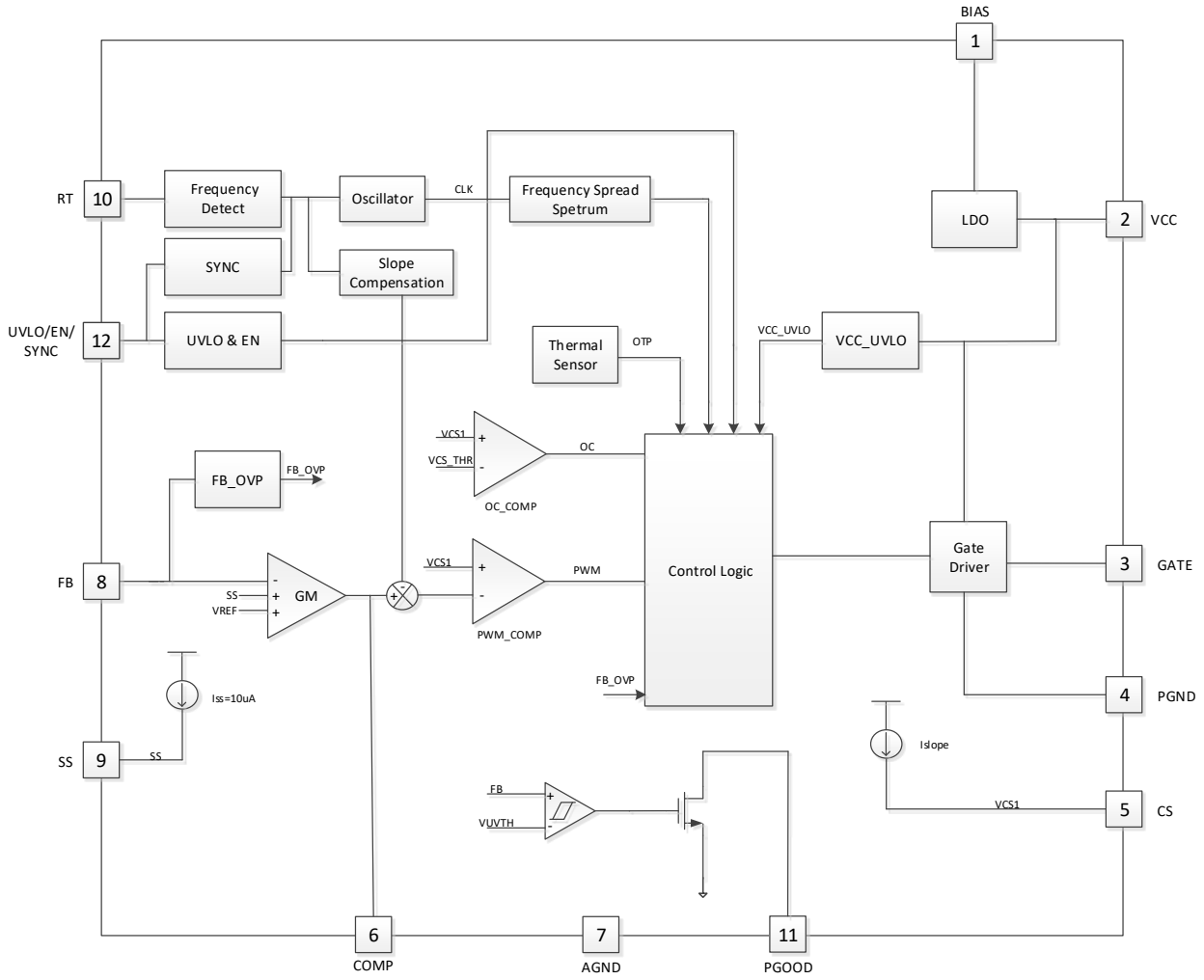


Figure 12. Functional Block Diagram

OPERATION

Overview

The SCT81623Q device is a wide input range, non-synchronous boost controller that uses peak-current-mode control. The device can be used in boost, SEPIC, and flyback topologies.

In a typical application circuit, the peak current through the external MOSFET is sensed through an external sense resistor. The voltage across this resistor is fed into the CS pin. This voltage is fed into the positive input of the PWM comparator. The output voltage is also sensed through an external feedback resistor divider network and fed into the error amplifier negative input. The output of the error amplifier (COMP pin) is added to the slope compensation ramp and fed into the negative input of the PWM comparator. At the start of any switching cycle, the oscillator sets the RS latch using the switch logic block. This forces a high signal on the GATE pin (driver of the external MOSFET) and the external MOSFET turns on. When the voltage on the positive input of the PWM comparator exceeds the negative input, the RS latch is reset and the external MOSFET turns off. The voltage sensed across the sense resistor generally contains spurious noise spikes. These spikes can force the PWM comparator to reset the RS latch prematurely. To prevent these spikes from resetting the latch, a blank-out circuit inside the IC prevents the PWM comparator from resetting the latch for a short duration after the latch is set. This duration is called the blanking interval and is specified as minimum on-time in the Electrical Characteristics section. Under extremely light-load or no-load conditions, the energy delivered to the output capacitor when the external MOSFET in on during the blanking interval is more than what is delivered to the load. An over-voltage comparator inside the SCT81623Q prevents the output voltage from rising under these conditions. The over-voltage comparator senses the feedback (FB pin) voltage and resets the RS latch. The latch remains in reset state until the output decays to the nominal value.

The SCT81623Q works at pulse skip mode (PSM) to further increase the efficiency in light load condition.

The quiescent current of SCT81623Q is 540uA typical under no-load condition and no switching. Disabling the device, the typical supply shutdown current on BIAS pin is 3.9μA.

Overvoltage Protection

The SCT81623Q has over voltage protection (OVP) for the output voltage. OVP is sensed at the feedback pin (FB). If at any time the voltage at the feedback pin rises to 1.1V (typ.), OVP is triggered. OVP will cause the GATE pin to go low, forcing the power MOSFET off. With the MOSFET off, the output voltage will drop. The SCT81623Q begins switching again when the feedback voltage reaches 1V (typ.).

Slope Compensation Ramp

The SCT81623Q uses a current mode control scheme. The main advantages of current mode control are inherent cycle-by-cycle current limit for the switch and simpler control loop characteristics. However, current mode control has a Sub-harmonic Oscillation when duty cycle is greater than 50%. To prevent the Sub-harmonic oscillations, a compensation ramp is added to the control signal.

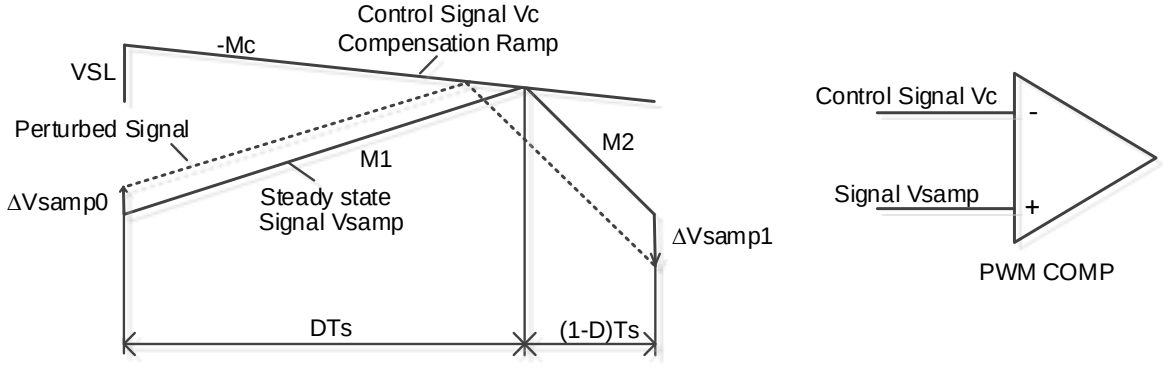


Figure13. Sub-Harmonic Oscillation for D>0.5 and Compensation Ramp to Avoid Sub-Harmonic Oscillation

The current mode control scheme samples the inductor current, IL, and compares the sampled signal, V_{samp}, to a internally generated control signal, Vc. The current sense resistor, R_{SEN}, as shown in Figure13 converts the sampled inductor current, IL, to the voltage signal, V_{samp}, that is proportional to IL such that：

$$V_{samp} = I_L * R_{SEN} \quad (1)$$

Figure13 illustrate the theory why Sub-Harmonic Oscillation happen. The rising and falling slopes, M1 and -M2 respectively, of V_{samp} are also proportional to the inductor current rising and falling slopes, Mon and -Moff respectively. Where Mon is the inductor slope during the switch on-time and -Moff is the inductor slope during the switch off-time and are related to M1 and -M2 by：

$$M_1 = M_{on} * R_{SEN} \quad (2)$$

$$-M_2 = -M_{off} * R_{SEN} \quad (3)$$

For the boost topology:

$$M_1 = M_{on} * R_{SEN} = Vin * R_{SEN} / L \quad (4)$$

$$M_2 = M_{off} * R_{SEN} = (Vout - Vin) * R_{SEN} / L \quad (5)$$

In Figure13, a small increase in the load current causes the sampled signal to increase by ΔV_{samp0}. The effect of this load change, ΔVsamp1, at the end of the first switching cycle is

$$\Delta V_{samp1} = -(\frac{M_2 - M_c}{M_1 + M_c}) * \Delta V_{samp0} \quad (6)$$

So, When No compensation ramp signal is added, which Mc is zero, then:

$$\Delta V_{samp1} = -(\frac{M_2}{M_1}) * \Delta V_{samp0} = -(\frac{D}{1-D}) * \Delta V_{samp0} \quad (7)$$

When D > 0.5, ΔV_{samp1} will be greater than ΔV_{samp0}. In other words, the disturbance is divergent. So a very small perturbation in the load will cause the disturbance to increase.

After a compensation ramp is added to the control signal. To ensure that the perturbed signal converges we must maintain:

$$\left| -(\frac{M_2 - M_c}{M_1 + M_c}) \right| < 1 \quad (8)$$

The compensation ramp has been added internally in the SCT81623Q. The slope of this compensation ramp has been selected to satisfy most applications, and its value depends on the switching frequency. This slope can be calculated using the formula:

$$M_c = V_{SL} * F_s \quad (9)$$

V_{SL} is the amplitude of the internal compensation ramp and F_S is the controller's switching frequency.

For more flexibility, slope compensation can be increased by adding one external resistor, R_{SL}, in the CS's path. Figure14 shows the setup. The externally generated slope compensation is then added to the internal slope compensation of the SCT81623Q. When using external slope compensation, the formula for Mc becomes:

$$M_c = (V_{SL} + K * R_{SL}) * F_s \quad (10)$$

A typical value for factor K is 40 μA.

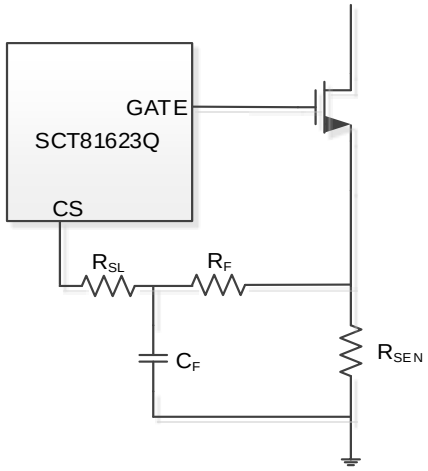


Figure14. External R_{SL} to increase slope compensation

Adjustable Peak Current Limit

The device provides cycle-by-cycle peak current limit protection that turns off the MOSFET when the sum of the inductor current and the programmable slope compensation ramp reaches the current limit threshold. Peak inductor current limit ($I_{PEAK-CL}$) in steady state is calculated as shown in:

$$I_{PEAK\_CL} = \frac{V_{SENSE} - 40uA \times R_{SL} \times D}{R_{SEN}} \quad (11)$$

Where

- V_{CS_THR} is CS pin limiting voltage (Typ. =100mV)
- $I_{PEAK-CL}$ is the inductor peak current limit
- R_{SL} is Slope compensation resistor
- D is Duty cycle
- R_{SEN} is the Inductance peak current detection resistance

If required, a small external RC filter (R_F, C_F) at the CS pin can be added to overcome the large leading edge spike of the current sense signal. Select an R_F value in the range of 10 Ω to 200 Ω and a C_F value in the range of 100 pF to 2 nF. Because of the effect of this RC filter, the peak current limit is not valid when the on-time is less than 2 × R_F × C_F. To fully discharge the C_F during the off-time, the RC time constant should satisfy the following inequality.

$$3 \times R_F \times C_F < \frac{1-D}{F_S} \quad (12)$$

When overload happens, the converter cannot provide output current to satisfy loading requirement. The inductor current is clamped at over current limitation. Thus, the output voltage drops below regulated voltage with FB voltage less than internal reference voltage continuously. The internal COMP voltage ramps up to high. When COMP voltage is clamped for 64 cycles, the controller stops working. After remaining OFF for 32768 cycles, the device restarts from soft starting phase. If overload or hard short condition still exists during soft-start and make COMP voltage clamped at high , after soft start time and COMP still keep high for 64 cycles , the device enters into turning-off mode again. When overload or hard short condition is removed, the device automatically recovers to enters normal regulating operation.

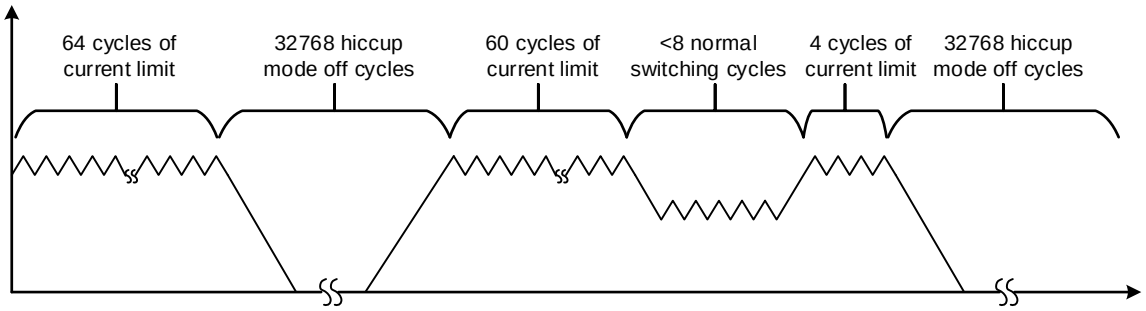


Figure15. Hiccup Mode Protection

Because D can be variable under different V_{BIAS}, $I_{PEAK-CL}$ is not stable under different V_{BIAS} when using external slope compensation resistor. So for an accurate peak current limit operation over the input supply voltage, SCT recommends using only the fixed slope compensation.

Output Voltage

The output voltage is set by an external resistor divider R_{FBT} and R_{FBB} in typical application schematic. The value of RFBT can be calculated by equation 13.

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \quad (13)$$

where:

- V_{REF} is the feedback reference voltage, typical 1V

Switching Frequency

The switching frequency of the SCT81623Q can be adjusted between 100 kHz and 2.2 MHz using a single external resistor. This resistor must be connected between the RT pin and ground. Equation 14 can be used to estimate the frequency adjust resistor.

$$R_{FA}(\mathrm{K\Omega}) = \frac{19700}{fsw(\mathrm{kHz})} - 1.177 \quad (14)$$

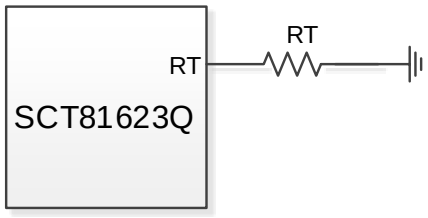


Figure16. Frequency Adjust

Enable and Under Voltage Lockout

The external UVLO resistor divider must be designed so that the voltage at the UVLO pin is greater than 1.5V typical) when the input voltage is in the desired operating range. The values of R1 and R2 can be calculated as shown in Equation 15 and Equation 16.

$$R1 = \frac{V_{IN\_ON} - V_{IN\_OFF}}{I_{UVLO}} \quad (15)$$

where

- V_{IN_ON} is the desired start-up voltage of the converter
- V_{IN_OFF} is the desired turnoff voltage of the converter.

$$R2 = R1 * \frac{V_{UVLOEN}}{V_{IN\_ON} - V_{UVLOEN}} \quad (16)$$

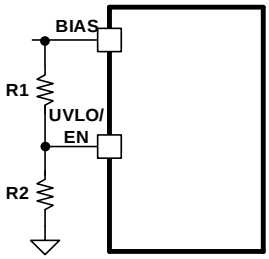


Figure17. System UVLO Resistor Divider

When the UVLO pin voltage is above the UVLO threshold, the device enters run mode. In run mode, a soft-start sequence starts after 8 clocks once the VCC voltage exceeds the 2.85V VCC UV threshold. UVLO hysteresis is accomplished with an internal 50mV voltage hysteresis and an additional 5μA current source that is switched on or off. When the UVLO pin voltage exceeds the UVLO threshold, the current source is enabled to quickly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the UVLO threshold, the current source is disabled, causing the voltage at the UVLO pin to fall quickly. When the UVLO pin voltage is less than the enable threshold, the device enters shutdown mode after a 30μs (typical) delay with all functions disabled.

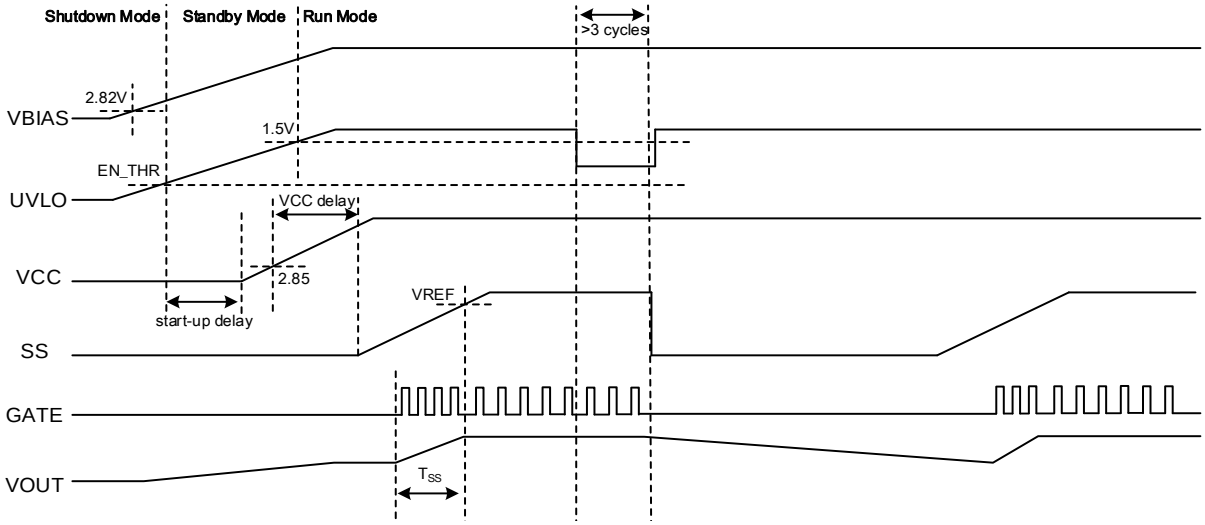


Figure 18. Boost Start-Up Waveforms Case 1: Start-Up diagram, UVLO Toggle After Start-Up

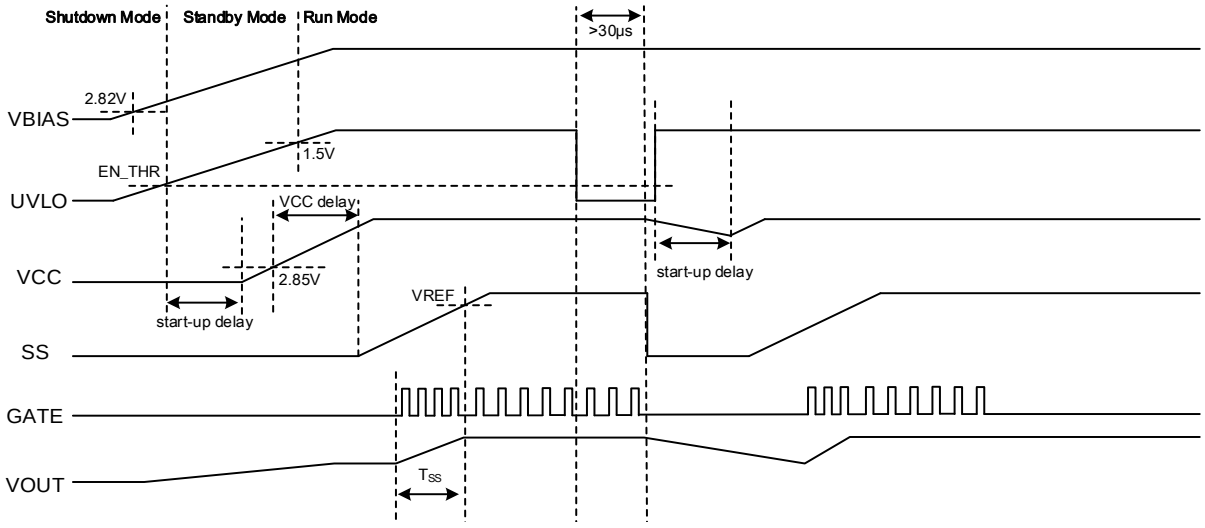


Figure 19. Boost Start-Up Waveforms Case 2: Start-Up diagram, EN Toggle After Start-Up

Clock Synchronization

The switching frequency of the device can be synchronized to an external clock by pulling down the UVLO/ SYNC pin. The external synchronization clock must pull down the UVLO/SYNC pin voltage below 1.45 V (typical). The duty cycle of the pulldown pulse is not limited, but the minimum pulldown pulse width must be greater than 150 ns, and the minimum pullup pulse width must be greater than 250 ns.

The external clock frequency f_{SYNC} must be within +25% and –30% of f_{RT}(TYPICAL). Because the maximum duty cycle limit and the peak current limit with slope resistor (R_{SL}) are affected by the clock synchronization, take extra care when using the clock synchronization function.

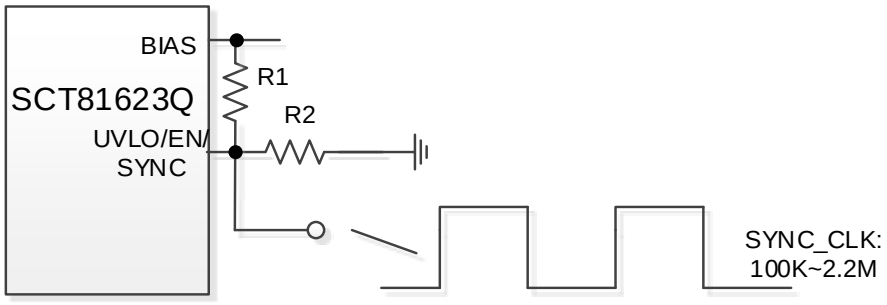


Figure 20. Frequency Sync

Programmable Soft-Start

The SS pin voltage controls start-up of output voltage. After the voltage is rising threshold of under voltage lockout reference voltage, the SCT81623Q begins regulating the output to the level dictated by the feedback resistor network and SS voltage. A 10μA current source charges the soft-start capacitor connecting SS pin. Soft start avoids inrush current as a result of high output capacitance to avoid an overcurrent condition. The inrush stress on the input supply rail is also reduced. The soft-start time, t_{SS}, for the output voltage to ramp to its nominal level is set by:

$$t_{SS} = \frac{C_{SS}}{I_{SS}} \quad (17)$$

where

- C_{SS} is the soft-start capacitance
- I_{SS} is the current sourced from the SS pin

The device adopts the lower voltage between the internal voltage reference 1V and the SS pin voltage as the reference input voltage of the error amplifier and regulates the output. The soft-start completes when the voltage at the SS pin exceeds the internal reference voltage of 1V. The SS pin is pulled down to ground by an internal switch when the VCC is less than VCC UVLO threshold, the UVLO is less than the UVLO threshold, during hiccup mode off-time or thermal shutdown.

MOSFET Driver

The device provides an N-channel MOSFET driver that can source or sink a peak current of 1A. During start-up, especially when the input voltage range is below the VCC regulation target, the VCC voltage must be sufficient to completely enhance the MOSFET. If the MOSFET drive voltage is lower than the MOSFET gate plateau voltage during start-up, the boost converter may not start up properly and it can stick at the maximum duty cycle in a high power dissipation state. This condition can be avoided by selecting a lower threshold N-channel MOSFET switch and setting the V_{IN_ON} greater than 6 to 7 V. Since the internal VCC regulator has a limited sourcing capability, the MOSFET gate charge should satisfy the following inequality.

$$Q_{G@VCCSS} \times F_S < 20\text{mA} \quad (18)$$

An internal 400kΩ resistor is connected between GATE and PGND to prevent a false turnon during shutdown. In boost topology, a switch node dV/dT must be limited during the 75μs internal start-up delay to avoid a false turnon, which is caused by the coupling through CDG parasitic capacitance of the MOSFET.

Frequency Spread Spectrum

To reduce EMI, the device implements Frequency Spread Spectrum (FSS). The FSS circuitry shifts the switching frequency of the regulator periodically within a certain frequency range around the adjusted switching frequency. The jittering span is ±6% of the switching frequency with 1/512 swing frequency. This frequency dithering function is effective for both frequency adjusted by resistor placed at RT pin and an external clock synchronization application.

Power Good

The PGOOD pin is an open-drain output. A pull up resistor between the values of 10KΩ and 100KΩ to a voltage source recommended.

The PGOOD pin is pulled low when the FB is lower than 90% or greater than 110% of the nominal internal reference voltage. Also, the PGOOD is pulled low if VBIAS UVLO or thermal shutdown are asserted or the UVLO/EN pin pulled low.

Thermal Shutdown

An internal thermal shutdown turns off the VCC regulator, disables switching, and pulls down the SS when the junction temperature exceeds the thermal shutdown threshold (T_{SD}). After the temperature is decreased by 25°C, the VCC regulator is enabled again and the device performs a soft start.

Shutdown Mode

If the UVLO pin voltage is below the enable threshold for longer than 30 μs (typical), the device goes to the shutdown mode with all functions disabled. In shutdown mode, the device decreases the BIAS pin current consumption to below 3.9 μA (typical).

Standby Mode

If the UVLO pin voltage is greater than the enable threshold and below the UVLO threshold for longer than 2 μs, the device is in standby mode with the VCC regulator operational, RT regulator operational, SS pin grounded, and no switching at the GATE output. The PGOOD is activated when the VCC voltage is greater than the VCC UV threshold.

Run Mode

If the UVLO pin voltage is above the UVLO threshold and the VCC voltage is sufficient, the device enters RUN mode. In this mode, soft start starts 8 internal clocks after the VCC voltage exceeds the 2.85 VCC UV threshold.

APPLICATION INFORMATION

Typical Application (Boost)

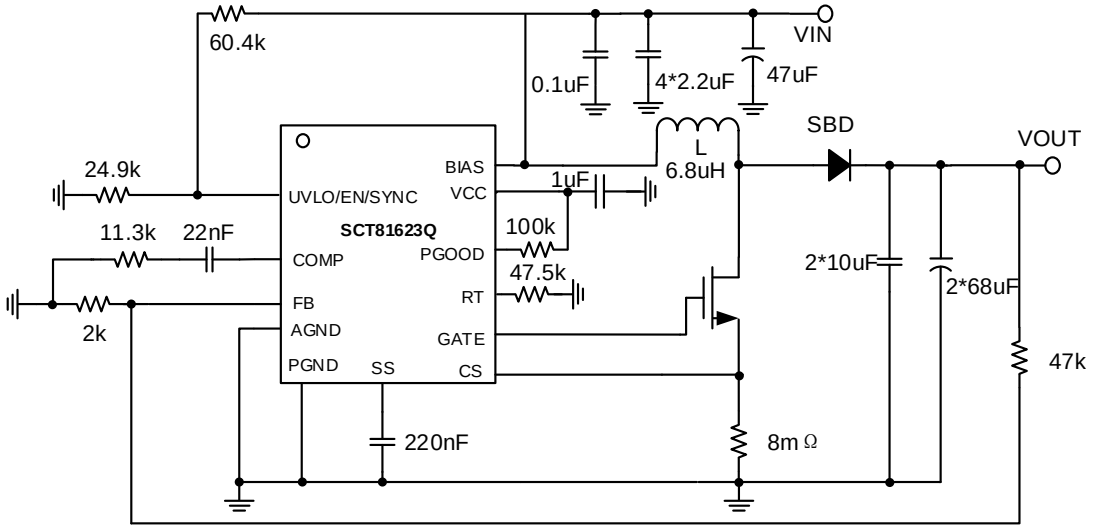


Figure 21. Application Schematic, 6V to 18V, 2A Boost Regulator at 400kHz

Design Parameters

Design Parameters	Example Value
Input Voltage	6V to 18V
Output Voltage	24V
Maximum Output Current	2A
Switching Frequency	400 KHz
Output voltage ripple (peak to peak)	85mV (Load=2A)

Inductor Selection (Boost)

The performance of inductor affects the power supply's steady state operation, transient behavior, loop stability, and boost converter efficiency. The inductor value, DC resistance, and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DC resistance, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have ±20% or even ±50% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, maxim load current and minimum switching frequency of the application, while considering the inductance with -30% tolerance and low-power conversion efficiency.

For a boot converter, calculate the inductor DC current as:

$$I_{LDC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (19)$$

Where

- V_{OUT} is the output voltage of the boost converter
- I_{OUT} is the output current of the boost converter
- V_{IN} is the input voltage of the boost converter
- η is the power conversion efficiency

Calculate the inductor current peak-to-peak ripple, I_{LPP}, as:

$$I_{LPP} = \frac{1}{L \times \left(\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}} \right) \times f_{SW}} \quad (20)$$

Where

- I_{LPP} is the inductor peak-to-peak current
- L is the inductance of inductor
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Therefore, the peak switching current of inductor, I_{LPEAK}, is calculated as:

$$I_{LPEAK} = I_{LDC} + \frac{I_{LPP}}{2} \quad (21)$$

Set the current limit of the SCT81623Q higher than the peak current I_{LPEAK} and select the inductor with the saturation current higher than the current limit.

Input Capacitor Selection

Due to the presence of an inductor at the input of a boost converter, the input current waveform is continuous. The inductor ensures that the input capacitor sees fairly low ripple currents. However, as the input capacitor gets smaller, the input ripple goes up. The RMS current in the input capacitor is given using following equation.

$$I_{CIN(RMS)} = \frac{(V_{OUT} - V_{IN}) \times V_{IN}}{\sqrt{12} \times V_{OUT} \times L \times fsw} \quad (22)$$

The input capacitor should be capable of handling the RMS current. Although the input capacitor is not as critical in a boost application, low values can cause impedance interactions. Therefore, a good quality capacitor should be chosen in the range of 10 µF to 40 µF. If a value lower than 10 µF is used, then problems with impedance interactions or switching noise can affect the SCT81623Q. To improve performance, especially with VBIAS below 8 volts, it is recommended to use a 2.2 Ohm resistor at the input to provide an RC filter. The resistor is placed in series with the BIAS pin with only a bypass capacitor attached to the BIAS pin directly. A 0.1-µF or 1-µF ceramic capacitor is necessary in this configuration. The bulk input capacitor and inductor will connect on the other side of the resistor at the input power supply.

Output Capacitor Selection

For small output voltage ripple, choose a low-ESR output capacitor like a ceramic capacitor. Typically, 3～4x 22µF ceramic output capacitors work for most applications. A 0.1µF ceramic bypass capacitor is recommended to be placed as close as possible to the switch node. Higher capacitor values can be used to improve the load transient response. Due to a capacitor's derating under DC bias, the bias can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. From the required output voltage ripple, use the equation 23 and 24 to calculate the minimum required effective capacitance, C_{OUT}.

$$V_{ripple\_C} = \frac{(V_{OUT} - V_{IN\_MIN}) \times I_{OUT}}{V_{OUT} \times C_{OUT} \times fsw} \quad (23)$$

$$V_{ripple\_ESR} = I_{LPEAK} \times ESR \quad (24)$$

where

- V_{ripple_C} is output voltage ripple caused by charging and discharging of the output capacitor.
- V_{ripple_ESR} is output voltage ripple caused by ESR of the output capacitor.
- V_{IN_MIN} is the minimum input voltage of boost converter.
- V_{OUT} is the output voltage.
- I_{OUT} is the output current.
- I_{Lpeak} is the peak current of the inductor.
- f_{SW} is the converter switching frequency.
- ESR is the ESR resistance of the output capacitors.

Power MOSFET Selection

The following parameters should be taken into consideration for MOSFET: the on-resistance R_{DS_ON}, the minimum gate threshold voltage V_{TH_MIN}, the total gate charge Q_g, the reverse transfer capacitance C_{RSS}, and the maximum drain to source voltage V_{Q_MAX}. The peak switching voltage between drain to source in a Boost is given by

$$V_{SW\_PEAK} = V_{IN} + V_D \quad (25)$$

Then the V_{Q_MAX} of power MOSFET should be greater than the peak switching voltage.

The peak switching current flowing through the MOSFET is given by:

$$I_{Q\_PEAK} = I_{LPEAK} \quad (26)$$

The RMS current through the MOSFET is calculated by:

$$I_{Q\_RMS} = \sqrt{(I_{LDC}^2 + \frac{I_{LPP}}{12}) * D} \quad (27)$$

Then power dissipation in MOSFET can be estimated by:

$$P_{DIS} = I_{Q\_RMS}^2 \times R_{DS\_ON} \times D_{MAX} + \left(V_O + V_{IN\_MIN}\right) \times I_{Q\_PEAK} \times \frac{Q_g \times f_{SW}}{I_G} \quad (28)$$

Where

- I_G is the gate drive current.

The total power dissipation of MOSFET includes conduction loss as shown in the first term and switching loss as shown in the second term. The total power dissipation should be within package thermal ratings.

Output Diode Selection

Observation of the boost converter circuit shows that the average current through the diode is the average load current, and the peak current through the diode is the peak current through the inductor. The diode should be rated to handle more than its peak current. The peak diode current can be calculated using following equation.

$$I_{D(PEAK)} = \frac{I_{OUT}}{(1-D)} + \Delta I_L \quad (29)$$

Thermally the diode must be able to handle the maximum average current delivered to the output. The peak reverse voltage for boost converters is equal to the regulated output voltage. The diode must be capable of handling this voltage. To improve efficiency, a low forward drop schottky diode is recommended.

Application Waveforms

VBIAS=12V, Vout=24V, unless otherwise noted

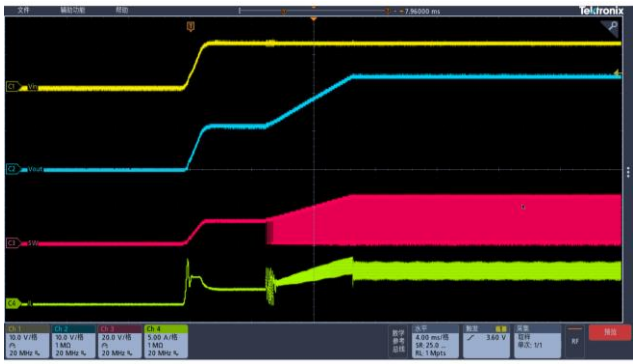


Figure 22. Power up(Iload=2A)

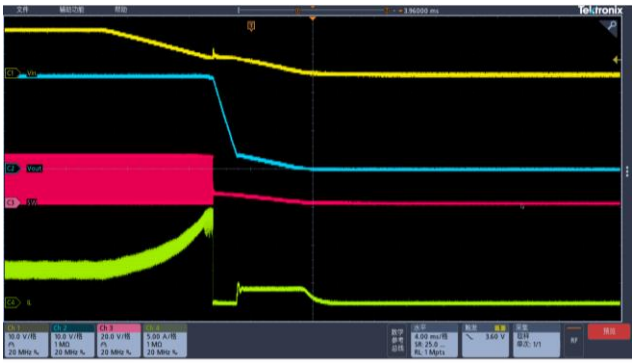


Figure 23. Power down(Iload=2A)

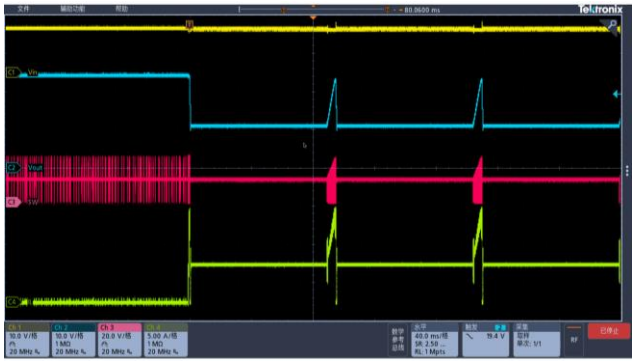


Figure 24. Over current protection (Iload=5A)

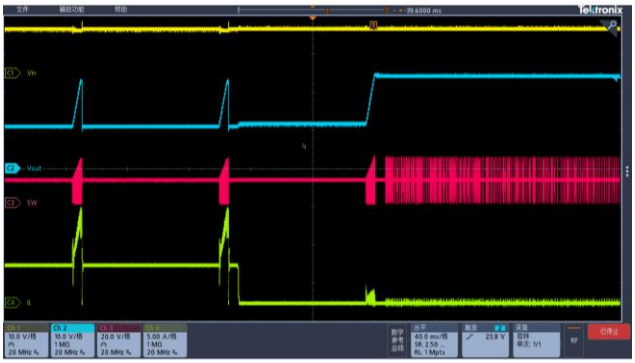


Figure 25. Over current recovery (Iload=5A)

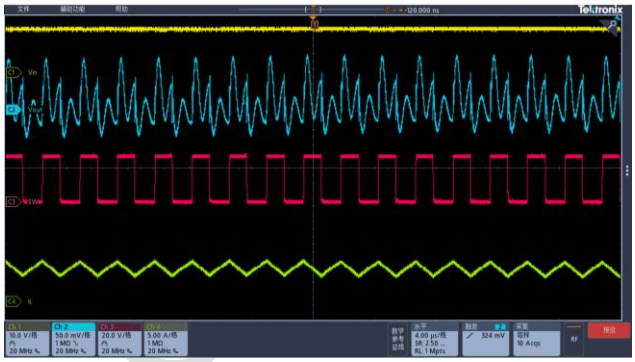


Figure 26. Steady-state (Iload=2A)

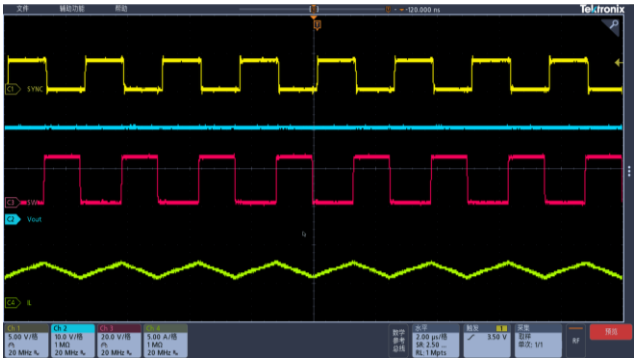


Figure 27. Sync Frequency

APPLICATION INFORMATION

Typical Application(Sepic)

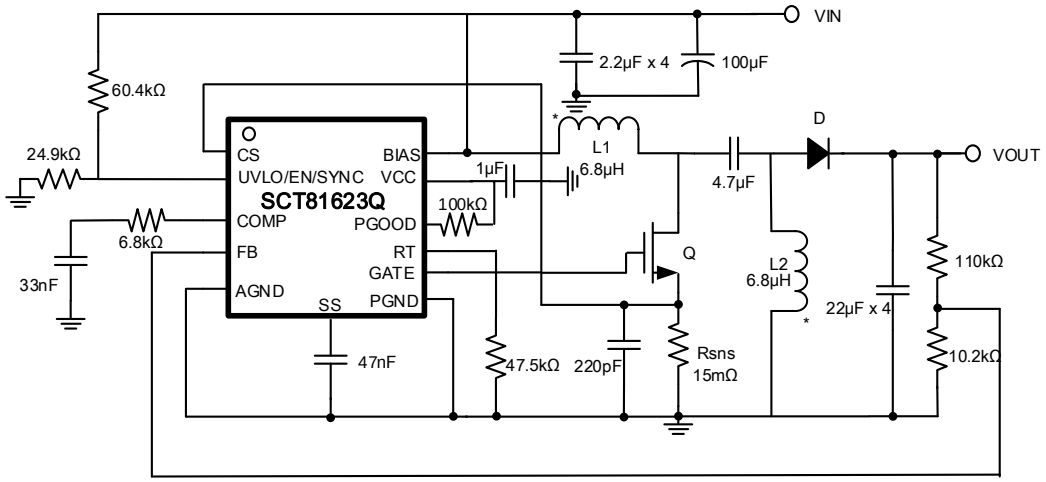


Figure 28. Application Schematic, 5V to 50V, 2A Sepic Regulator at 200kHz

Design Parameters

Design Parameters	Example Value
Input Voltage	24V Normal 5V to 50V
Output Voltage	12V
Maximum Output Current	2A
Switching Frequency	400 KHz
Output voltage ripple (peak to peak)	75mV (Load=2A)

Inductor Selection (Sepic)

A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20% to 40% of the maximum input current at the minimum input voltage. The current ripple flowing in inductors L1 and L2 is given by:

$$\Delta I_{L1} = I_{IN} \times 40\% = I_O \times \frac{V_O}{V_{IN\_MIN}} \times 40\% \quad (30)$$

$$\Delta I_{L2} = I_O \times 40\% = I_O \times 40\% \quad (31)$$

Normally we can select equal value for the inductors L1 and L2, derived as:

$$L_1 = L_2 = L = \frac{V_{IN\_MIN}}{\Delta I_L \times f_{SW}} \times D_{MAX} \quad (32)$$

Where

- f_{SW} is the switching frequency.

Note that the saturation current of inductors should be greater than peak current flowing in inductors, given by:

$$I_{L1\_PEAK} = I_{IN} + \frac{\Delta I_L}{2} = I_O \times \frac{V_O}{V_{IN\_MIN}} \times (1 + \frac{40\%}{2}) \quad (33)$$

$$I_{L2\_PEAK} = I_O + \frac{\Delta I_L}{2} = I_O \times (1 + \frac{40\%}{2}) \quad (34)$$

If L1 and L2 are wound in same core as a coupled inductor, the inductance required will be half due to the mutual induction, calculated by:

$$L_1 = L_2 = \frac{L}{2} = \frac{V_{IN\_MIN}}{2 \times \Delta I_L \times f_{SW}} \times D_{MAX} \quad (35)$$

Power MOSFET Selection

The following parameters should be taken into consideration for MOSFET: the on-resistance R_{DS_ON}, the minimum gate threshold voltage V_{TH_MIN}, the total gate charge Q_g, the reverse transfer capacitance C_{RSS}, and the maximum drain to source voltage V_{Q_MAX}. The peak switching voltage between drain to source in a SEPIC is given by:

$$V_{SW\_PEAK} = V_{IN} + V_O + V_D \quad (36)$$

Then the V_{Q_MAX} of power MOSFET should be greater than the peak switching voltage.

The peak switching current flowing through the MOSFET is given by:

$$I_{Q\_PEAK} = I_{L1\_PEAK} + I_{L2\_PEAK} \quad (37)$$

The RMS current through the MOSFET I s calculated by:

$$I_{Q\_RMS} = I_O \times \sqrt{\frac{(V_O + V_{IN\_MIN} + V_D) \times (V_O + V_D)}{V_{IN\_MIN}^2}} \quad (38)$$

Then power dissipation in MOSFET can be estimated by:

$$P_{DIS} = I_{Q\_RMS}^2 \times R_{DS\_ON} \times D_{MAX} + (V_O + V_{IN\_MIN}) \times I_{Q\_PEAK} \times \frac{Q_g \times f_{SW}}{I_G} \quad (39)$$

Where

I_G is the gate drive current.

The total power dissipation of MOSFET includes conduction loss as shown in the first term and switching loss as shown in the second term. The total power dissipation should be within package thermal ratings.

Output Diode Selection

The diode at the output side must withstand the reverse voltage when the MOSFET is turned-on. The peak reverse voltage is given by:

$$V_{D\_PEAK} = V_{IN\_MAX} + V_{O\_MAX} \quad (40)$$

The diode should also be capable to flow switch peak current I_{Q_PEAK}.

The power dissipation of the diode is equal to the forward voltage drop multiplies output current. Schottky diodes are recommended here to minimize the power loss.

Coupling Capacitor Selection

For ceramic capacitors with low-ESR, the peak to peak voltage ripple on coupling capacitor is estimated by:

$$\Delta V_{CS} = \frac{I_O \times D_{MAX}}{C_S \times f_{SW}} \quad (41)$$

The maximum voltage across the coupling capacitor is maximum input voltage. The voltage rating of the coupling capacitor must be greater than it.

The RMS current of coupling capacitor is given by:

$$I_{CS\_RMS} = I_O \times \sqrt{\frac{V_O + V_D}{V_{IN\_MIN}}} \quad (42)$$

There is a large RMS current through coupling capacitor relative to output power. Ensure the coupling capacitor can withstand it with good heat generation to have proper thermal performance.

Input Capacitor Selection

The SEPIC has an inductor at input side thus the input current is continuous and triangular. The RMS current flowing through the input capacitor is given by:

$$I_{IN\_RMS} = \frac{\Delta I_{L1}}{\sqrt{12}} \quad (43)$$

Since input current ripple is relative low, the capacitance would be not too critical. While 100μF in total or higher value is strongly recommended in order to provide stable input supply.

Output Capacitor Selection

Similar to boost converter, the SEPIC output capacitor suffers large current ripple. The capacitance must be enough to provide the load current. The maximum voltage ripple in the output capacitor is:

$$\Delta V_{OUT} = \frac{I_O \times D_{MAX}}{C_{OUT} \times f_{SW}} + ESR \times \left(I_{L1\_PEAK} + I_{L2\_PEAK} \right) \quad (44)$$

Assuming ceramic capacitors are used here and ESR can be ignored, the output capacitor is given by:

$$C_{OUT} \geq \frac{I_O \times D_{MAX}}{\Delta V_{OUT} \times f_{SW}} \quad (45)$$

The output capacitor must have an enough RMS current rating to handle the maximum RMS current in the output capacitor, calculated by:

$$I_{COUT\_RMS} = I_O \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}} \quad (46)$$

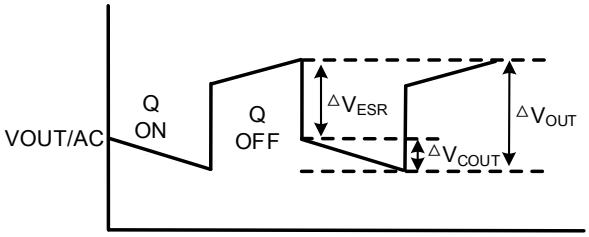


Figure 29. Output Voltage Ripple

APPLICATION INFORMATION

Typical Application(Flyback)

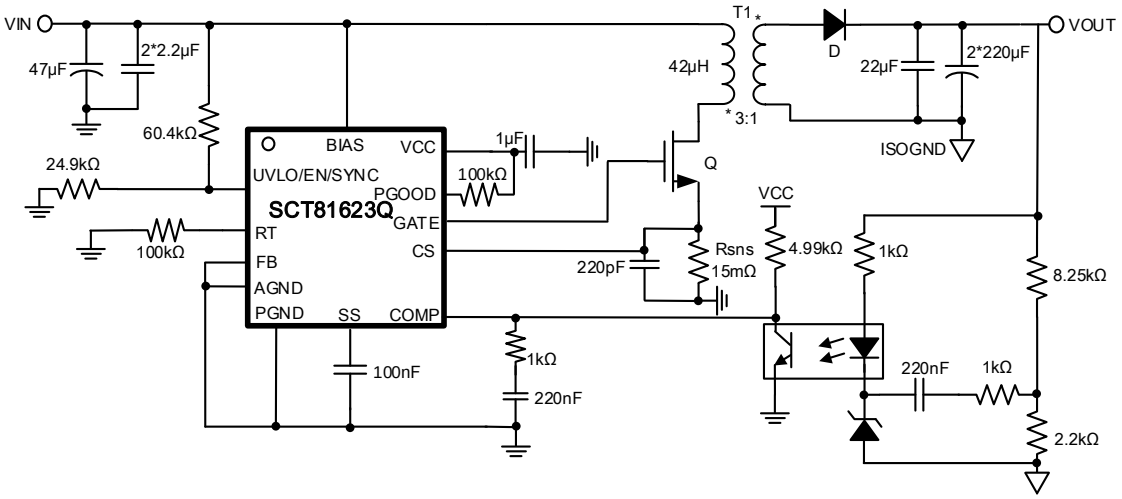


Figure 30. Application Schematic, 8V to 50V, 2A Flyback Regulator at 400kHz +Design Parameters

Design Parameters	Example Value
Input Voltage	8V to 50V
Output Voltage	12V
Maximum Output Current	2A
Switching Frequency	200 KHz
Output voltage ripple (peak to peak)	75mV (Load=2A)

Transformer Selection (Flyback)

Transformer design is critical for flyback application. The first step is to select a proper operation mode. The discontinuous conduction mode (DCM) will minimize the transformer size at the cost of higher rating switch, while the continuous conduction mode (CCM) can achieve higher efficiency at full load and minimize output voltage ripple.

For DC-DC applications, where the input voltage is low, CCM operation is an attractive option to minimize the primary RMS current particularly in higher power systems even though the system's dynamic behavior is considerably difficult to maintain., it's easy to get the maximum duty cycle as below equation:

$$D_{MAX} = \frac{\frac{N_P}{N_S} \times V_O}{V_{IN\_MIN} + \frac{N_P}{N_S} \times V_O} \quad (47)$$

where

- N_P is s the number of turns on the primary side winding
- N_S is s the number of turns on the secondary side winding

SCT recommends to determine the maximum duty cycle below 50%, which brings two benefit for flyback design: first, to get a stable loop, slope compensation is needed when duty cycle is larger than 50%. SCT81623Q also supports external additional slope compensation if duty cycle must be large to ease other designs. Second, the right-half plane zero of the modulator is pushed to high frequencies, helping to improve the load transient response and simplifying the control loop compensation calculations. Then the turns ration between primary side and secondary side N_{PS} can be determined accordingly.

The number of turns on the auxiliary winding is calculated using below equation:

$$N_{AUX} = N_S \times \frac{V_{AUX}}{V_O} \quad (48)$$

Assuming the efficiency of the flyback converter is η, the input power and output power relationship could be derived as shown in below equation:

$$V_{IN} \times I_{LM} \times D \times \eta = V_O \times I_O = P_O \quad (49)$$

where

- I_{LM} is the average current flowing in the transformer primary winding

The current increase of primary inductor during ON period is:

$$\Delta I_{LM} = V_{IN} \times \frac{D \times T_S}{L_P} \quad (50)$$

where

- L_P is the inductance of primary winding
- T_S is the switching period of flyback

Then the L_P can be derived as below equation:

$$L_P = \frac{V_{INMAX}^2 \times \eta}{K_L \times P_O \times f_S} \times \frac{V_O^2 \times N_{PS}^2}{\left(V_{INMAX} + V_O \times N_{PS}\right)^2} \quad (51)$$

where

- K_L is the ripple ratio

A maximum ripple ratio between 30% and 70% results in a good balance of the total power loss of the transformer, matching the down slope of the transformer current to the internal slope compensation and the increasing the right half plane zero frequency. The maximum ripple ratio of the inductor current is set to 60%. In CCM operation, the maximum primary winding ripple current occurs when the supply voltage is at the maximum value.

The peak primary winding current occurs at the minimum supply voltage as below equation:

$$I_{L\_PEAK} = I_{LM} + \frac{\Delta I_{LM}}{2} = \frac{P_O}{V_{INMIN} \times D_{MAX} \times \eta} + \frac{V_{INMIN} \times D_{MAX}}{2 \times L_P \times f_S} \quad (52)$$

The calculated turns ratio, primary winding inductance and peak current can be used to determine the magnetic core of the transformer, number of turns on primary and secondary windings, as well as wire thickness.

MOSFET and Diode Selection

The voltage rating of the MOSFET and the diode needs to be chosen with appropriate margin as both of them suffers from high voltage spike. In case of MOSFET, the primary leakage inductance resonates with output capacitance of MOSFET and similarly in case of diode, secondary leakage inductance resonates with diode capacitance and results into high voltage spikes. Considering the spike voltage, usually choose 1.5~2 times of the voltage stage as the voltage rating to ensure sufficient margin.

The voltage rating of MOSFET and Diode could be derived as shown in below equation:

$$V_{ds\_MOS} = (1.5 \sim 2) \times \left(V_{IN\_MAX} + \frac{N_P}{N_S} \times V_O \right) \quad (53)$$

$$V_{R\_diode} = (1.2 \sim 1.5) \times \left(V_{IN\_MAX} \times \frac{N_S}{N_P} + V_O \right)$$

The current RMS rating of MOSFET could be derived as shown in below equation:

$$I_{MOS\_RMS} = \sqrt{D \times \left(\left(\frac{P_O}{V_{IN\_MIN} \times D} \right)^2 + \frac{\Delta I_{LM}{}^2}{12} \right)} \quad (54)$$

The current rating of MOSFET and Diode should at least be I_{L_PEAK} and I_O respectively.

Output Capacitor Selection

The output capacitor is required to smooth the load voltage ripple, provides an energy source during load transients and provides energy to the load during the on-time of the MOSFET. A practical way to size the output capacitor is based on the required load transient specification. The load transient specification is related to the control loop crossover frequency. For this estimate it is expected that the control loop cross over frequency is set to 1/5th the right half plane zero frequency. This right half plane zero frequency is calculated using below equation:

$$f_{CROSS} = \frac{f_{RHZP}}{5} = \frac{N_P{}^2}{N_S{}^2} \times \frac{\frac{V_O{}^2}{P_O} \times (1-D)^2}{5 \times 2\pi \times L_M} \quad (55)$$

Then below equation is used to calculate the estimated load capacitance to achieve the specified load transient requirements.

$$C_O \geq \frac{\Delta I_O}{2\pi \times f_{CROSS} \times \Delta V_{RIPPLE}} \quad (56)$$

where

- ΔI_O is the difference in the load current conditions
- ΔV_{RIPPLE} is the specified overshoot voltage specification and undershoot voltage specification

Input Capacitor Selection

The input capacitors smooth the supply ripple voltage during operation. Below equation is used to estimate the required input capacitor based on the supply ripple voltage specification.

$$C_{IN} \geq \frac{\frac{P_O}{V_{IN\_MIN}} \times (1-D)}{f_{SW} \times \Delta V_{SUPPLY}} \quad (57)$$

Application Waveforms

VBIAS=12V, Vout=12V, unless otherwise noted

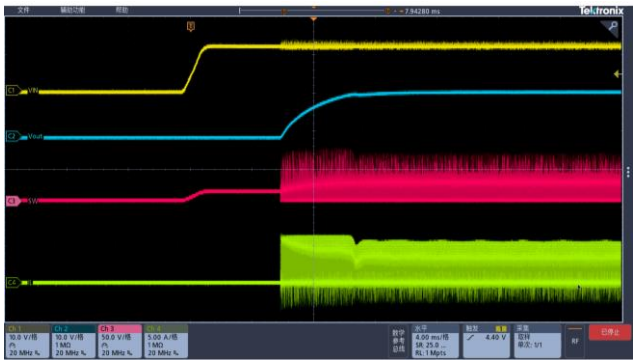


Figure 31. Power up(Iload=2A)

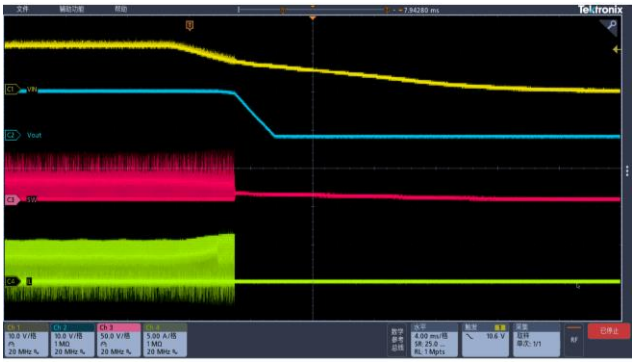


Figure 32. Power down(Iload=2A)

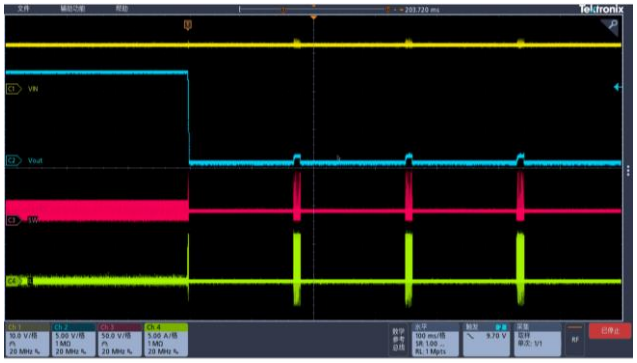


Figure 33. Over current protection (Iload=5A)

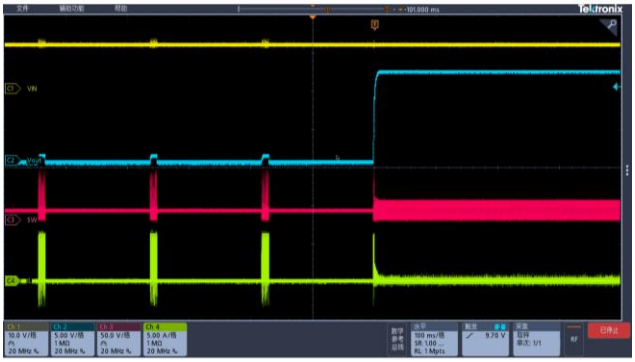


Figure 34. Over current recovery (Iload=5A)

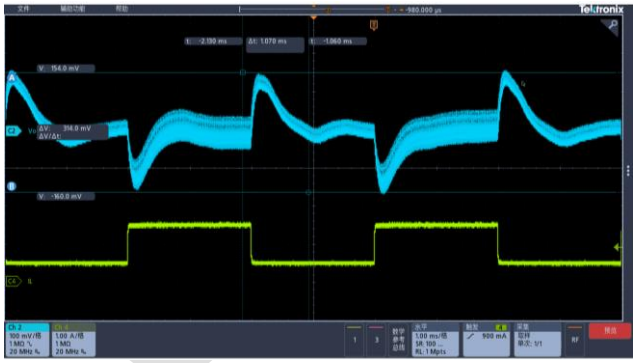


Figure 35. LoadTrans (Iload=0.5A-1.5A)

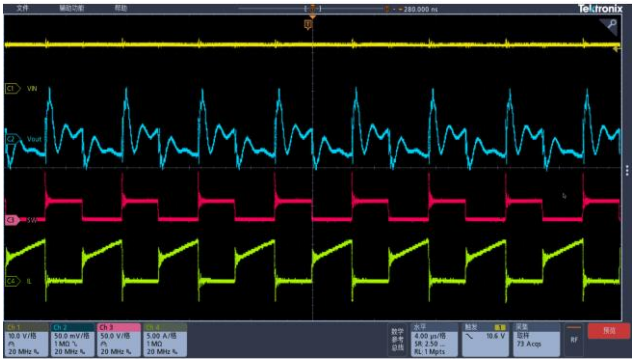


Figure 36. steady-state (Iload=2A)

Layout Guideline

The performance of switching converters heavily depends on the quality of the PCB layout. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimize generation of unwanted EMI.

- Use a small size ceramic capacitor for C_{OUT}.
- Make the switching loop (C_{OUT} to D to Q to R_S to C_{OUT}) as small as possible.
- Leave a copper area near the D diode for thermal dissipation.
- Put the device near the R_S resistor.
- Put the C_{VCC} capacitor as near the device as possible between the VCC and PGND pins.
- Use a wide and short trace to connect the PGND pin directly to the center of the sense resistor.
- Connect the CS pin to the center of the sense resistor. If necessary, use vias.
- Connect a filter capacitor between CS pin and power ground trace.
- Connect the COMP pin to the compensation components.
- Connect the AGND pin directly to the analog ground plane. Connect the AGND pin to the UVLO, RT, SS, and FB components.
- Connect the exposed pad to the AGND and PGND pins under the device.
- Connect the GATE pin to the gate of the Q. If necessary, use vias.
- Make the switching signal loop (GATE to Q to R_S to PGND to GATE) as small as possible.
- Add several vias under the exposed pad to help conduct heat away from the device. Connect the vias to a large ground plane on the bottom layer.

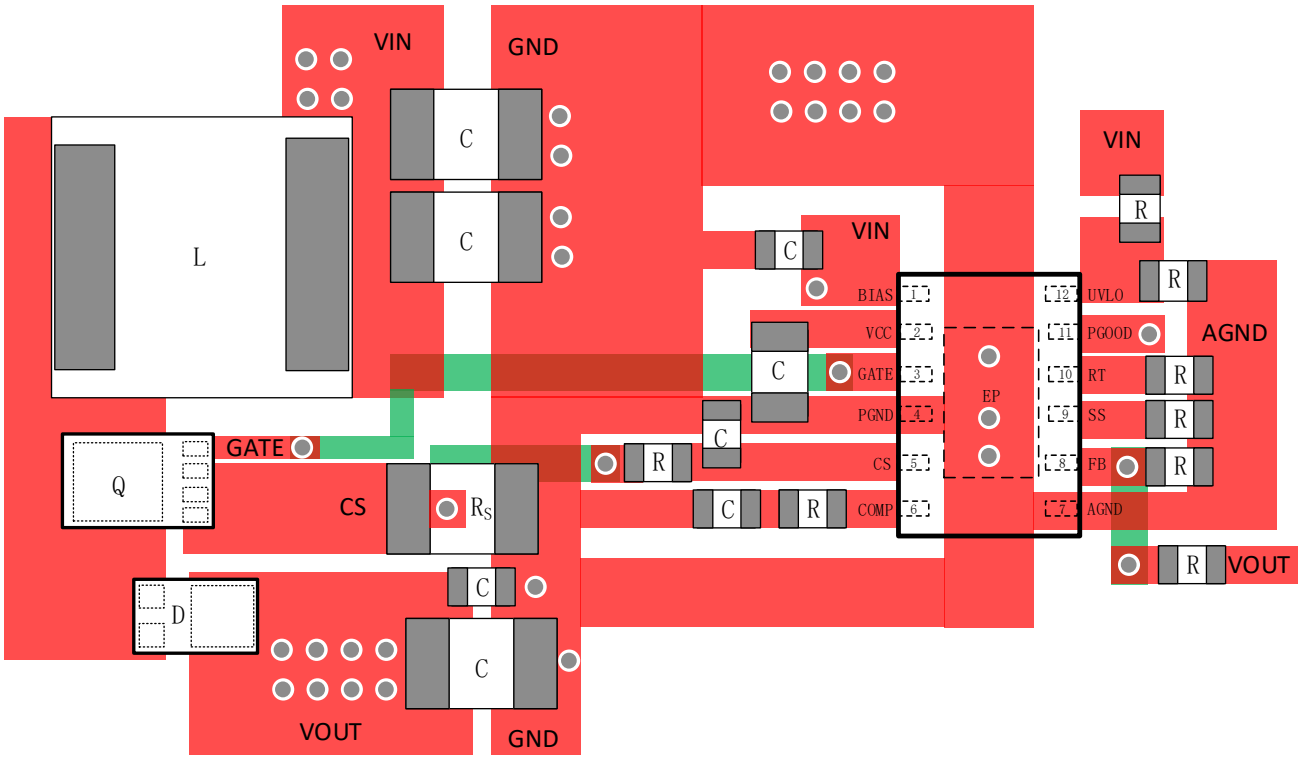
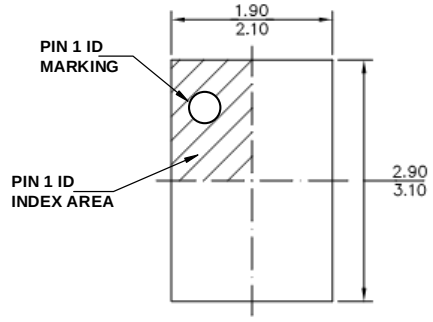
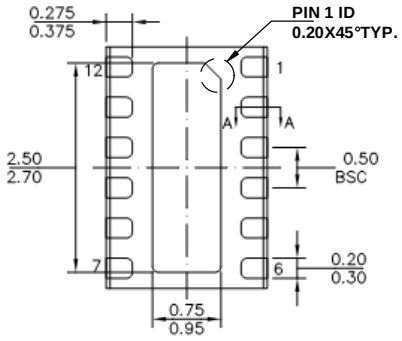


Figure 37. BOOST PCB Layout

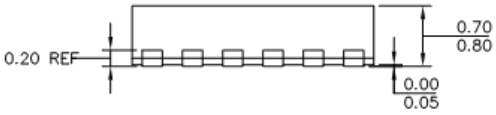
PACKAGE INFORMATION



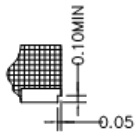
TOP VIEW



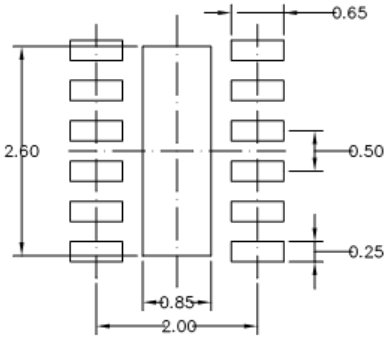
BOTTOM VIEW



SIDE VIEW



SECTION A-A
TYPICAL

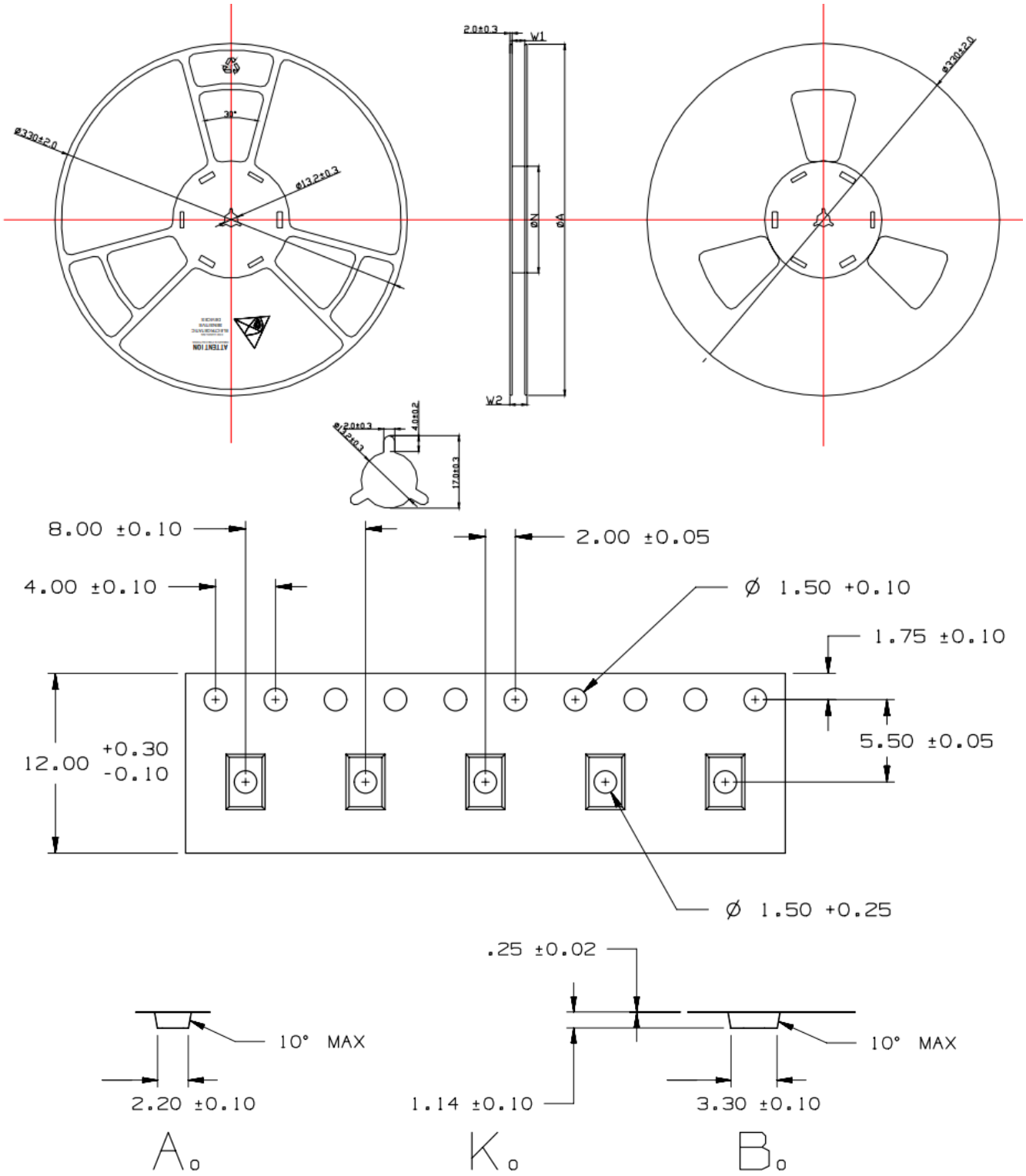


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

TAPE AND REEL INFORMATION



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