SGM25733Q
Low Quiescent Current Ideal Diode Controller with Reverse Battery Protection

GENERAL DESCRIPTION

The SGM25733Q, an ideal diode controller used as an ideal diode rectifier with external NMOS, offers low-loss reverse polarity protection, which has a mere 20mV forward voltage drop. Its 3.2V to 65V wide supply input range facilitates control over various DC bus voltages commonly found in automotive battery systems like 12V, 24V, and 48V. The device supports input voltage downs to 3.2V, making it well-suited for automotive systems with stringent cold crank conditions. It also protects connected loads against reverse supply voltages as low as -65V.

Controlling the GATE of MOSFET, the device regulates the 20mV forward voltage drop. The control architecture ensures the external MOSFET turns off in the event of reverse current, effectively preventing any steady-state reverse current flow. With a rapid reverse current blocking response time of less than 0.88μs, the device is well-suited for applications requiring output voltage hold-up during ISO7637 pulse tests, as well as during input micro-short and power fail scenarios.

This controller incorporates a charge pump gate driver for an external NMOS. Its high voltage rating simplifies system designs for automotive EMC transient interference standard ISO7637. When the enable pin is held low, the controller remains disabled and consumes only about 1.2μA of supply current.

The device is AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and it is suitable for automotive applications.

The SGM25733Q is available in Green SOT-23-6 and TSOT-23-8 packages.

FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
  Device Temperature Grade 1
  T_A = -40℃ to +125℃
- **Functional Safety-Capable**
- **Documentation Available for Assisting in Functional Safety System Design**
- **3.2V to 65V Input Range (3.9V Start-Up)**
- **-65V Reverse Voltage Rating**
- **Charge Pump for External NMOS**
- **Regulation of 20mV Forward Voltage Drop from ANODE to CATHODE**
- **Enable Pin Feature**
- **1.2μA Shutdown Current (EN = Low)**
- **98μA Operating Quiescent Current (EN = High)**
- **1.8A Peak Gate Turn-Off Current**
- **Quick Response Time to Reverse Current Blocking: < 0.88μs**
- **Compliance with Automotive ISO7637 Transient Requirements with Appropriate TVS Diode**
- **Available in Green SOT-23-6 and TSOT-23-8 Packages**

APPLICATIONS

Automotive Infotainment Systems: Digital Cluster and Head Unit
Active ORing for Redundant Power Systems
Automotive ADAS Systems: Camera Integration
Enterprise Power Supplies
Industrial Factory Automation: PLC Integration

TYPICAL APPLICATION SCHEMATIC

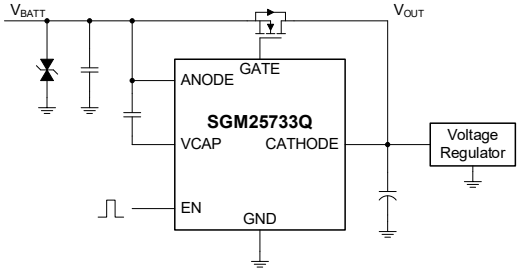


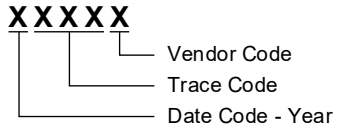
Figure 1. Application Schematic

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM25733Q	SOT-23-6	-40℃ to +125℃	SGM25733QN6G/TR	175 XXXXX	Tape and Reel, 3000
	TSOT-23-8	-40℃ to +125℃	SGM25733QTN8G/TR	XXXXX 176	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Pins
ANODE to GND ..... -65V to 65V
EN to GND, (V_{ANODE} > 0V) ..... -0.3V to 65V
EN to GND, (V_{ANODE} ≤ 0V) ..... V_{ANODE} to 65V + V_{ANODE}
Output Pins
GATE to ANODE ..... -0.3V to 15V
VCAP to ANODE ..... -0.3V to 15V
CATHODE to GND, (V_{ANODE} > 0V)..... -0.3V to 75V
CATHODE to GND, (V_{ANODE} ≤ 0V).. V_{ANODE} to 75V + V_{ANODE}
Output to Input Pins
CATHODE to ANODE..... -5V to 75V
Package Thermal Resistance
SOT-23-6, θ_{JA}..... 145.4℃/W
SOT-23-6, θ_{JB}..... 39.7℃/W
SOT-23-6, θ_{JC} ..... 89.1℃/W
TSOT-23-8, θ_{JA} ..... 135.9℃/W
TSOT-23-8, θ_{JB} ..... 56.3℃/W
TSOT-23-8, θ_{JC} ..... 91.8℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility (1) (2)
HBM (Connect EN Pin to Anode Pin).....±2000V
HBM (All Pins Except EN) (3).....±2000V
CDM .....±1000V

NOTES:

1. For human body model (HBM), all pins comply with AEC-Q100-002 specification.

2. For charged device model (CDM), all pins comply with AEC-Q100-011 specification.

3. The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. 2kV rating for all pins except EN, which is rated for 1.5kV.

RECOMMENDED OPERATING CONDITIONS

Input Pins
ANODE to GND.....-60V to 60V
CATHODE to GND 60V
EN to GND.....-60V to 60V
Input to Output Pins
ANODE to CATHODE ..... ≥ -70V
External Capacitance
ANODE.....≥ 22nF
CATHODE, VCAP to ANODE.....≥ 0.1μF
External MOSFET Max V_{GS} Rating
GATE to ANODE ..... ≥ 15V
Operating Ambient Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

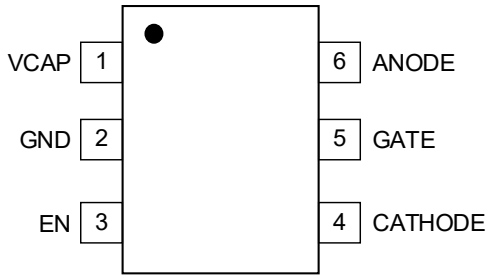
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

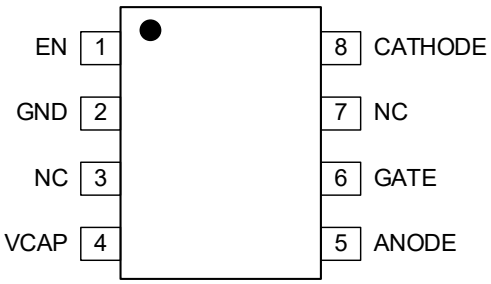
PIN CONFIGURATION

(TOP VIEW)



SOT-23-6

(TOP VIEW)



TSOT-23-8

PIN DESCRIPTION

PIN		NAME	I/O (1)	FUNCTION
SOT-23-6	TSOT-23-8			
1	4	VCAP	O	Charge Pump Output. This pin is connected to external charge pump capacitor.
2	2	GND	G	Ground.
3	1	EN	I	Enable. This pin is connected to ANODE during always ON operation.
4	8	CATHODE	I	Cathode of the Diode. This pin is connected to the drain of the external MOSFET.
5	6	GATE	O	Gate Drive Output. This pin is connected to the gate of the external MOSFET.
6	5	ANODE	I	Anode of the Diode and Input Power. This pin is connected to the source of the external MOSFET.
-	3, 7	NC	-	No Connection.

NOTE: 1. I = input, O = output, G = ground.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, all typical values are measured at T_J = +25℃, V_{ANODE} = 12V, C_{VCAP} = 0.1μF and V_{EN} = 3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{ANODE} Supply Voltage						
Operating Input Voltage	V_{ANODE}		4	12	60	V
VANODE POR Rising Threshold	V_{ANODE_POR}				3.9	V
VANODE POR Falling Threshold			2.46	2.78	3.08	V
VANODE POR Hysteresis	$V_{ANODE\_POR\_Hys}$		0.73		1.03	V
Shutdown Supply Current	I_{SD}	V_{EN} = 0V		1.2	3.0	μA
Operating Quiescent Current	I_Q			98	135	μA
Enable Input						
Enable Input Low Threshold	V_{EN_IL}		0.90	1.20	1.52	V
Enable Input High Threshold	V_{EN_IH}		1.79	2.11	2.45	V
Enable Hysteresis	V_{EN_Hys}		0.59	0.91	1.20	V
Enable Sink Current	I_{EN}	V_{EN} = 12V		1.9	4.0	μA
V_{ANODE} to $V_{CATHODE}$						
Regulated Forward V_{AK} Threshold	V_{AK_REG}		11	20	29	mV
V_{AK} Threshold for Full Conduction Mode	V_{AK}		31	46	61	mV
V_{AK} Threshold for Reverse Current Blocking	V_{AK_REV}		-22	-11	-1	mV
Regulation Error AMP Transconductance (1)	Gm		1200	1800	3100	μA/V
Gate Drive						
Peak Source Current	I_{GATE}	V_{ANODE} - $V_{CATHODE}$ = 100mV, V_{GATE} - V_{ANODE} = 5V	5	10.2		mA
Peak Sink Current		V_{ANODE} - $V_{CATHODE}$ = -100mV, V_{GATE} - V_{ANODE} = 5V		1800		mA
Regulation Max Sink Current		V_{ANODE} - $V_{CATHODE}$ = 0V, V_{GATE} - V_{ANODE} = 5V	6	24		μA
Discharge Switch R_{DSON}	R_{DSON}	V_{ANODE} - $V_{CATHODE}$ = -100mV, V_{GATE} - V_{ANODE} = 100mV	0.4		2.3	Ω

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, all typical values are measured at T_J = +25℃, V_{ANODE} = 12V, C_{VCAP} = 0.1μF and V_{EN} = 3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Charge Pump						
Charge Pump Source Current (Charge Pump On)	I_{VCAP}	V_{VCAP} - V_{ANODE} = 7V	200	300	400	μA
Charge Pump Sink Current (Charge Pump Off)		V_{VCAP} - V_{ANODE} = 13V		4	10	μA
Charge Pump Voltage at V_{ANODE} = 3.2V	V_{VCAP} - V_{ANODE}	I_{VCAP} ≤ 10μA	7.6			V
Charge Pump Turn-On Voltage			9.1	10.5	12.0	V
Charge Pump Turn-Off Voltage			10.0	11.6	13.0	V
Charge Pump Enable Comparator Hysteresis			0.6	1.0	1.4	V
V_{VCAP} - V_{ANODE} UV Release	V_{VCAP_UVLO}	V_{ANODE} - $V_{CATHODE}$ = 100mV, rising edge	5.50	6.28	7.10	V
V_{VCAP} - V_{ANODE} UV Threshold		V_{ANODE} - $V_{CATHODE}$ = 100mV, falling edge	4.60	5.36	6.10	V
CATHODE						
CATHODE Sink Current	$I_{CATHODE}$	V_{ANODE} = 12V, V_{ANODE} - $V_{CATHODE}$ = -100mV		1.9	3.0	μA
		V_{ANODE} - $V_{CATHODE}$ = -100mV		1.9	3.0	μA
		V_{ANODE} = -12V, $V_{CATHODE}$ = 12V		-0.01	0.50	μA

NOTE:

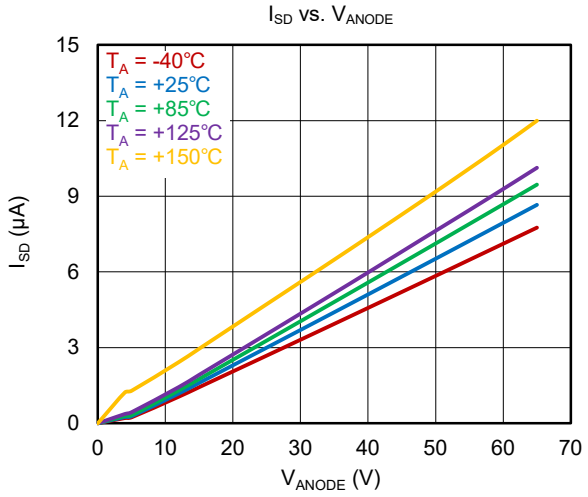
1. Parameter assured by design and characterization.

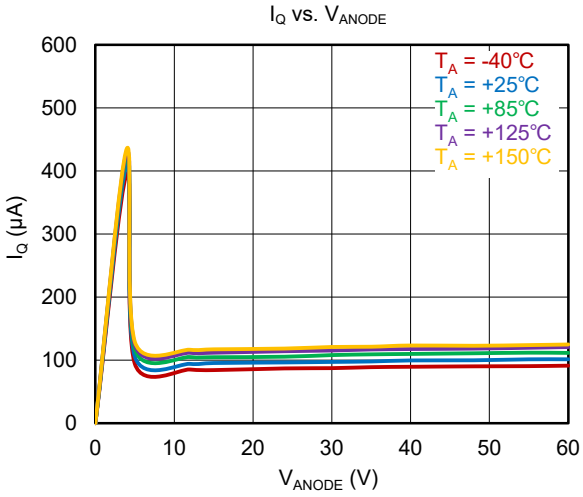
SWITCHING CHARACTERISTICS

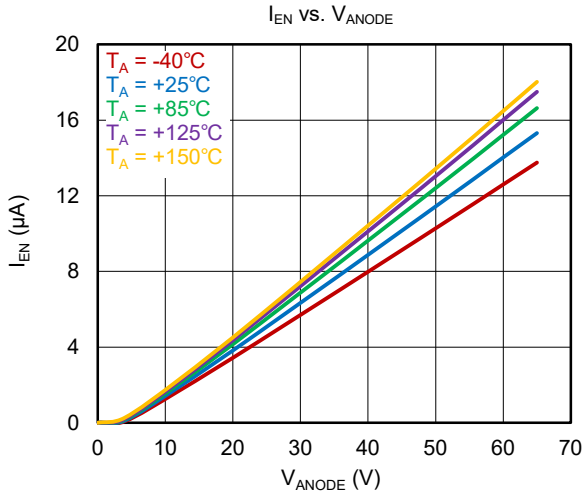
(T_J = -40℃ to +125℃, all typical values are measured at T_J = +25℃, V_{ANODE} = 12V, C_{VCAP} = 0.1μF and V_{EN} = 3.3V, unless otherwise noted.)

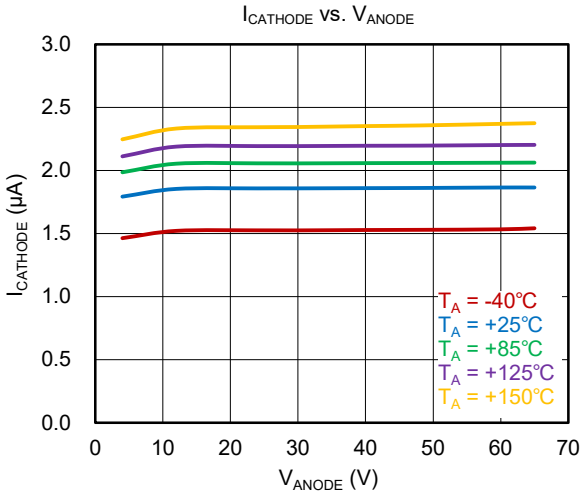
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Enable to Gate Turn-On Delay	EN_{TDLY}	V_{VCAP} > $V_{VCAP\_UVLO\_R}$		83	121	μs
Reverse Voltage Detection to Gate Turn-Off Delay	$t_{Reverse\_Delay}$	V_{ANODE} - $V_{CATHODE}$ = 100mV to -100mV		0.44	0.88	μs
Forward Voltage Detection to Gate Turn-On Delay	$t_{Forward\_Recovery}$	V_{ANODE} - $V_{CATHODE}$ = -100mV to 700mV		1.91	3.60	μs

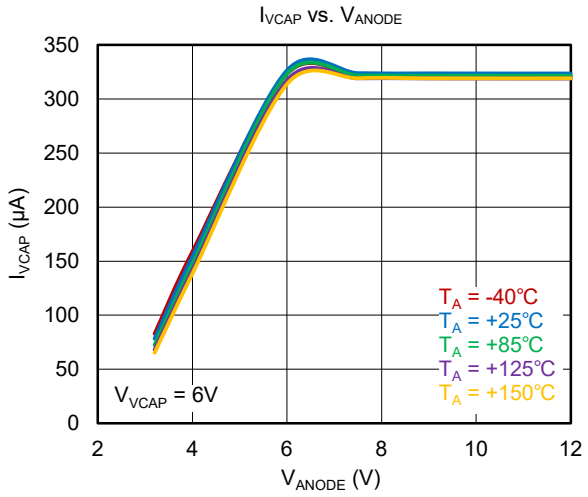
TYPICAL PERFORMANCE CHARACTERISTICS

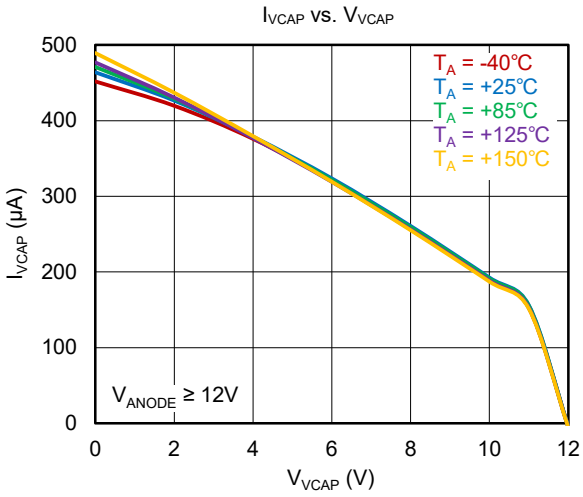






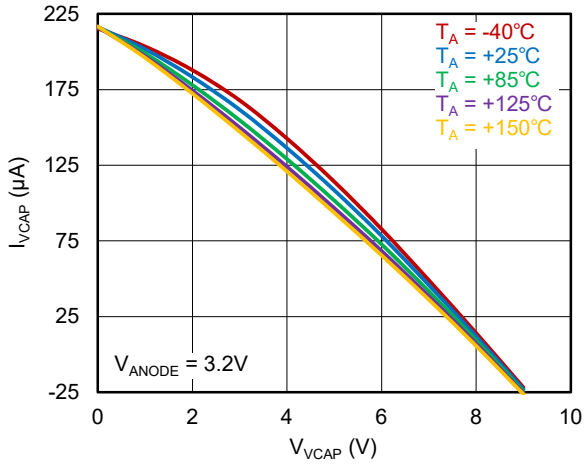




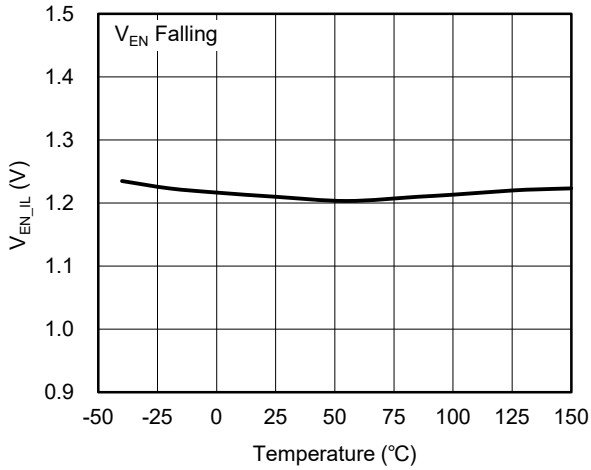


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

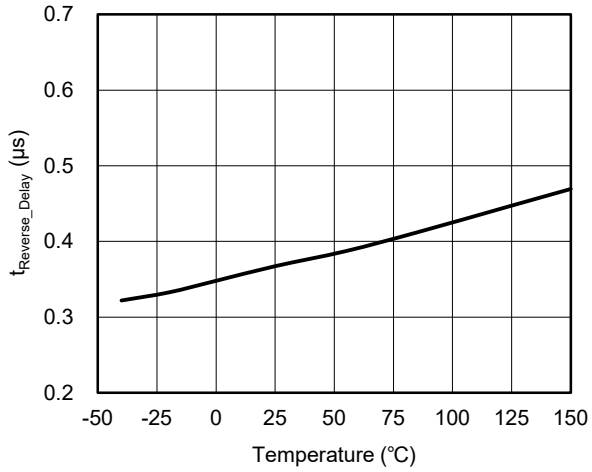
I_{VCAP} vs. V_{VCAP}



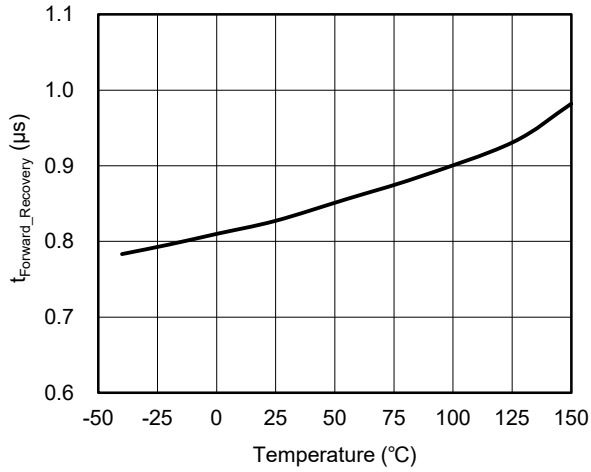
V_{EN_IL} vs. Temperature



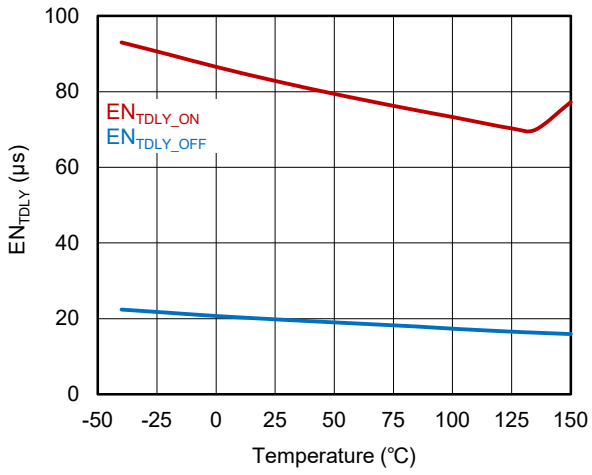
$t_{Reverse\_Delay}$ vs. Temperature



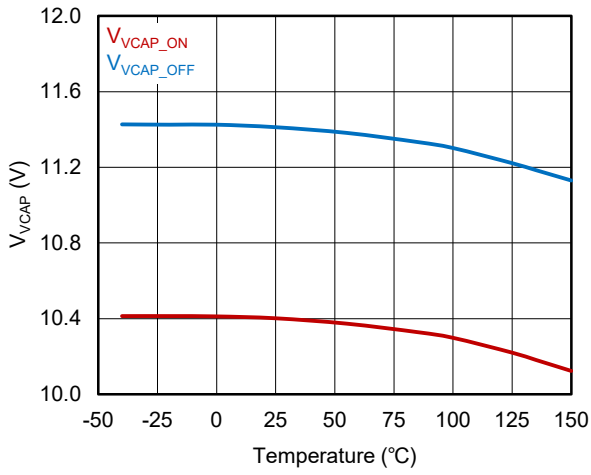
$t_{Forward\_Recovery}$ vs. Temperature



EN_{TDLY} vs. Temperature

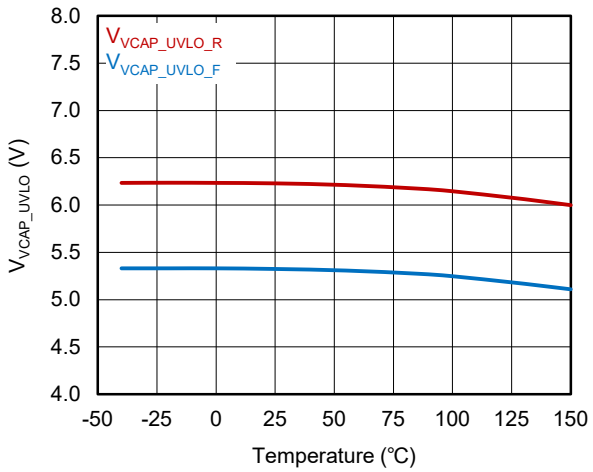


V_{VCAP} vs. Temperature

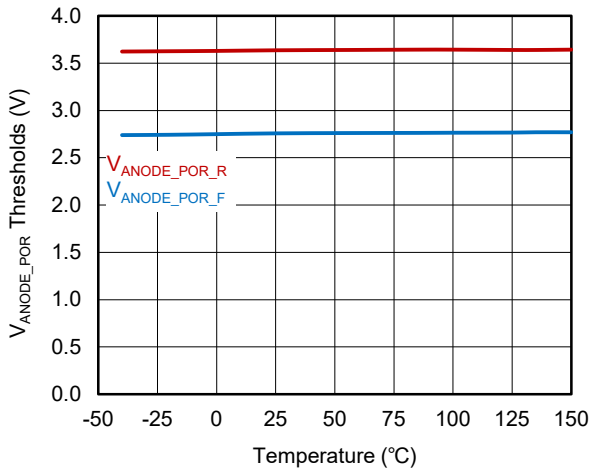


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

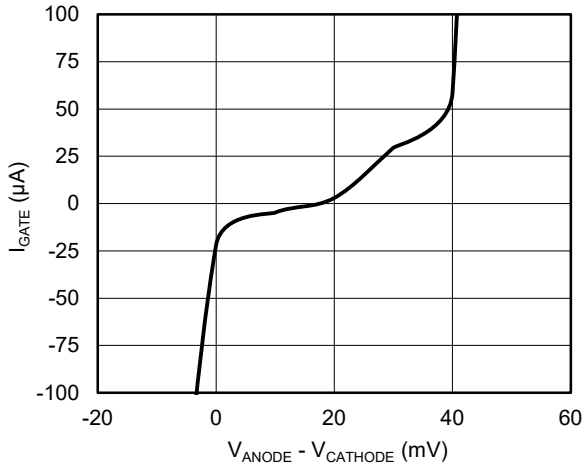
V_{VCAP_UVLO} vs. Temperature



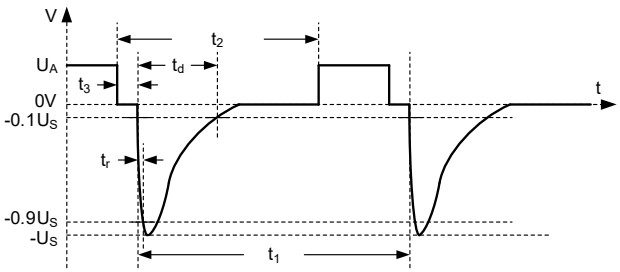
V_{ANODE_POR} Thresholds vs. Temperature



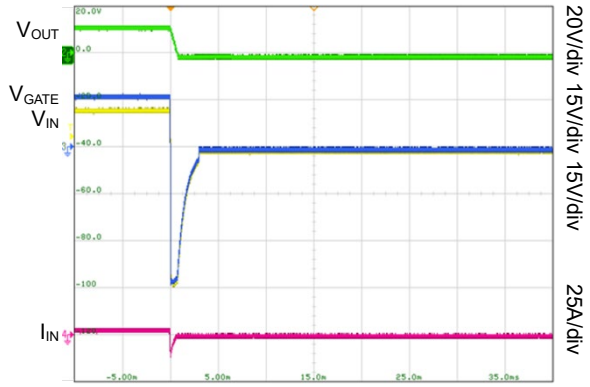
I_{GATE} vs. Forward Voltage Drop



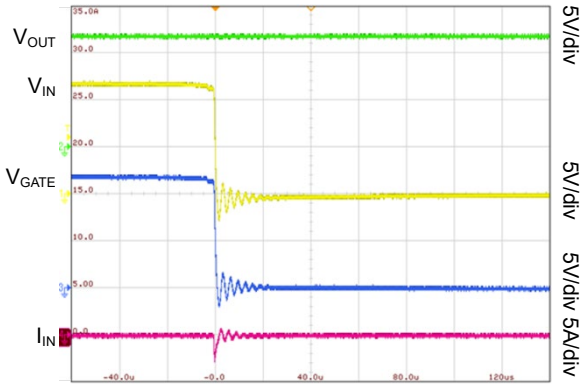
ISO7637-2 Pulse 1



Response to ISO7637-2 Pulse 1



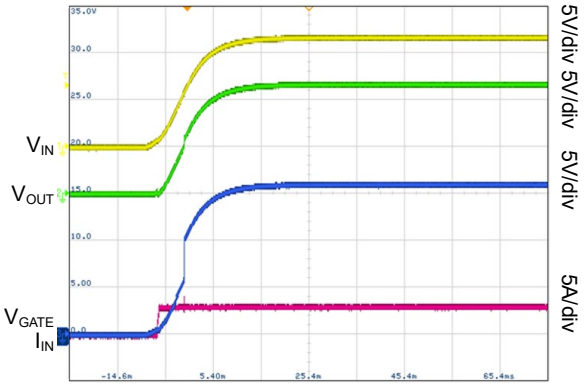
Reverse Current Blocking



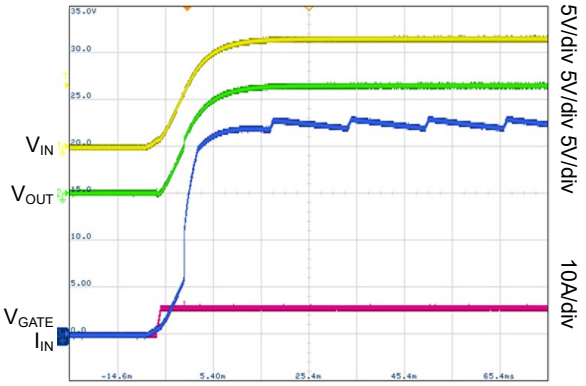
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, C_{VCAP} = 0.1μF and C_{OUT} = 2.2μF, unless otherwise noted.

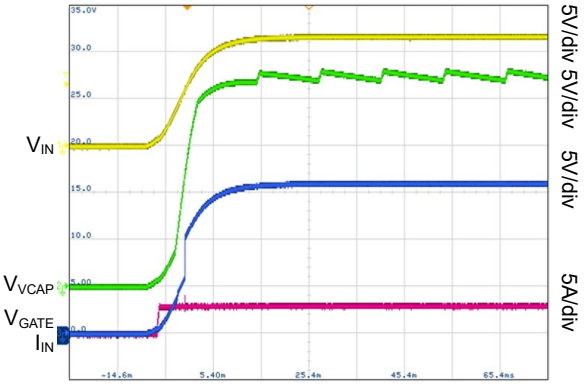
Start-Up, 3A Load



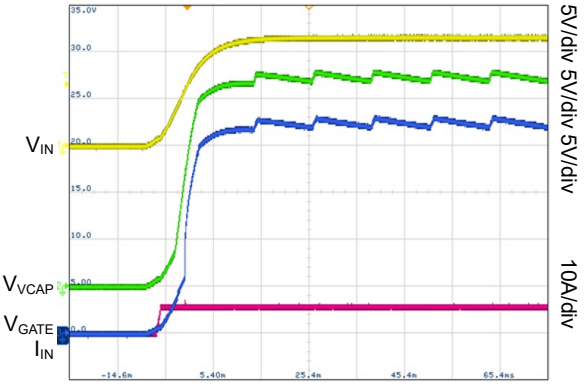
Start-Up, 5.8A Load



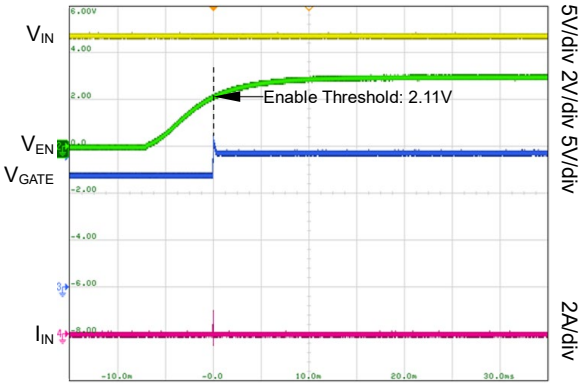
V_{VCAP} During Start-Up, 3A Load



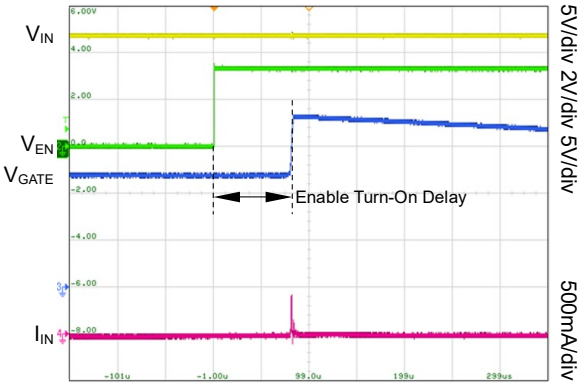
V_{VCAP} During Start-Up, 5.8A Load



Enable Threshold



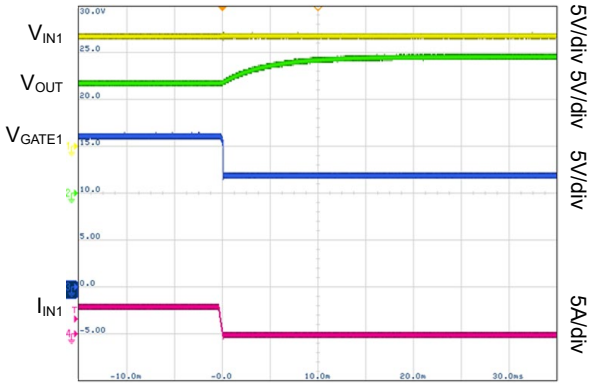
Enable Turn-On Delay



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

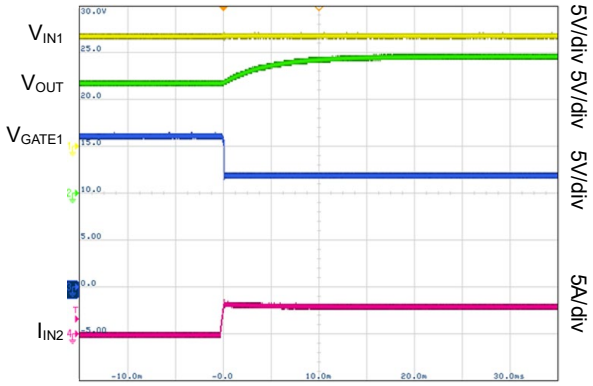
T_A = +25℃, C_{VCAP} = 0.1μF, C_{OUT} = 470μF, unless otherwise noted.

ORing - V_{IN1} (12V) to V_{IN2} (15V) Switch Over



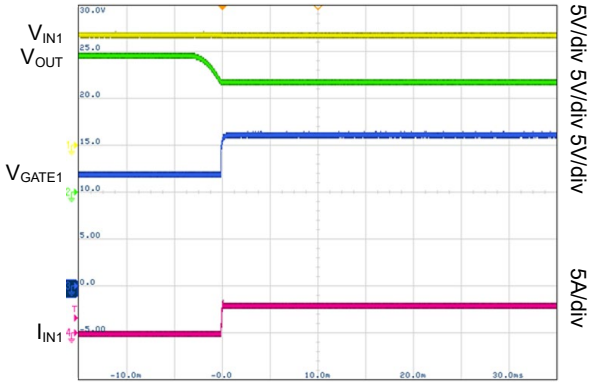
Time (5ms/div)

ORing - V_{IN1} (12V) to V_{IN2} (15V) Switch Over



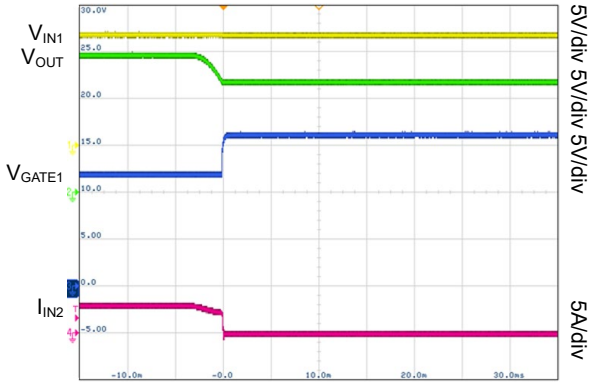
Time (5ms/div)

ORing - V_{IN2} (15V) to V_{IN1} (12V) Switch Over



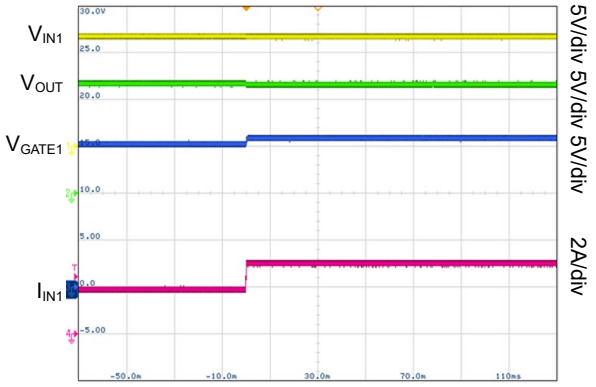
Time (5ms/div)

ORing - V_{IN2} (15V) to V_{IN1} (12V) Switch Over



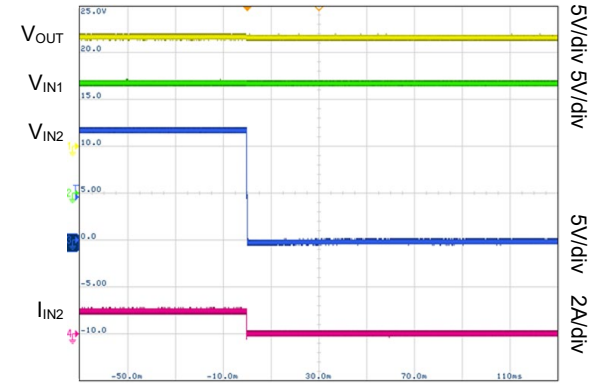
Time (5ms/div)

ORing - V_{IN2} Fail and Switch Over to V_{IN1}



Time (20ms/div)

ORing - V_{IN2} Fail and Switch Over to V_{IN1}



Time (20ms/div)

TIMING DIAGRAMS

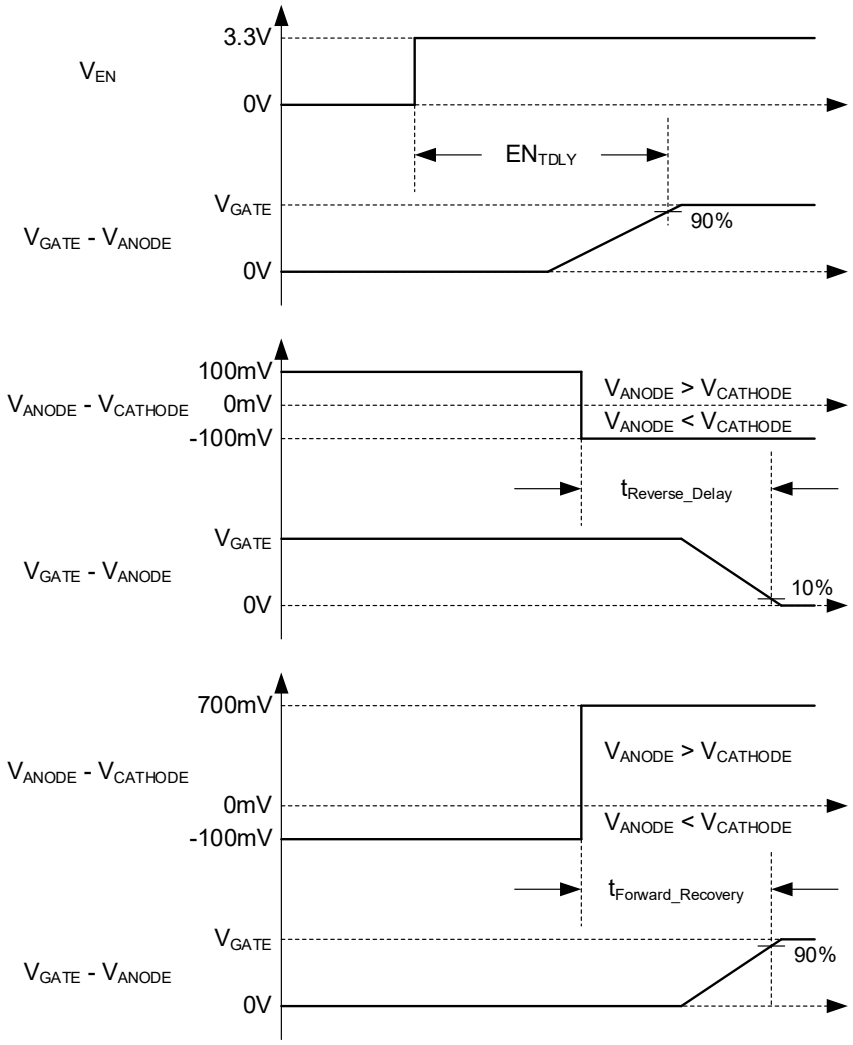


Figure 2. Timing Diagrams

FUNCTIONAL BLOCK DIAGRAM

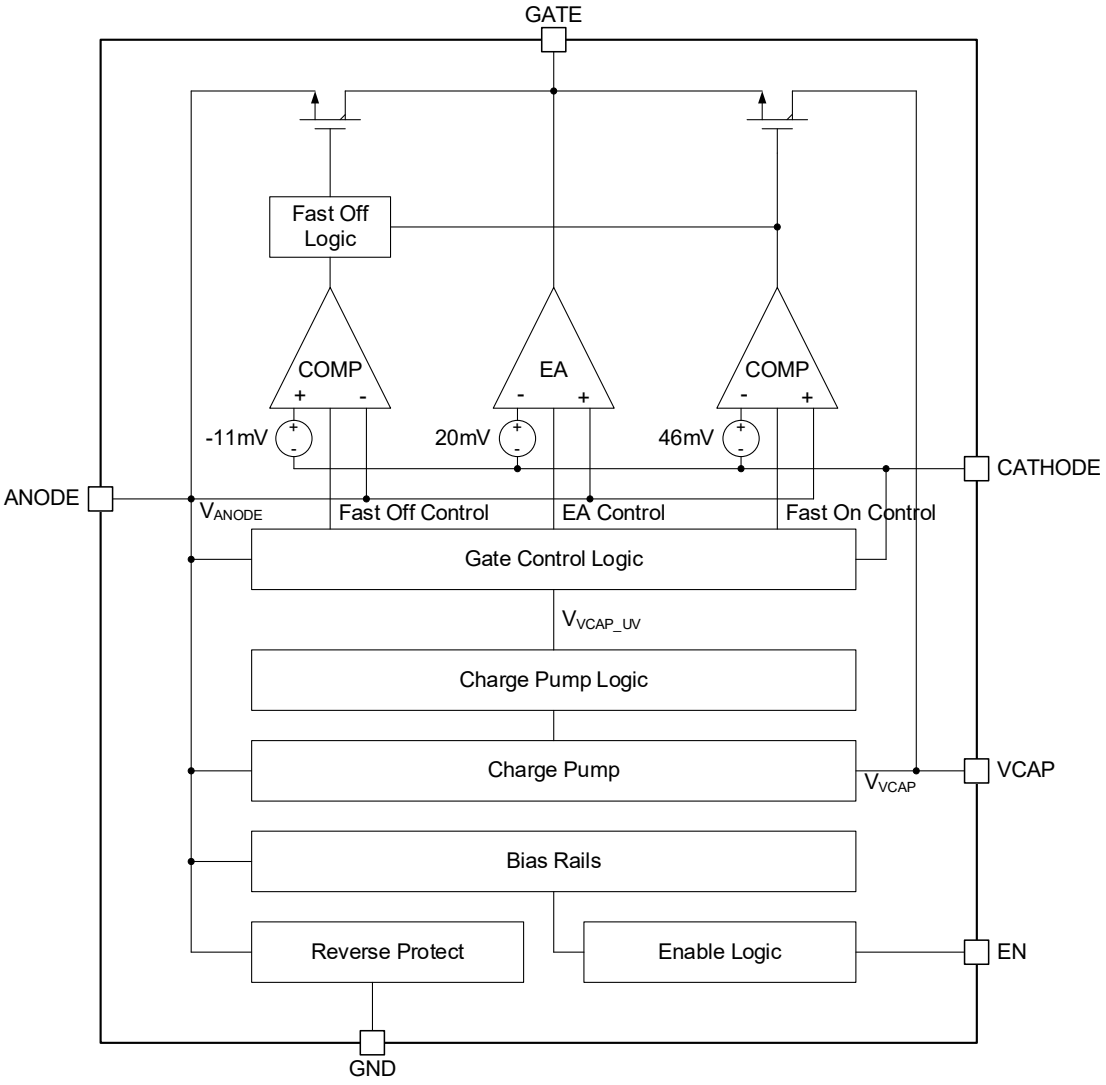


Figure 3. Block Diagram

DETAILED DESCRIPTION

The SGM25733Q ideal diode controller integrates all the essential functions for building a fast, efficient reverse polarity protection circuit or implementing an ORing configuration, all while requiring minimal external components. At the same time, it minimizes the amount of external components. This user-friendly ideal diode controller is combined with an NMOS situated externally. The user-friendly ideal diode controller, combined with an external NMOS, replaces PMOSs or Schottky diodes for reverse polarity protection. Its internal charge pump drives the MOSFET with a max 15V gate voltage.

The device constantly measures the voltage across the MOSFET via the ANODE and CATHODE pins, dynamically adjusting the GATE-to-ANODE voltage to maintain a forward voltage drop of 20mV. This closed-loop control mechanism allows for smooth MOSFET turn-off during reverse current conditions and guarantees zero steady-state reverse current. When the voltage difference between the ANODE and CATHODE pins is lower than -11mV, it triggers the detection of a rapid reverse current event. Subsequently, an internal connection is made between the GATE pin and the ANODE pin, effectively deactivating the external NMOS. And the body diode takes over to block all reverse current flows. There is also an enable pin called EN. By using this pin, the SGM25733Q can enter shutdown mode, which disables the NMOS and reduces the quiescent current to the minimum.

Input Voltage

The ANODE pin supplies power to the internal circuitry of the SGM25733Q. Generally, it consumes 98μA when it is enabled and 1.2μA when disabled. When the voltage of the ANODE pin exceeds the POR Rising threshold, the SGM25733Q will operate either in shutdown mode or conduction mode, depending on the voltage of the EN pin. The designed voltage range from the ANODE to GND is from 65V to -65V. This enables the SGM25733Q to endure negative voltage transients.

Charge Pump

The external NMOS is driven by the voltage produced by the charge pump. An external charge-pump capacitor is positioned between the VCAP and ANODE pins. This capacitor supplies the energy required to activate the external MOSFET. For the charge pump to deliver current to the external capacitor, the EN pin voltage must exceed the defined input high threshold, V_{EN_IH}. Once enabled, the charge pump typically provides a charging current of 300μA. When the EN pin is set to a low level, the charge pump remains inoperative. In order to guarantee the external MOSFET can be driven to a voltage higher than its specified threshold, the voltage between VCAP pin and ANODE pin must exceed the under-voltage lockout threshold, which is typically 6.28V. This condition must be met before enabling the internal gate driver. Calculate the initial gate driver enable delay using Equation 1. Here, C_{VCAP} represents the charge-pump capacitance connected between the ANODE pin and VCAP pin, and $V_{VCAP\_UVLO\_R}$ = 6.28V (TYP).

$$t_{DRV\_EN} = 83\mu s + C_{VCAP} \times \frac{V_{VCAP\_UVLO\_R}}{300\mu A} \quad (1)$$

To eliminate gate drive chatter, approximately 900mV of hysteresis is applied to the VCAP under-voltage lockout threshold. The charge pump continues operating until the VCAP-to-ANODE voltage rises to 11.6V (TYP). Once this voltage level is reached, the charge pump is switched off. This action results in a reduction of the current consumption on the ANODE pin. The charge pump remains in the disabled state until the voltage from VCAP to ANODE drops below 10.5V typically. Once this voltage condition is met, the charge pump is activated. As illustrated in Figure 4, the voltage between VCAP and ANODE cycles through charging and discharging processes within the range of 10.5V to 11.6V. This on-off operation of the charge pump serves to reduce the quiescent operating current of the SGM25733Q. When disabled, the charge pump typically sinks a current of 4μA.

DETAILED DESCRIPTION (continued)

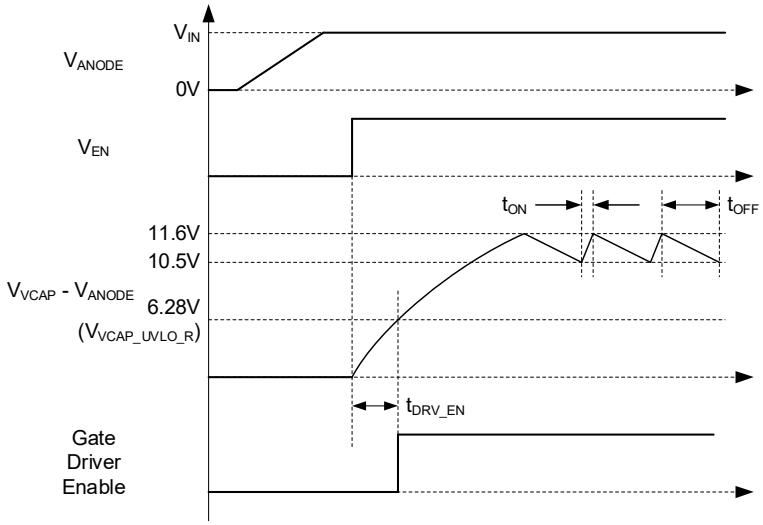


Figure 4. Charge Pump Operation

Gate Driver

The gate driver controls the external NMOS by adjusting the GATE to ANODE voltage to match the appropriate operating mode. Depending on the voltage difference between the ANODE pin and CATHODE pin, there are three distinct operational modes for the gate driver. These are forward regulation mode, full conduction mode, and reverse current protection. These three modes are described in more detail in the *Conduction Mode* section. Figure 5 illustrates the operating modes of the SGM25733Q as a function of the ANODE-to-CATHODE voltage. Transition from regulated conduction mode to full conduction mode occurs at 46mV, while the switch to reverse current protection mode happens when the ANODE-to-CATHODE voltage drops below -11mV.

In order to enable the gate driver, three specific requirements must all be satisfied:

- The voltage at the EN pin must exceed the Enable Input High Threshold.
- The VCAP-to-ANODE voltage must exceed the under-voltage lockout threshold.
- The ANODE voltage must exceed the VANODE POR rising threshold.

If these conditions are not met, the GATE pin is internally pulled to the ANODE pin. This ensures the external MOSFET is turned off. Once the conditions are satisfied, the gate driver functions according to the appropriate mode based on the ANODE-to-CATHODE voltage.

Enable

The SGM25733Q features an enable pin, EN. An external signal uses this pin to enable or disable the gate driver. When V_{EN} > V_{EN_IH}, the gate driver and charge pump function as outlined in the sections above. When V_{EN} < V_{EN_IL}, the charge pump and gate driver are disabled, causing the SGM25733Q to enter a shutdown state. The EN pin has a specified voltage tolerance ranging from -65V to 65V. When enable function is unnecessary, it can be directly connected to the ANODE pin. When EN pin floats, a 1.9μA internal sink current pulls it to a low level, thus disabling the device.

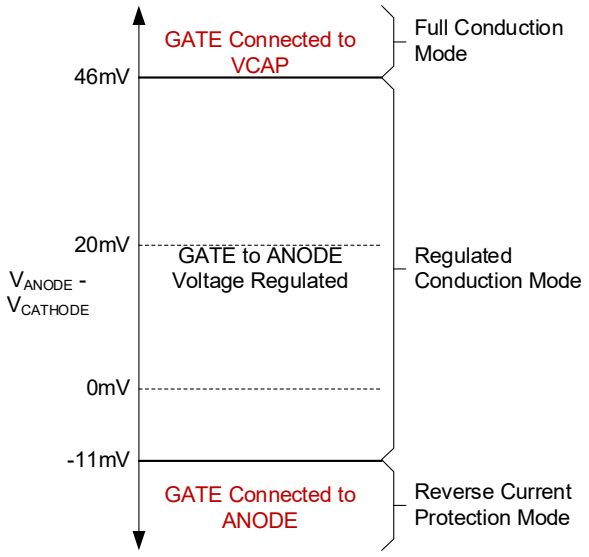


Figure 5. Gate Driver Mode Transitions

DETAILED DESCRIPTION (continued)

Device Functional Modes

Shutdown Mode

When V_{EN} < V_{EN_IL}, the charge pump and gate driver are disabled, causing the SGM25733Q to enter the shutdown mode. During the shutdown mode, the SGM25733Q operates in a low-quiescent-current (low-I_Q) state. Specifically, the ANODE pin only consumes a current of 1.2μA. In shutdown mode, the SGM25733Q does not interrupt forward current flow through the external MOSFET. Instead, the current is conducted through the MOSFET's body diode.

Conduction Mode

When the gate driver is activated, the SGM25733Q enters the conduction mode. In this conduction mode, the device's operation can be divided into three distinct regions, which are determined by the voltage difference between the ANODE and the CATHODE. These three modes are detailed in the sections below.

Regulated Conduction Mode

To allow the SGM25733Q to function in regulated conduction mode, the gate driver should be activated as specified in the *Gate Driver* section. Additionally, the current passing from the source to the drain of the external MOSFET should be in the range that enables the ANODE pin to CATHODE pin voltage drop from -11mV to 46mV. In forward regulation mode, the ANODE-to-CATHODE voltage is controlled at 20mV by adjusting the GATE-to-ANODE voltage. This closed loop regulation mechanism allows the MOSFET to turn off smoothly under extremely light loads and guarantees that no DC reverse current occurs.

Full Conduction Mode

To allow the SGM25733Q to function in full conduction mode, the gate driver should be activated as specified in the *Gate Driver* section. Additionally, the current flowing from the source to the drain of the external MOSFET should be large enough that it causes the ANODE pin to CATHODE pin voltage drop greater than 46mV typical. Once these conditions are met, the GATE pin is internally connected to the VCAP pin. Consequently, the voltage between the GATE and the ANODE approximates that between the VCAP and the ANODE. Connecting the GATE pin to the VCAP pin leads to the minimization of the external MOSFET's R_{DSON}, thereby reducing power loss in the MOSFET during high forward current conditions.

Reverse Current Protection Mode

To allow the SGM25733Q to function in reverse current protection mode, the gate driver should be activated as specified in the *Gate Driver* section. Additionally, the current in the external MOSFET must flow from the drain to the source. When the ANODE-to-CATHODE voltage falls below approximately -11mV, reverse current protection mode is activated, and the GATE pin is internally connected to the ANODE pin. This connection disables the external MOSFET. The flow of reverse current from the drain to the source is interrupted by the body diode integrated within the MOSFET.

APPLICATION INFORMATION

In a typical reverse polarity protection use case, the SGM25733Q is used in conjunction with an NMOS. Figure 6 presents the schematic for the 12V battery protection application. In this setup, the MOSFET is driven by connecting the SGM25733Q and a battery in series.

The SGM25733Q can operate without TVS. However, the TVS devices are applied to limit both positive and negative voltage spikes. Meanwhile, it is advisable to utilize the output capacitor C_{OUT}. This capacitor helps prevent an abrupt drop in the output voltage caused by line disturbances.

Typical Application

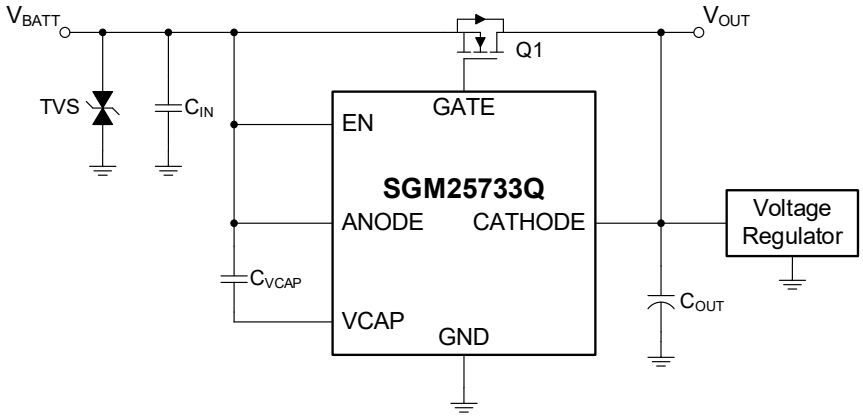


Figure 6. Typical Application Circuit

Design Requirements

A design sample is shown, where the system design parameters are detailed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	12V battery, 12V TYP with 3.2V cold crank and 35V load dump.
Output Voltage	3.2V during cold crank to 35V load dump.
Output Current Range	3A TYP, 5A MAX.
Output Capacitance	1μF MIN, 47μF TYP hold up capacitance
Automotive EMC Compliance	ISO7637-2 and ISO16750-2

Detailed Design Procedure

Design Considerations

- Input operating voltage range, accounting for cold crank and load dump scenarios
- Typical load current and maximum load current requirements

MOSFET Selection

Key MOSFET electrical parameters include the maximum continuous drain current I_D, maximum drain-to-source voltage $V_{DS(MAX)}$, maximum source current through the body diode, and the drain-to-source on-resistance R_{DSON}.

The I_D rating should be higher than the maximum continuous load current, while the $V_{DS(MAX)}$ must be sufficient to handle the highest differential voltage encountered in the application, including any fault conditions that are expected. Considering the anode-cathode maximum voltage of the SGM25733Q is 65V, it's advisable to select MOSFETs with a voltage rating of up to 60V. The SGM25733Q can drive a V_{GS} up to a maximum of 13V. Thus, it is advisable to select a MOSFET with a minimum V_{GS} of 15V. If a MOSFET with a V_{GS} rating of less than 15V is selected, a Zener diode can be employed to clamp the V_{GS} to a safe level.

APPLICATION INFORMATION (continued)

To minimize the conduction losses of the MOSFET, it is preferable to choose a device with the lowest possible R_{DSON}. Nevertheless, choosing a MOSFET merely because of its low R_{DSON} might not consistently lead to favorable results. A higher R_{DSON} value offers enhanced voltage information to the reverse comparator of the SGM25733Q even at a relatively low reverse current. This means that reverse current detection becomes more effective when the R_{DSON} is increased. Under nominal load conditions, it is suggested to operate the MOSFET in the regulated conduction mode. When selecting the MOSFET, the R_{DSON} should be chosen in such a way that, at the nominal operating current, the forward voltage drop V_{DS} is close to the 20mV regulation point and does not exceed 46mV.

As a practical guideline, it is proposed that the selection of the MOSFET should follow the criterion where the R_{DSON} satisfies the inequality (20mV / $I_{LOAD(TYP)}$) ≤ R_{DSON} ≤ (46mV / $I_{LOAD(TYP)}$). Typically, MOSFET manufacturers provide the specification of R_{DSON} at V_{GS} values of 4.5V and 10V. The R_{DSON} increases significantly when V_{GS} is below 4.5V, and it reaches its maximum value when V_{GS} is close to the MOSFET's threshold voltage V_{TH}. To ensure stable regulation under light load conditions, it is recommended to operate the MOSFET with a V_{GS} close to 4.5V, which is considerably higher than the MOSFET's gate threshold voltage. It is also suggested to choose a MOSFET with a maximum gate threshold voltage V_{TH} in the range of 2V to 2.5V. Selecting a MOSFET with a lower can also shorten the turn-on time.

According to the design requirements, the recommended MOSFET ratings are:

- 60V $V_{DS(MAX)}$ and ±20V $V_{GS(MAX)}$
- R_{DSON} (at 3A TYP): (20mV / 3A =) 6.67mΩ to (46mV / 3A =) 15.33mΩ
- MOSFET V_{TH}: 2V (MAX)

In order to meet the requirements of this 12V reverse battery protection design, the DMT6007LFG MOSFET from Diodes Inc. is chosen, and it is rated as:

- 60V $V_{DS(MAX)}$ and ±20V $V_{GS(MAX)}$
- R_{DSON}: 6.5mΩ (TYP) and 8.5mΩ (MAX) rated at 4.5V V_{GS}
- MOSFET V_{TH}: 2V (MAX)

To maintain safe operational conditions, the MOSFET's thermal resistance must be evaluated in relation to its anticipated maximum power dissipation, guaranteeing that the junction temperature (T_J) remains within prescribed limits.

Charge Pump C_{VCAP}, Input and Output Capacitance

The minimum required capacitance values for the charge pump are as follows:

- C_{VCAP}: A minimum of 0.1μF is required, with a recommended value of C_{VCAP} (μF) ≥ 10 × C_{ISS_MOSFET} (μF).
- C_{IN}: A minimum of 22nF for input capacitance.
- C_{OUT}: A minimum of 100nF for output capacitance.

APPLICATION INFORMATION (continued)

Selection of TVS Diodes for 12V Battery Protection Applications

In automotive electrical systems, transient voltage suppression devices play a critical role in safeguarding circuits. For the 12V battery protection application circuit presented in Figure 7, a bi-directional TVS diode is used. It defends against transient voltage spikes in both the positive and negative polarities that happen when the car is running normally. The levels and pulses of these transient voltages are defined by the ISO7637-2 and ISO16750-2 standards.

Two key parameters of the TVS are its breakdown voltage and clamping voltage. The breakdown voltage is the voltage at which the TVS diode initiates an avalanche effect, similar to that of a Zener diode. It is specified under a low current condition, usually 1mA. The breakdown voltage must surpass the steady-state voltages encountered in the system under the worst case scenarios. The breakdown voltage of TVS+ is required to be greater than the 24V jump start voltage as well as the 35V suppressed load dump voltage, and it should be lower than the 65V maximum ratings of SGM25733Q. To safeguard against damage due to extended reverse-battery exposure, the breakdown voltage of TVS- should lower than the maximum reverse battery voltage of -16V.

The clamping voltage refers to the stabilized potential a TVS maintains during high-energy surge events, significantly exceeding its nominal breakdown threshold. TVS diodes are designed to suppress transient pulses without affecting the normal steady state operation of the circuit. Under the conditions of ISO7637-2 pulse 1, the input voltage can reach -150V, with the generator having an impedance of 10Ω. As a result, a current of 15A passes through the TVS-, and the voltage across the TVS will be approximately equal to its clamping voltage.

An additional design constraint is to avoid exceeding the SGM25733Q's maximum reverse voltage limit from anode to cathode (-75V) as well as the MOSFET's V_{DS} rating. In the design example, a MOSFET rated for 60V is selected, and the maximum allowable cathode to anode voltage is set at 60V.

Under ISO7637-2 Pulse 1 conditions, the anode of the SGM25733Q is driven low by the transient pulse and clamped by the TVS diode. To stop the bulk output capacitors from being discharged by reverse current, the MOSFET is rapidly shut off. When the MOSFET turns off, the voltage across the cathode to anode becomes the sum of the TVS clamping voltage and the output capacitor voltage. Given that the output capacitor voltage can rise to 16V (the maximum battery voltage), the TVS clamping voltage must stay below (60V - 16V) = 44V to remain within the system's voltage rating.

The SMBJ33CA TVS diode is suitable for 12V battery protection applications. Its breakdown voltage of 36.7V satisfies the requirements of jump start and load dump on the positive side, as well as for a 16V reverse battery connection on the negative side. During the ISO7637-2 Pulse 1 test, with a peak surge current of 15A, the SMBJ33CA exhibits a clamping voltage of -44V, as illustrated in Figure 7. This clamping voltage complies with the requirement of being ≤ 44V.

The SMBJ series of TVS diodes have a rating of up to 600W peak pulse power levels. This power rating is adequate to handle the pulses specified in ISO7637-2 and the suppressed load dump pulses as per ISO16750-2 pulse B.

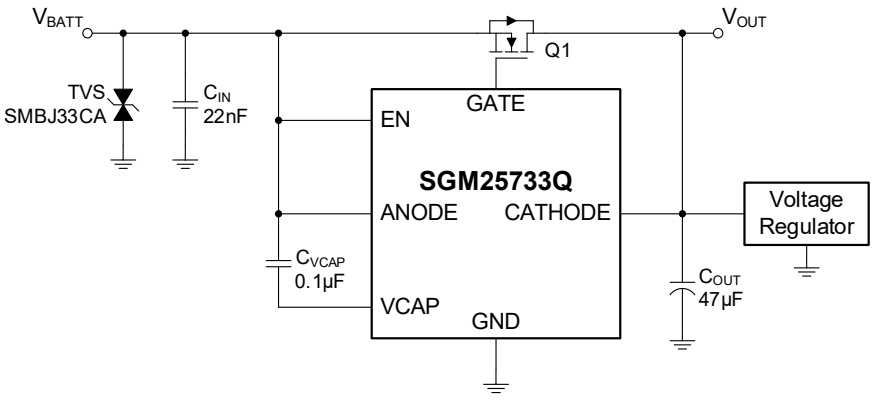


Figure 7. Single Bi-Directional TVS, 12V (TYP) Battery Protection

APPLICATION INFORMATION (continued)

Selection of TVS Diodes and MOSFET for 24V Battery Protection Applications

In a standard 24V battery protection circuit, as depicted in Figure 8, two uni-directional TVS diodes are employed to safeguard against both positive and negative transient voltage spikes. For the TVS+ diode, its breakdown voltage must exceed the 48V jump start voltage. Simultaneously, it should not exceed the absolute maximum ratings of the anode and enable pin of the SGM25733Q, which is 65V. Additionally, it needs to endure the 65V suppressed load dump. Regarding the TVS diode, its breakdown voltage should be lower than the maximum reverse battery voltage of -32V. This ensures that the TVS- is not damaged during prolonged exposure to a reverse-connected battery.

During the ISO7637-2 Pulse 1 event, the input voltage reaches to -600V with a 50Ω generator impedance, causing 12A to flow through the TVS-. The clamping voltage of the TVS- in this scenario differs from that of the 12V battery protection setup. Since during the ISO7637-2 pulse, the ANODE-to-CATHODE voltage observed is equal to the sum of the negative TVS clamping voltage and the output capacitor voltage. In a 24V battery application, where the maximum battery voltage amounts to 32V, the clamping voltage of the TVS- must not be more than 75V - 32V, equating to 43V.

A single bi-directional TVS diode is unsuitable for 24V battery protection due to the conflicting requirements for the breakdown voltage and clamping voltage. Specifically, the TVS+ requires a breakdown voltage of at least 65V, while the maximum clamping voltage must not exceed 43V, which is impossible since the clamping voltage cannot be lower than the breakdown voltage. Therefore, two uni-directional TVS diodes connected in a back-to-back configuration are necessary at the input. For the positive side TVS+, the SMBJ58A is suggested, featuring a minimum breakdown voltage of 64.4V and a typical value of 67.8V. For the negative side TVS-, the SMBJ26A is recommended, as it offers a breakdown voltage near 32V (to tolerate the maximum reverse battery voltage of -32V) and a maximum clamping voltage of 42.1V.

In the case of 24V battery protection, it is suggested to employ a MOSFET with a 75V rating. Additionally, at the input, the SMBJ26A and SMBJ58A, connected back-to-back, are to be utilized.

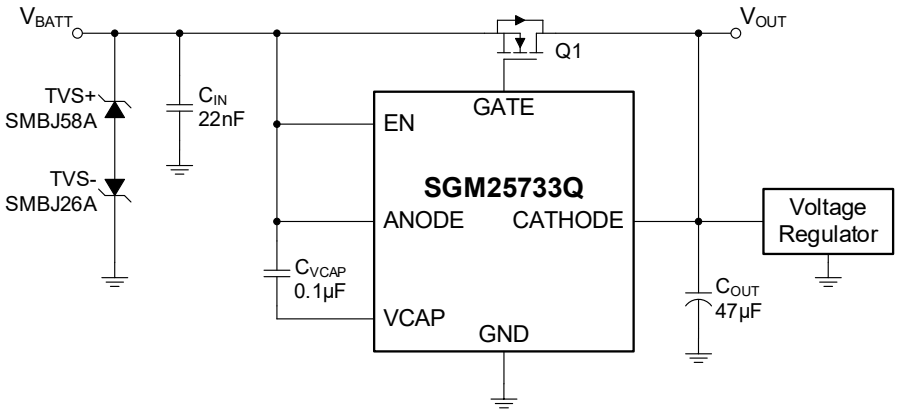


Figure 8. Two Uni-Directional TVS, 24V (TYP) Battery Protection

APPLICATION INFORMATION (continued)

ORing Application Configuration

A fundamental redundant power architecture consists of two or more voltage or power supply sources that power a single load. In its most elementary configuration, the ORing approach for redundant power supplies is constituted by Schottky ORing diodes. These diodes serve to defend the system from situations where the input power supply malfunctions. While diode ORing solution offers an efficient and cost-effective solution with minimal components, the forward voltage drop across the diodes leads to permanent efficiency losses. This is because each diode in an ORing setup primarily operates in forward conduction mode, resulting in continuous power dissipation. These power dissipations enhance the specifications for heat management and expand the required footprint on the printed circuit board.

As depicted in Figure 9, the SGM25733Q ICs, along with external NMOSs, can be utilized within an ORing Solution. During normal operation, the external NMOS turns on, minimizing the forward diode drop. The SGM25733Q is capable of quickly detecting reverse current. Upon detecting reverse current, it rapidly pulls down the gate of the MOSFET. This mechanism allows the body diode of the MOSFET to prevent the reverse current from passing through. To ensure an efficient ORing solution, rapid response is critical to minimize both the magnitude and duration of reverse current. In the ORing configuration, the SGM25733Q constantly monitors the voltage disparity between its ANODE and CATHODE pins. The ANODE pin represents the voltage at the power sources (V_{IN1}, V_{IN2}), while the CATHODE pin represents the voltage at the shared load point. The SGM25733Q uses its ANODE and CATHODE pins to sense the source to drain voltage V_{DS} of each MOSFET. When the voltage difference V_{IN} - V_{OUT} drops below -11mV, a high speed comparator quickly disables the gate drive by pulling it down within 0.44μs (TYP). Conversely, when the forward voltage differential V_{IN} - V_{OUT} exceeds 46mV, the GATE is activated with an 11mA gate charge current.

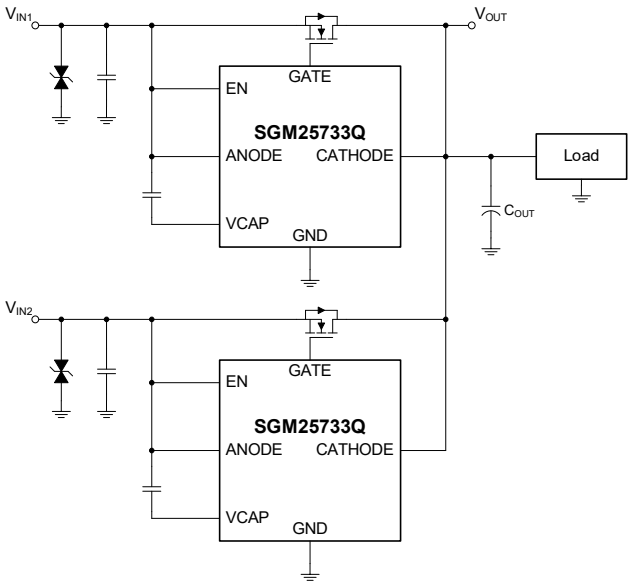


Figure 9. Typical ORing Application

APPLICATION INFORMATION (continued)

Power Supply Recommendations

The SGM25733Q ideal diode controller is designed to operate within a supply voltage range of 3.2V to 65V. When the input supply is situated several inches or more away from the device, it's best to employ an input ceramic bypass capacitor with a capacitance greater than 22nF. To avoid damage to the SGM25733Q and its surrounding components in the event of a direct output short circuit, a power supply offering overload and short circuit protection is essential.

Layout Guidelines

- Connect the ANODE, GATE, and CATHODE pins of SGM25733Q near the corresponding SOURCE, GATE, and DRAIN pins of the MOSFET.
- Ensure the source and drain traces of the MOSFET are wide enough to handle the high current flow and reduce resistive losses.
- Keep the charge pump capacitor between VCAP and ANODE pins away from the MOSFET to minimize thermal impact on its capacitance.
- Use a short and robust trace to connect the SGM25733Q's GATE pin to the MOSFET gate, avoiding thin or lengthy traces.
- Place the GATE pin as close as possible to the MOSFET to reduce turn-off delays resulting from trace resistance.
- Acceptable results can be obtained with different layout designs, but the layout in Figure 10 is a recommended approach for achieving good performance.

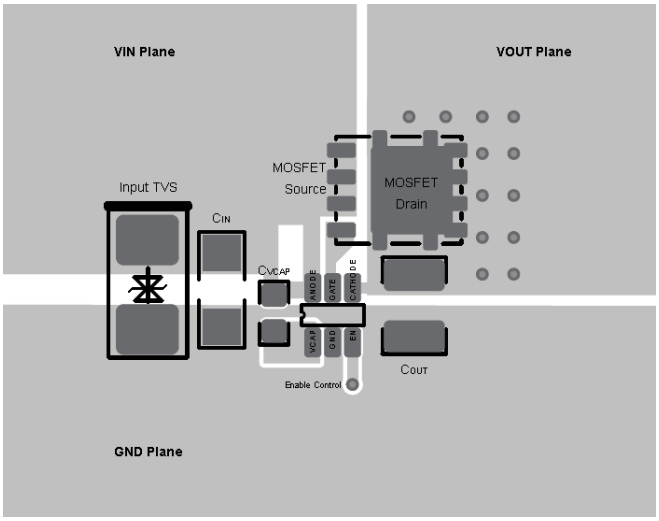


Figure 10. SOT-23-6 Layout Example

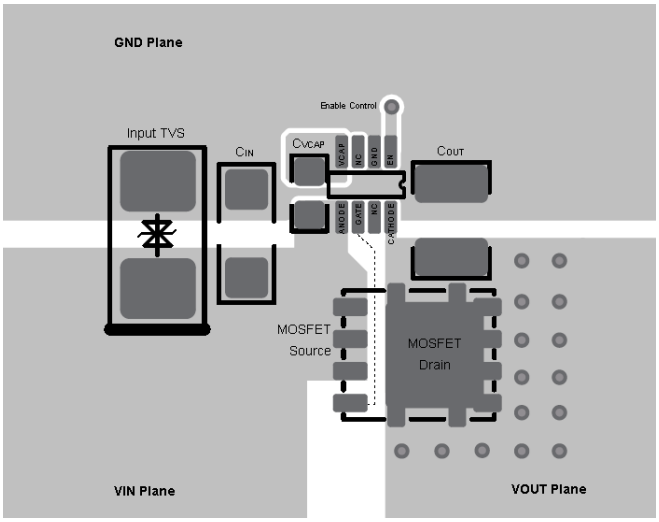


Figure 11. TSOT-23-8 Layout Example

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

JANUARY 2026 – REV.A.2 to REV.A.3	Page
Updated Detailed Description	13

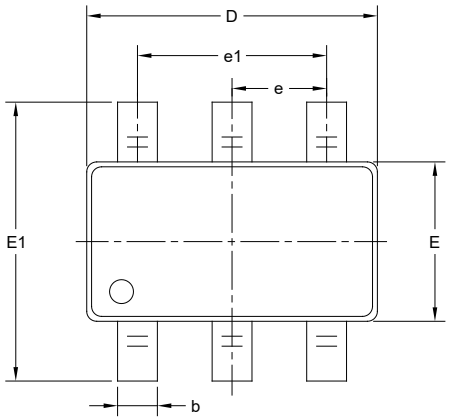
NOVEMBER 2025 – REV.A.1 to REV.A.2	Page
Added TSOT-23-8 Package	1, 2, 3, 21

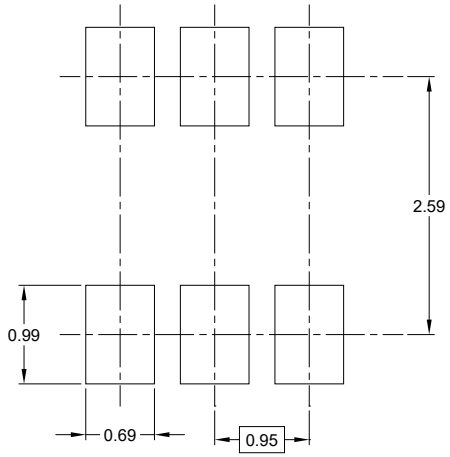
JULY 2025 – REV.A to REV.A.1	Page
Updated Application Information	20

Changes from Original (MAY 2025) to REV.A	Page
Changed from product preview to production data	All

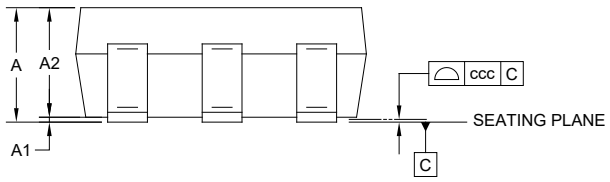
PACKAGE OUTLINE DIMENSIONS

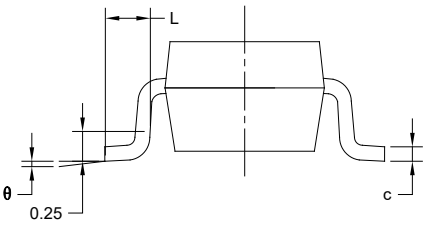
SOT-23-6





RECOMMENDED LAND PATTERN (Unit: mm)



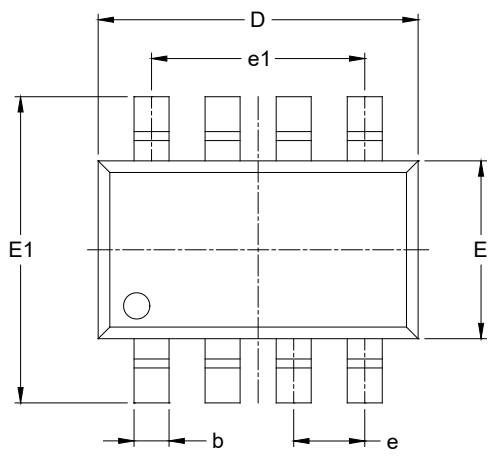


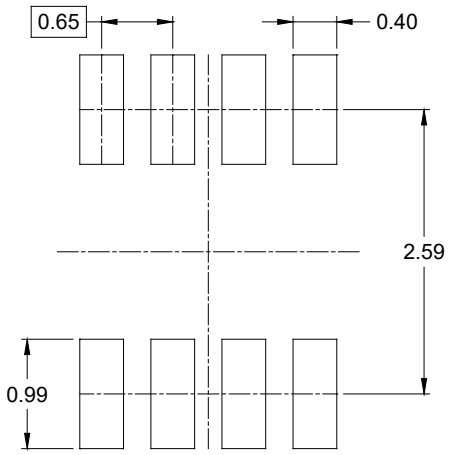
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.450
A1	0.000	-	0.150
A2	0.900	-	1.300
b	0.300	-	0.500
c	0.080	-	0.220
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
e1	1.900 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-178.

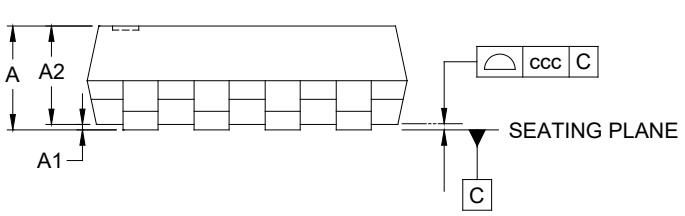
PACKAGE OUTLINE DIMENSIONS

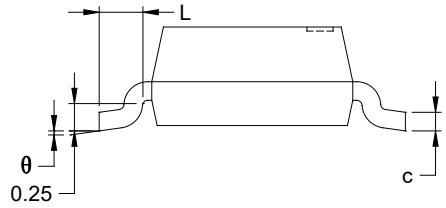
TSOT-23-8





RECOMMENDED LAND PATTERN (Unit: mm)



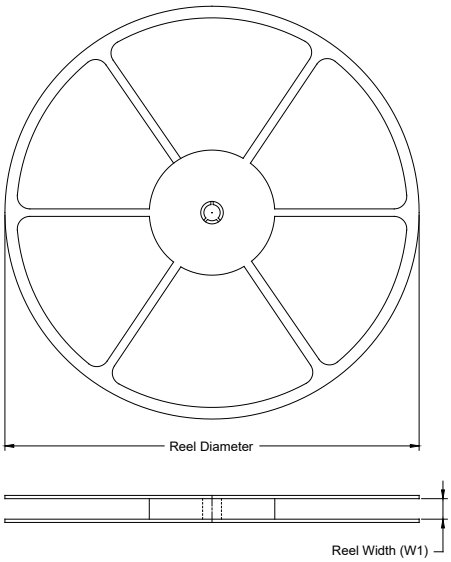


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.100
A1	0.000	-	0.100
A2	0.700		1.000
b	0.220	-	0.380
c	0.080		0.200
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.550	-	3.050
e	0.650 BSC		
e1	1.950 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

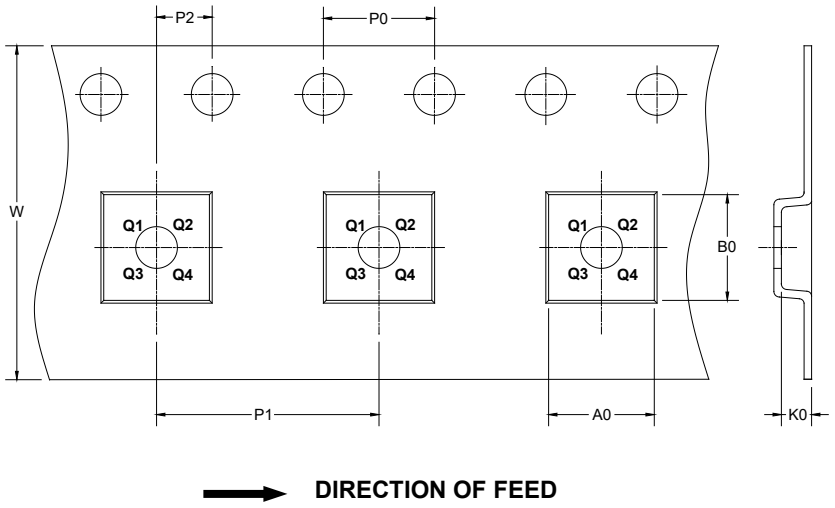
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-193.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



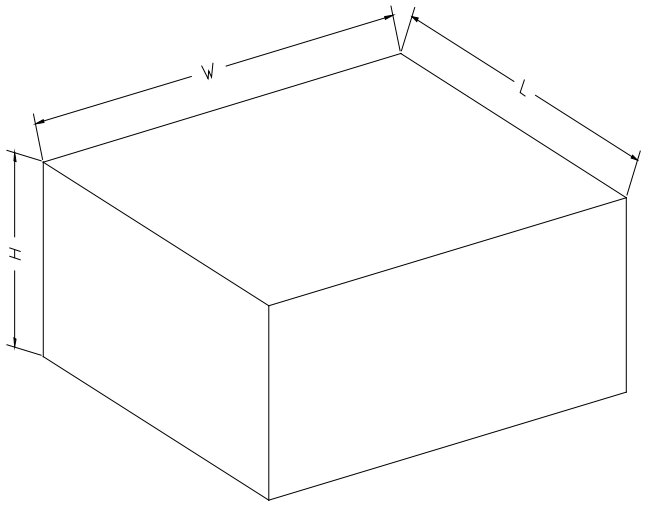
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-6	7"	9.5	3.23	3.17	1.37	4.0	4.0	2.0	8.0	Q3
TSOT-23-8	7"	9.5	3.20	3.10	1.10	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002