

INN700D130E

700V GaN Enhancement-mode Power Transistor

INN700D130E

1. General description

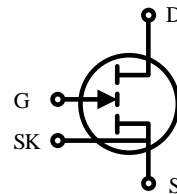
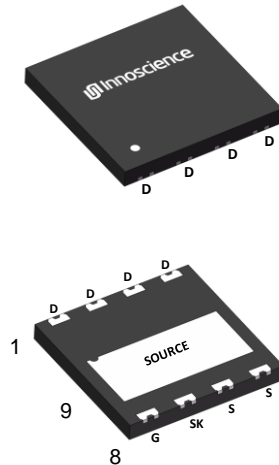
700V, 101mΩ typ., GaN-on-Silicon Enhancement-mode Power Transistor in Dual Flat No-lead package (DFN) with 8 mm × 8 mm size

2. Features

- Enhancement mode transistor-Normally off power switch
- Ultra high switching frequency
- No reverse-recovery charge
- Low gate charge, low output charge
- Qualified for industrial applications according to JEDEC Standards
- ESD safeguard
- RoHS, Pb-free, REACH-compliant

3. Applications

- AC-DC converters
- DC-DC converters
- Totem pole PFC
- Fast battery charging
- High density power conversion
- High efficiency power conversion



4. Key performance parameters

Table 1 Key performance parameters at $T_j = 25\text{ }^\circ\text{C}$

Parameter	Value	Unit
$V_{DS,max}$	700	V
$R_{DS(on),typ.} @ V_{GS} = 6\text{ V}$	101	mΩ
$R_{DS(on),max} @ V_{GS} = 6\text{ V}$	130	mΩ
$Q_{G,typ} @ V_{DS} = 400\text{ V}$	2.65	nC
$I_{D,pulse}$	32	A
$Q_{OSS} @ V_{DS} = 400\text{ V}$	25.5	nC
$Q_{rr} @ V_{DS} = 400\text{ V}$	0	nC

5. Pin information

Table 2 Pin information

Gate	Drain	Kelvin Source	Source
8	1, 2, 3, 4	7	5, 6, 9

Table 3 Ordering information

Type/Ordering Code	Package	Product Code	Carrier	Package base Qty.
INN700D130E	DFN 8X8	70D130E	Tape & Reel	2500

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6. Maximum ratings

at $T_j = 25\text{ °C}$ unless otherwise specified.

Exceeding the maximum ratings may destroy the device. For further information, contact Innoscience sales office.

Table 4 Maximum ratings

Parameter	Symbol	Values	Unit	Note/Test Condition
Drain source voltage	$V_{DS, max}$	700	V	$V_{GS} = 0\text{ V}$, $T_j = -55\text{ °C}$ to 150 °C
Drain source voltage transient ¹	$V_{DS, transient}$	800	V	$V_{GS} = 0\text{ V}$
Drain source voltage, pulsed ²	$V_{DS, pulse}$	750	V	$T_j = 25\text{ °C}$; total time < 10 h
				$T_j = 125\text{ °C}$; total time < 1 h
Continuous current, drain source ³	I_D	16	A	$T_c = 25\text{ °C}$
Pulsed current, drain source ⁴	$I_{D, pulse}$	32	A	$T_c = 25\text{ °C}$; $V_{GS} = 6\text{ V}$; $t_{PULSE} = 10\text{ }\mu\text{s}$
Pulsed current, drain source ⁴	$I_{D, pulse}$	18	A	$T_c = 125\text{ °C}$; $V_{GS} = 6\text{ V}$; $t_{PULSE} = 10\text{ }\mu\text{s}$
Gate source voltage, continuous	V_{GS}	-6 to +7	V	$T_j = -55\text{ °C}$ to 150 °C
Gate source voltage, pulsed	$V_{GS, pulse}$	-20 to +10	V	$T_j = -55\text{ °C}$ to 150 °C ; $f = 100\text{ kHz}$; open drain, $t_{PULSE} = 50\text{ ns}$, total time<50s
Power dissipation	P_{tot}	84	W	$T_c = 25\text{ °C}$
Operating temperature	T_j	-55 to +150	°C	
Storage temperature	T_{stg}	-55 to +150	°C	

1. $V_{DS, transient}$ is intended for non-repetitive events, $t_{PULSE} < 200\text{ }\mu\text{s}$.

2. $V_{DS, pulse}$ is intended for repetitive pulse, $t_{PULSE} < 100\text{ ns}$.

3. Limited by maximum temperature allowed with the parts assembled in DFN8X8 package.

4. Limit was extracted from characterization test, not measured during production.

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7. Thermal characteristics

Table 5 Thermal characteristics

Parameter	Symbol	Values	Unit	Note/Test Condition
Thermal resistance, junction-ambient	R_{thJA} ¹	63.4	°C/W	
Thermal resistance, junction-case	R_{thJC}	1.46	°C/W	
Maximum reflow soldering temperature	T_{sold}	260	°C	MSL3

1. R_{thJA} is determined with the device mounted on one square inch of copper pad, single layer 2oz copper on FR4 board.

8. Electric characteristics

at $T_j = 25\text{ °C}$, unless specified otherwise

Table 6 Static characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	1.2	1.6	2.5	V	$I_D = 14.3\text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 25\text{ °C}$
		-	1.5	-		$I_D = 14.3\text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 125\text{ °C}$
Drain-source leakage current	I_{DSS}	-	0.6	37.5	μA	$V_{DS} = 700\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$
		-	4	-		$V_{DS} = 700\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	40	-	μA	$V_{GS} = 6\text{ V}$; $V_{DS} = 0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	101	130	$\text{m}\Omega$	$V_{GS} = 6\text{ V}$; $I_D = 0.5\text{ A}$; $T_j = 25\text{ °C}$
		-	101	-	$\text{m}\Omega$	$V_{GS} = 6\text{ V}$; $I_D = 5\text{ A}$; $T_j = 25\text{ °C}$
		-	203	-	$\text{m}\Omega$	$V_{GS} = 6\text{ V}$; $I_D = 5\text{ A}$; $T_j = 125\text{ °C}$
Gate resistance	R_G	-	7	-	Ω	$f = 5\text{ MHz}$; open drain

Table 7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	101	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; $f = 100\text{ kHz}$
Output capacitance	C_{oss}	-	36.5	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; $f = 100\text{ kHz}$
Reverse transfer Capacitance	C_{rss}	-	0.4	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; $f = 100\text{ kHz}$
Effective output capacitance, energy related ¹	$C_{o(er)}$	-	49	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 0\text{ to }400\text{ V}$
Effective output capacitance, time related ²	$C_{o(tr)}$	-	65	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 0\text{ to }400\text{ V}$
Output charge	Q_{oss}	-	25.5	-	nC	$V_{GS} = 0\text{ V}$; $V_{DS} = 0\text{ to }400\text{ V}$

1. $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V.

2. $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400 V.

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Table 8 Gate charge characteristics

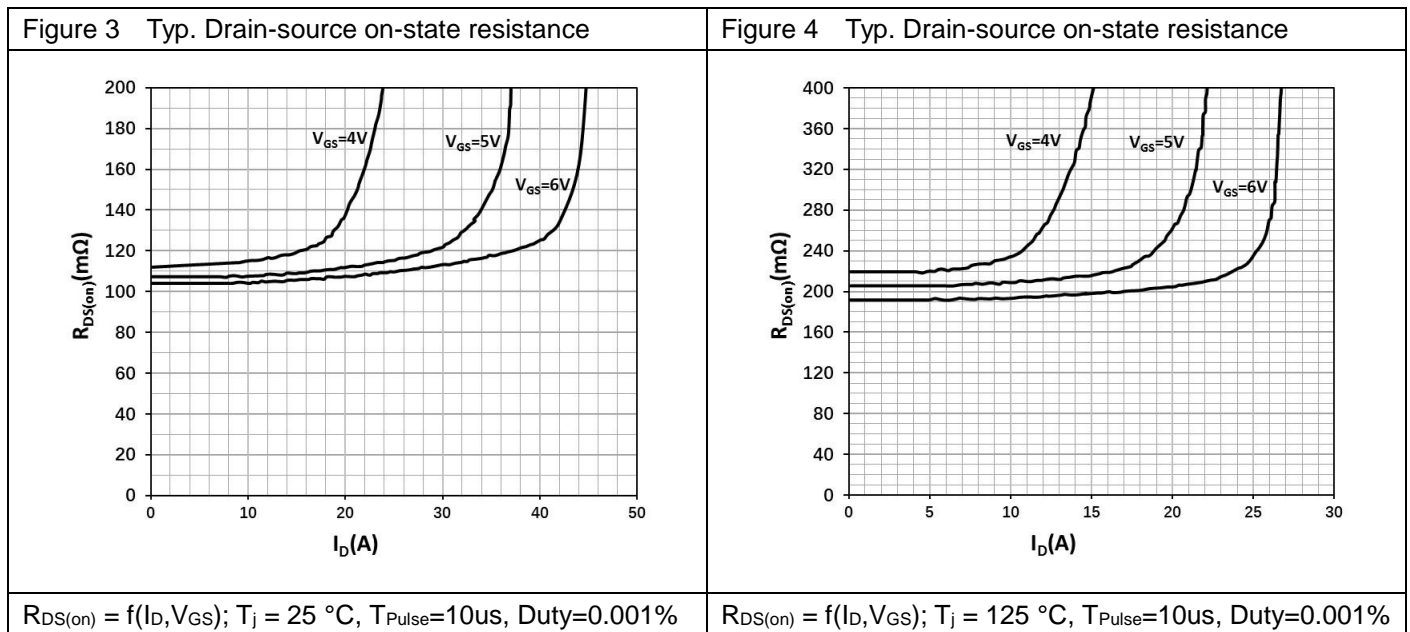
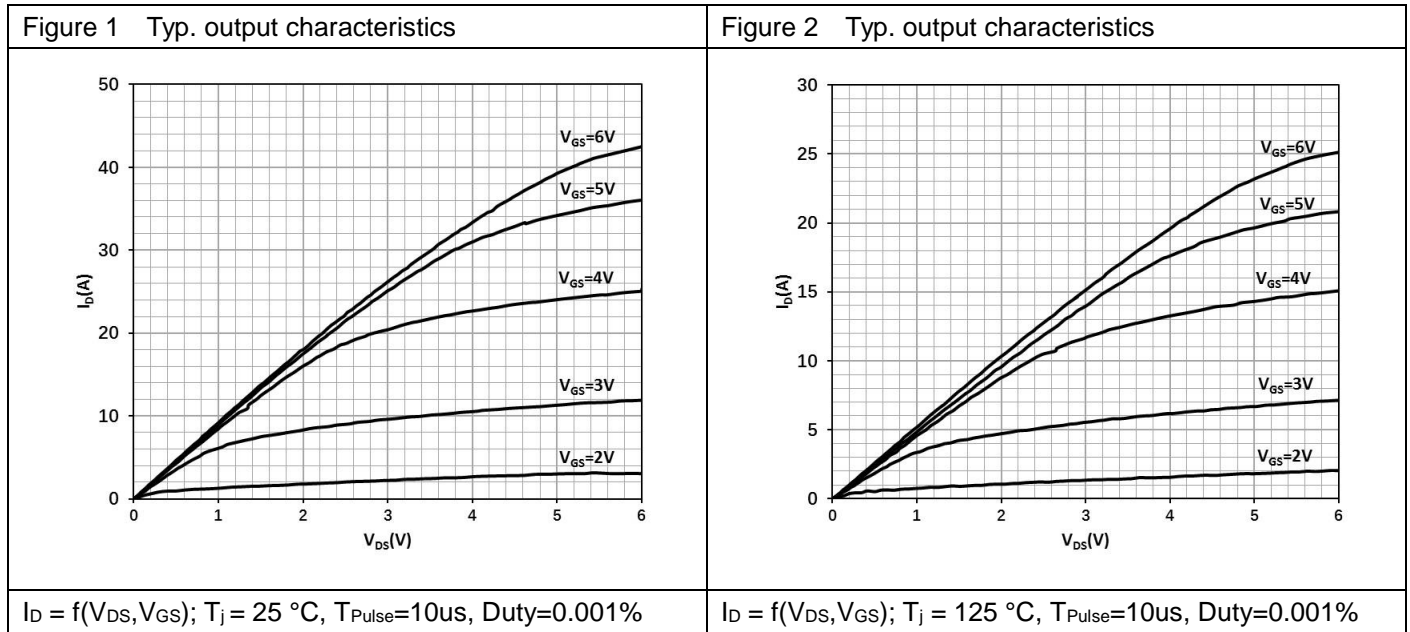
Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate charge	Q_G	-	2.65	-	nC	$V_{GS} = 0$ to 6 V; $V_{DS} = 400$ V; $I_D = 5$ A
Gate-source charge	Q_{GS}	-	0.22	-	nC	
Gate-drain charge	Q_{GD}	-	1.02	-	nC	
Gate Plateau Voltage	V_{Plat}	-	2.1	-	V	$V_{DS} = 400$ V; $I_D = 5$ A

Table 9 Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	V_{SD}	-	2.4	-	V	$V_{GS} = 0$ V; $I_S = 5$ A
Pulsed current, reverse	$I_{S, pulse}$	-	-	32	A	$V_{GS} = 6$ V; $t_{PULSE} = 10$ μ s
Reverse recovery charge	Q_{rr}	-	0	-	nC	$I_S = 5$ A; $V_{DS} = 400$ V
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

9. Electric characteristics diagrams

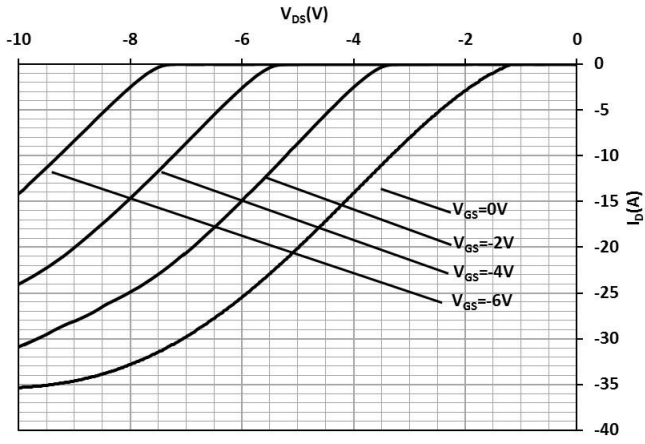
at $T_j = 25\text{ }^\circ\text{C}$, unless specified otherwise



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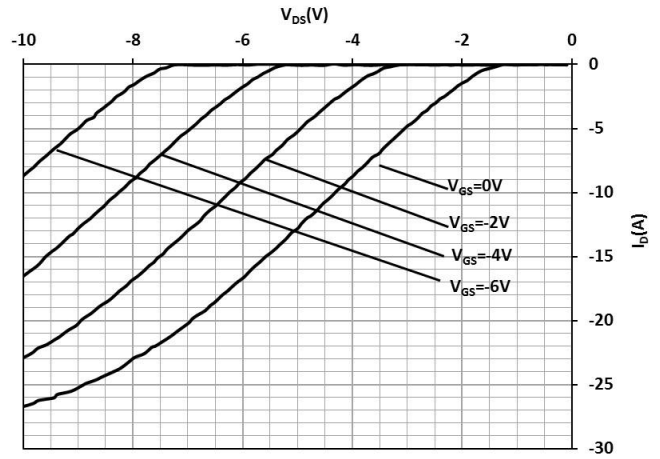
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Figure 5 Typ. channel reverse characteristics



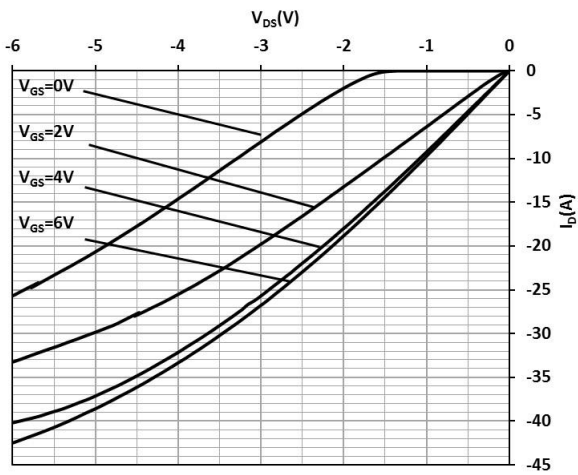
$I_D = f(V_{DS}, V_{GS}); T_j = 25\text{ °C}, T_{Pulse} = 10\mu s, Duty = 0.001\%$

Figure 6 Typ. channel reverse characteristics



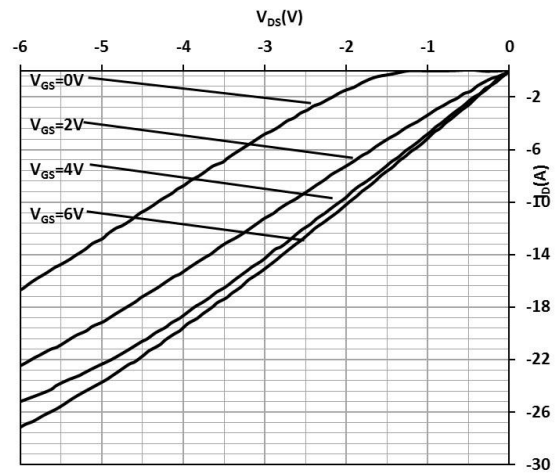
$I_D = f(V_{DS}, V_{GS}); T_j = 125\text{ °C}, T_{Pulse} = 10\mu s, Duty = 0.001\%$

Figure 7 Typ. channel reverse characteristics



$I_D = f(V_{DS}, V_{GS}); T_j = 25\text{ °C}, T_{Pulse} = 10\mu s, Duty = 0.001\%$

Figure 8 Typ. channel reverse characteristics

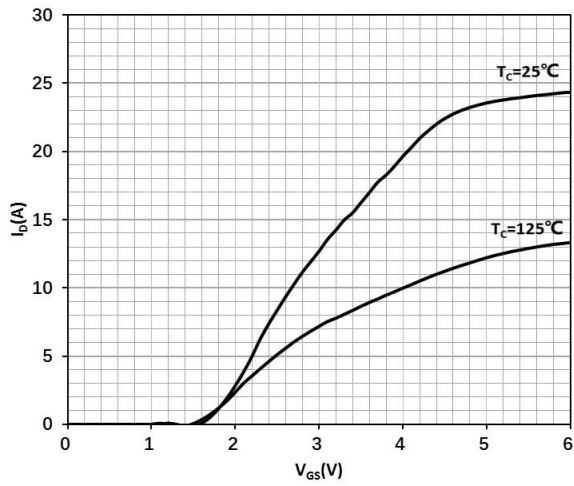


$I_D = f(V_{DS}, V_{GS}); T_j = 125\text{ °C}, T_{Pulse} = 10\mu s, Duty = 0.001\%$

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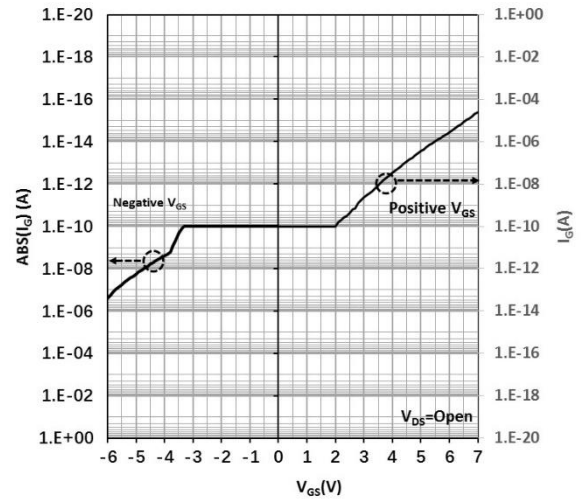
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Figure 9 Typ. transfer characteristics



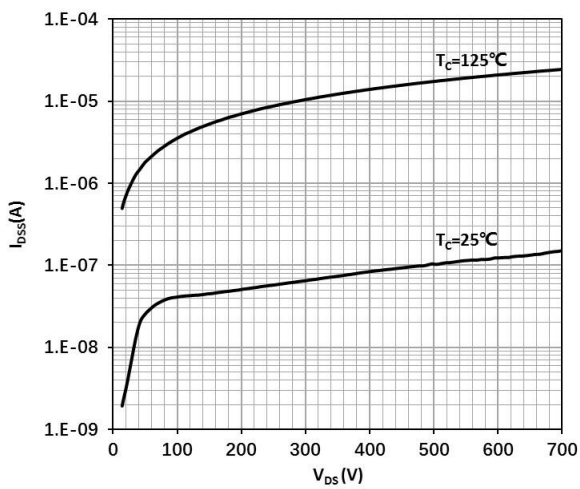
$I_D = f(V_{GS})$; $V_{DS} = 3\text{ V}$, $T_{Pulse} = 10\mu\text{s}$, $Duty = 0.001\%$

Figure 10 Typ. Gate-to-Source leakage



$I_G = f(V_{GS})$; test resolution limit 0.1nA

Figure 11 Drain-source leakage characteristics

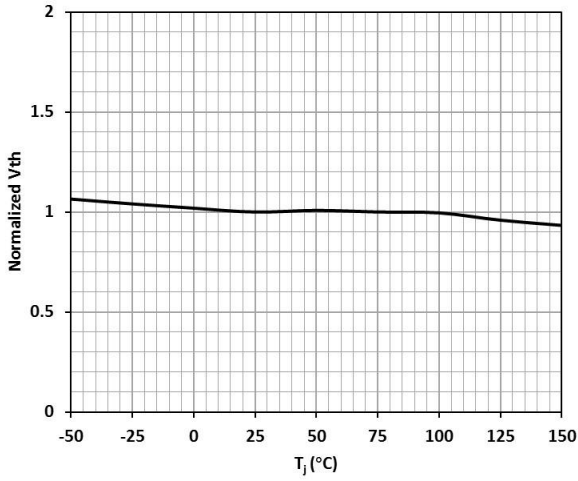


$I_{DSS} = f(V_{DS})$; $V_{GS} = 0\text{ V}$

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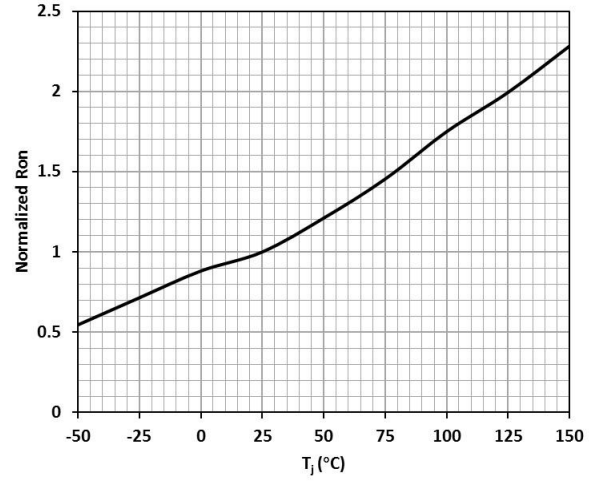
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Figure 12 Gate threshold voltage



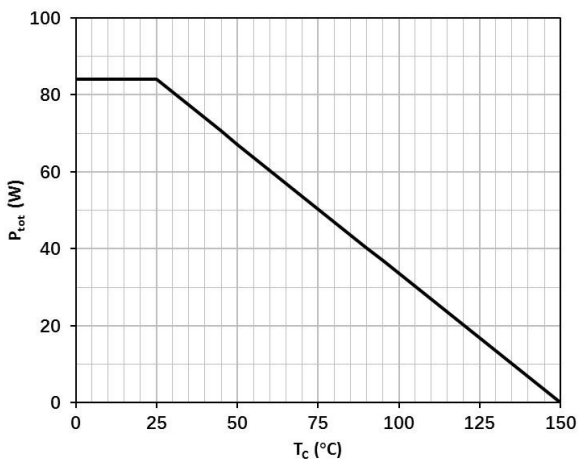
$V_{TH} = f(T_j)$; $V_{GS} = V_{DS}$; $I_D = 14.3\text{mA}$

Figure 13 Drain-source on-state resistance



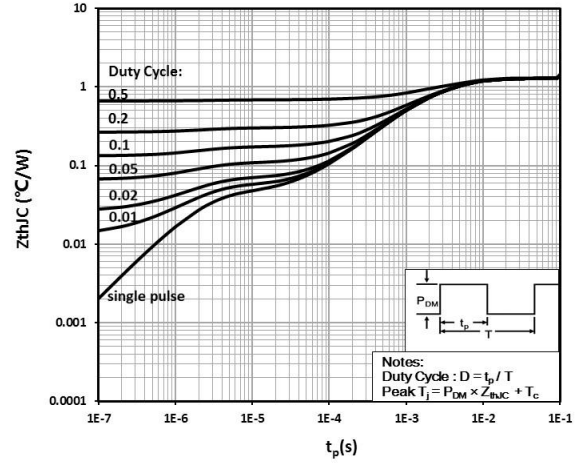
$R_{DS(on)} = f(T_j)$; $I_D = 5\text{ A}$; $V_{GS}=6\text{V}$, Duty=0.001%

Figure 14 Power dissipation



$P_{tot} = f(T_c)$

Figure 15 Max.transient thermal impedance

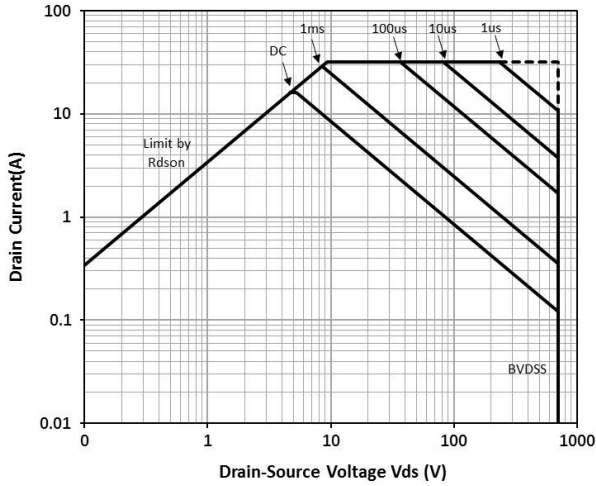


$Z_{thJC} = f(t_p, D)$

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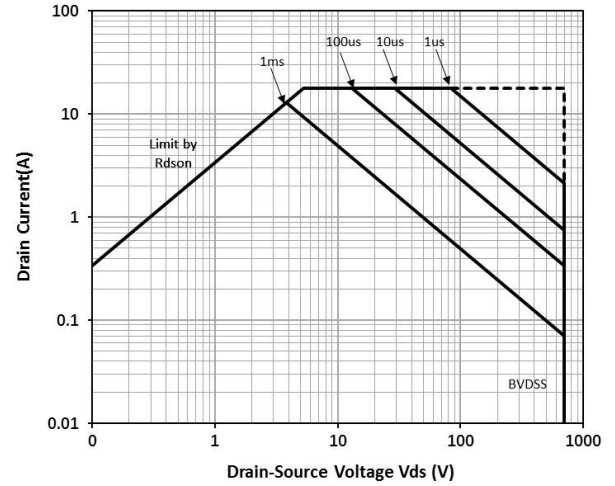
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Figure 16 Safe operating area



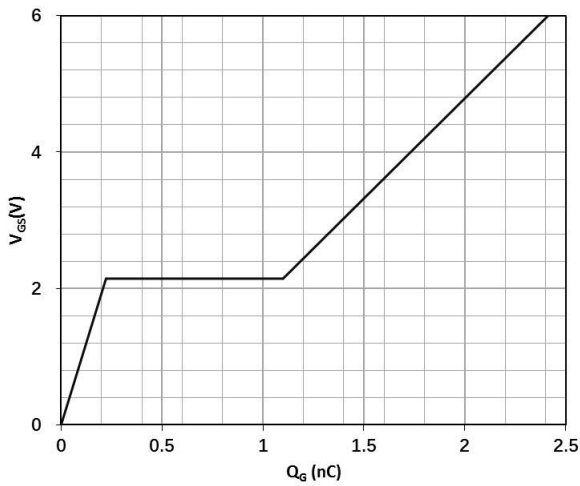
$I_D = f(V_{DS}); T_C = 25\text{ °C}, \text{Duty}=0$

Figure 17 Safe operating area



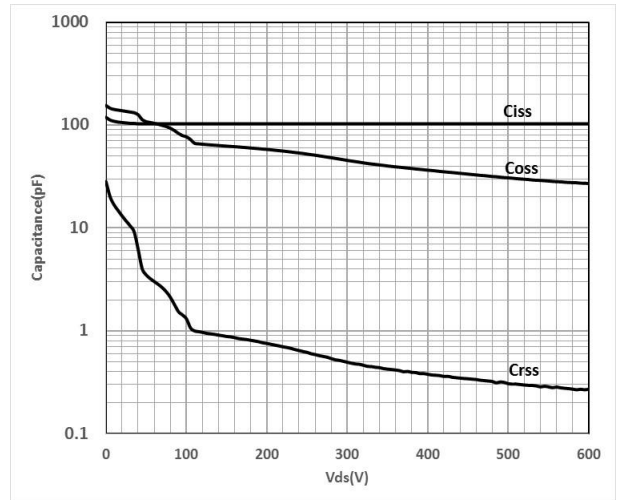
$I_D = f(V_{DS}); T_C = 125\text{ °C}, \text{Duty}=0$

Figure 18 Typ. gate charge



$V_{GS} = f(Q_G); V_{DCLINK} = 400\text{ V}; I_D = 5\text{ A}$

Figure 19 Typ. capacitances

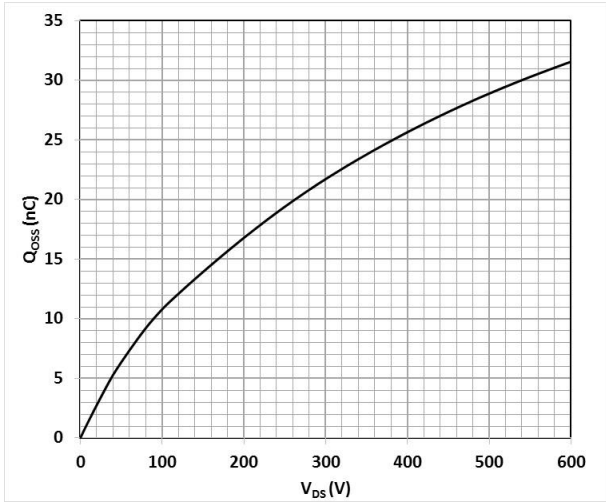


$C_{XSS} = f(V_{DS}); \text{Freq.} = 100\text{ kHz}$

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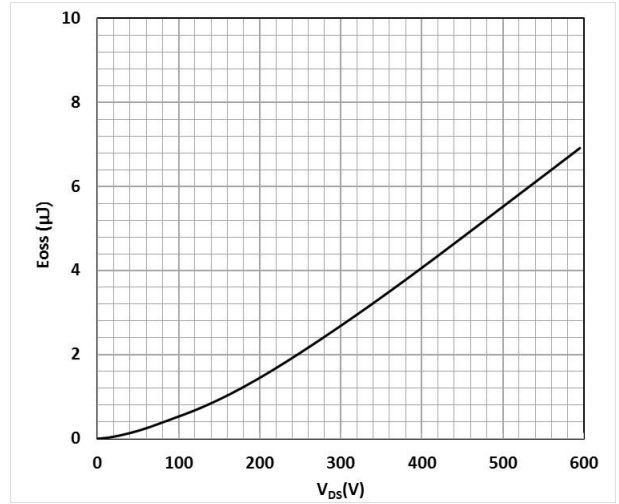
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Figure 20 Typ. output charge



$Q_{oss} = f(V_{DS}); \text{Freq.} = 100 \text{ kHz}$

Figure 21 Typ. C_{oss} stored Energy

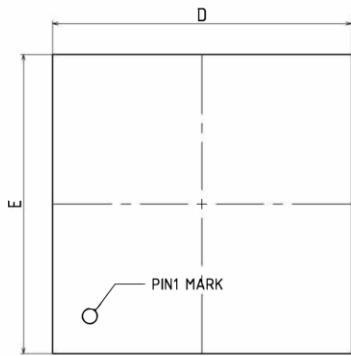


$E_{oss} = f(V_{DS}); \text{Freq.} = 100 \text{ kHz}$

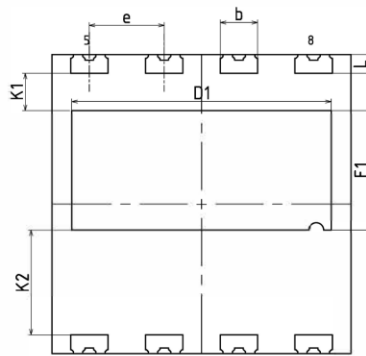
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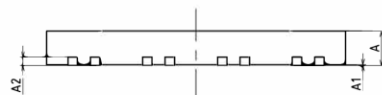
10. Package outlines



top view

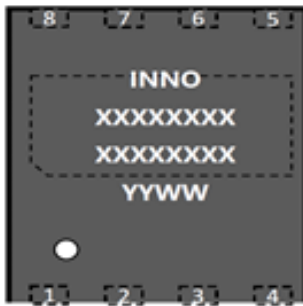


Bottom view



side view

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2	0.203REF		
b	0.95	1.00	1.05
D	7.90	8.00	8.10
D1	6.84	6.94	7.04
E	7.90	8.00	8.10
E1	3.10	3.20	3.30
K1	0.90	1.00	1.10
K2	2.70	2.80	2.90
e	2.00 BSC		
L	0.40	0.50	0.60

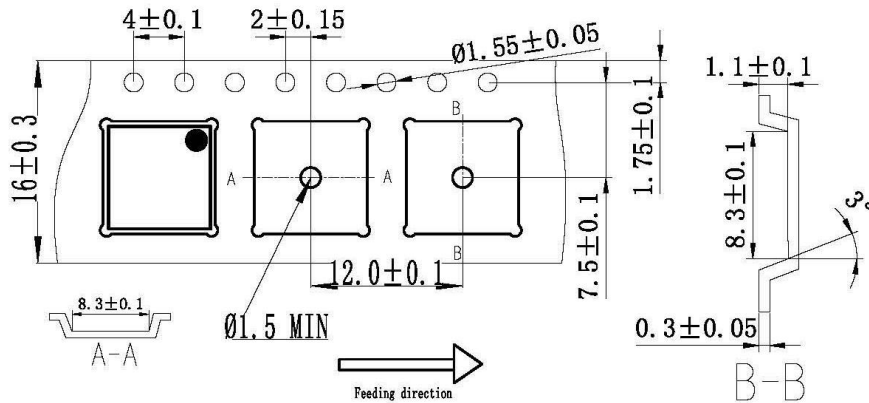


Row	Description	Example
Row1	Company name	INNO
Row2	Product code (In short)	XXXXXXXX
Row3	ASSY lot No.	XXXXXXXX
Row4	Date code	YYWW

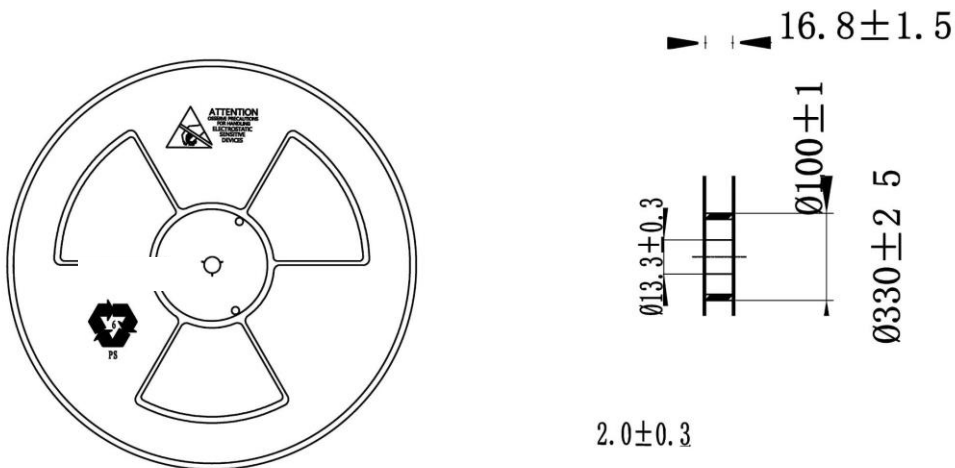
Notes:

- (1) Dimension and tolerance conform to ASME Y14.5-2009.
- (2) All dimension are in millimeters.
- (3) Lead coplanarity shall be 0.1 millimeters max.
- (4) Complies with JEDEC MO-229.
- (5) Drawing is not to scale.
- (6) Dimensions do not include mold protrusion.
- (7) Package outline exclusive of metal burr dimensions.

11. Reel information

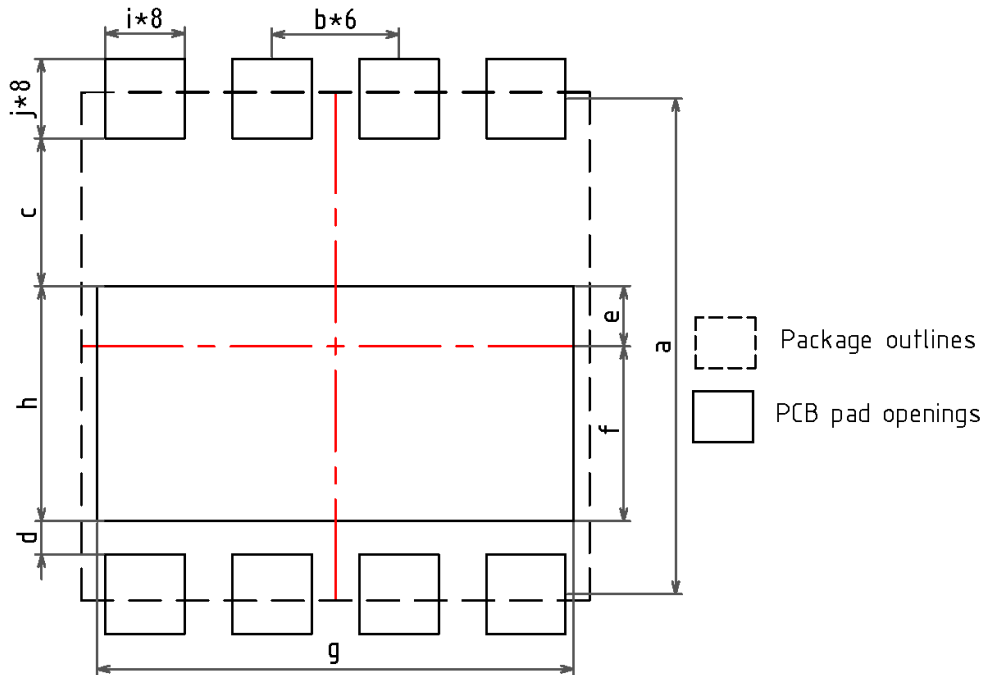


1. The cumulative error of any 10 sprocket holes shall not exceed $\pm 0.2\text{mm}$;
2. The material thickness shall be measured based on the edge of the carrier tape;
3. The unspecified tolerance is $\pm 0.1\text{mm}$, and $R < 0.3\text{mm}$ is not specified
4. The unmarked demolding slope is 5° ;
5. Surface resistivity: $1\text{e}5 \Omega / \Delta \sim 1 \times 10^{11}$



1. The surface of tape should be smooth, clean, and free of injection molding defects, and there should be no significant burrs;
2. Material surface resistivity: $1\text{e}5 \Omega / \Delta \sim 10\text{e}11 \Omega / \Delta$
3. Unspecified tolerance: $\pm 0.3\text{mm}$

12. Recommended PCB footprint



SYMBOL	DIMENSION	SYMBOL	DIMENSION
a	7.800	f	2.750
b	2.000	g	7.500
c	2.325	h	3.700
d	0.525	i	1.400
e	0.950	j	1.250

Notes:
 (1) All dimensions are in millimeters.
 (2) Drawing is not to scale.

Important Notice

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