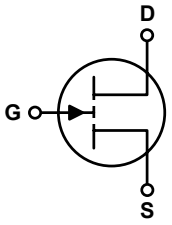
# INN040FQ043A

## 1. General Description

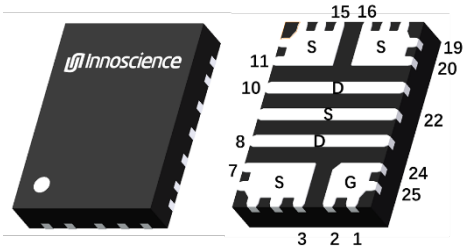
**GaN-on-Silicon enhancement mode high-electron-mobility-transistor (HEMT) in FCQFN with 3 mm x 4 mm package size.**

## 2. Features




- GaN-on-Silicon E-mode HEMT technology
- Very low gate charge
- Ultra-low on resistance
- Very small footprint

## 3. Applications




- High frequency DC-DC converter
- Point of Load
- RF envelope tracking
- PC charger
- Mobile power bank
- Motor driver

## 4. Key Performance Parameters

**Table 1 Key performance parameters at $T_J$ = 25 °C**

| Parameter | Value | Unit |
|---|---|---|
| $V_{DS,max}$ | 40 | V |
| $R_{DS(on),max}$ @ $V_{GS}$ = 5 V | 4.3 | mΩ |
| $Q_{G,typ}$ @ $V_{DS}$ = 20V | 6.2 | nC |
| $I_{DS,Pulse}$ | 160 | A |
| $Q_{OSS}$@ $V_{DS}$ = 20V | 14 | nC |

## 5. Pin Information

**Table 2 Pin information**

| Pin | Pin description | Pin function |
|---|---|---|
| 1, 2, 24, 25 | Gate | Driver Gate |
| 3-7, 9, 11-20, 22 | Source | Source |
| 8, 10, 21, 23 | Drain | Power Drain |

**Table 3 Ordering information**

| Type/Ordering Code | Package | Product Code |
|---|---|---|
| INN040FQ043A | FCQFN 3x4 | D17 |

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## 6. Maximum Ratings

at $T_J$ = 25 °C unless otherwise specified.

Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact Innoscience sales office.

**Table 4 Maximum ratings**

| SYMBOL | PARAMETER | MAX | UNIT |
|---|---|---|---|
| $V_{DS}$ | Drain-to-Source Voltage (Continuous) | 40 | V |
| $I_D$ | Continuous current | 24 | A |
| | Pulsed (25˚C, $T_{Pulse}$ = 300 μs) | 160 | A |
| $V_{GS}$ | Gate-to-Source Voltage | 6 | V |
| | Gate-to-Source Voltage | -4 | V |
| $P_{tot}$ | Power dissipation ($T_{c,\ bottom}$ = 25°C) | 43 | W |
| $T_J$ | Operating Temperature | -40 to 150 | ˚C |
| $T_{STG}$ | Storage Temperature | -40 to 150 | ˚C |

# 7. Thermal Characteristics

**Table 5 Thermal characteristics**

| SYMBOL | PARAMETER | TYP | UNIT | Note/Test Condition |
|---|---|---|---|---|
| $R_{\theta JC\_top}$ | Thermal Resistance, Junction to Case (top) | 26.2 | ˚C/W | |
| $R_{\theta JC\_bot}$ | Thermal Resistance, Junction to Case (bottom) | 2.9 | ˚C/W | |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient [1] | 45.9 | ˚C/W | |
| $T_{sold}$ | Maximum reflow soldering temperature | 260 | °C | MSL3 |

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

## 8. Electric Characteristics

at $T_J$ = 25 °C, unless specified otherwise

**Table 6 Static characteristics**

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-to-Source Voltage | 40 | | | V | $V_{GS}$ = 0 V, $I_D$ = 500 µA |
| $I_{DSS}$ | Drain Source Leakage | | | 100 | µA | $V_{GS}$ = 0 V, $V_{DS}$ = 32 V |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | | 3 | 80 | µA | $V_{GS}$ = 5 V |
| | Gate-to-Source Forward Leakage | | 50 | 500 | µA | $V_{GS}$ = 5 V, $T_j$ = 125 °C |
| | Gate-to-Source Reverse Leakage | | 1 | 20 | µA | $V_{GS}$ = -4 V |
| $V_{GS(TH)}$ | Gate Threshold Voltage | 0.7 | | 2.4 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 7 mA |
| $R_{DS(on)}$ | Drain-Source On-state Resistance | | 3 | 4.3 | mΩ | $V_{GS}$ = 5 V, $I_D$ = 15 A |
| $V_{SD}$ | Source-Drain Forward Voltage | | 1.9 | | V | $I_S$ = 0.5 A, $V_{GS}$ = 0 V |

**Table 7 Dynamic characteristics**

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input Capacitance | | 805 | | pF | $V_{GS}$ = 0 V, $V_{DS}$ = 20 V |
| $C_{oss}$ | Output Capacitance | | 428 | | | |
| $C_{rss}$ | Reverse Transfer Capacitance | | 13 | | | |
| $C_{oss(er)}$ | Energy Related Coss | | 600 | | | $V_{GS}$ = 5 V, $V_{DS}$ = 20 V, $I_D$=15 A |
| $C_{oss(tr)}$ | Time Related Coss | | 703 | | | |
| $R_G$ | Gate resistance | | 1.7 | | Ω | f = 1 MHz |
| $Q_G$ | Total Gate Charge | | 6.2 | 8.5 | nC | $V_{GS}$ = 5 V, $V_{DS}$ = 20 V, $I_D$=15 A |
| $Q_{GS}$ | Gate to Source Charge | | 1.4 | | | $V_{DS}$ = 20 V, $I_D$ =15 A |
| $Q_{GD}$ | Gate to Drain Charge | | 0.8 | | | |
| $Q_{G(TH)}$ | Gate Charge at Threshold | | 0.9 | | | |
| $Q_{OSS}$ | Output Charge | | 14 | | | $V_{GS}$ = 0 V, $V_{DS}$ = 0 V to 20 V |

## 9. Electric Characteristics Diagrams

at $T_J$ = 25 °C, unless specified otherwise

Figure 1 Typical Output Characteristics ($T_J$ = 25 °C)

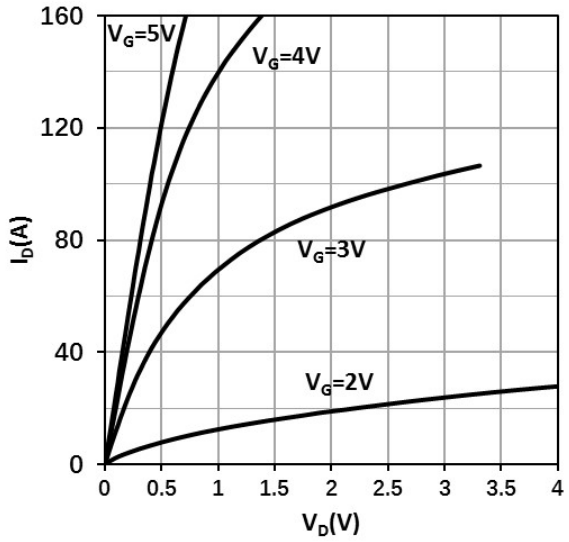



Figure 2 Typical Output Characteristics ($T_J$ = 125 °C)

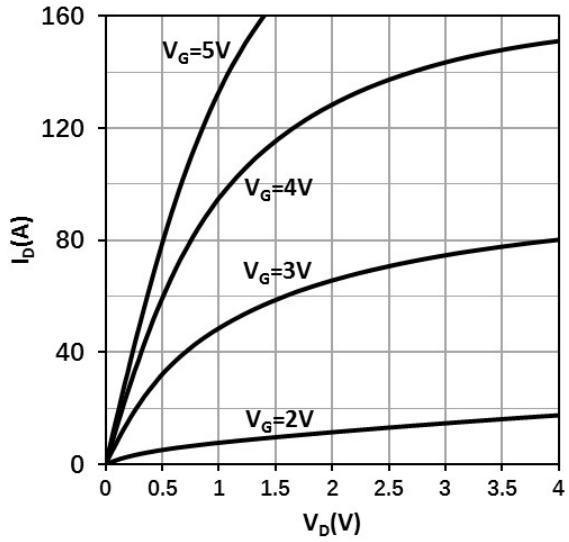



Figure 3 Typ. Drain On-state Resistance($T_J$ = 25 °C)

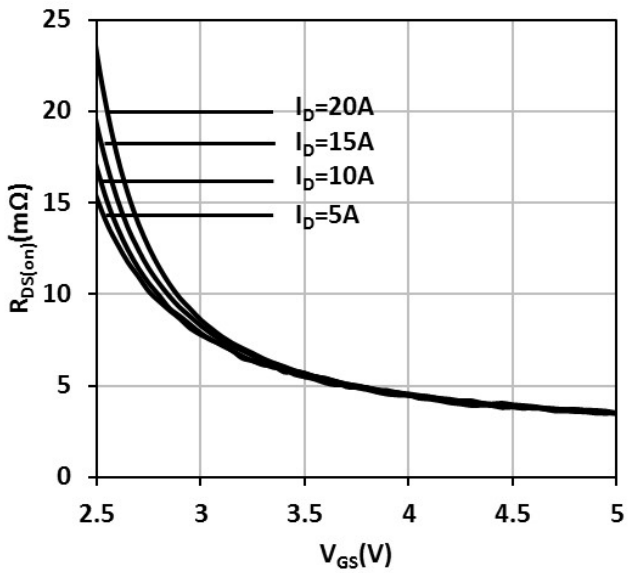



Figure 4 Typ. Drain On-state Resistance ($T_J$ = 125 °C)

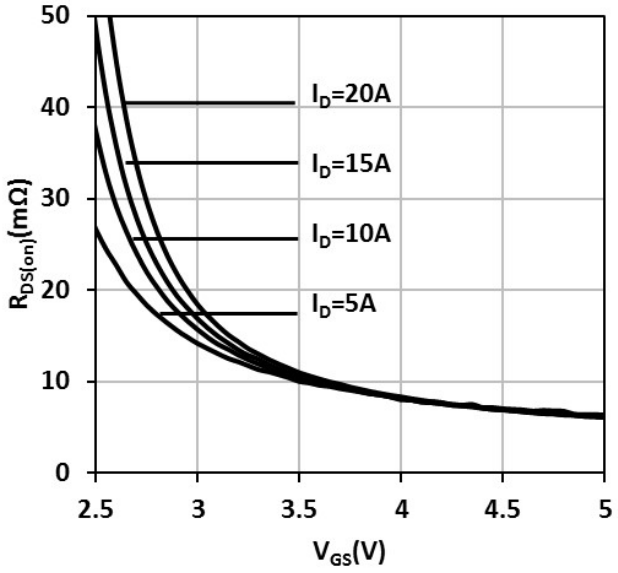


Figure 5 Typical On Resistance vs. Temperature

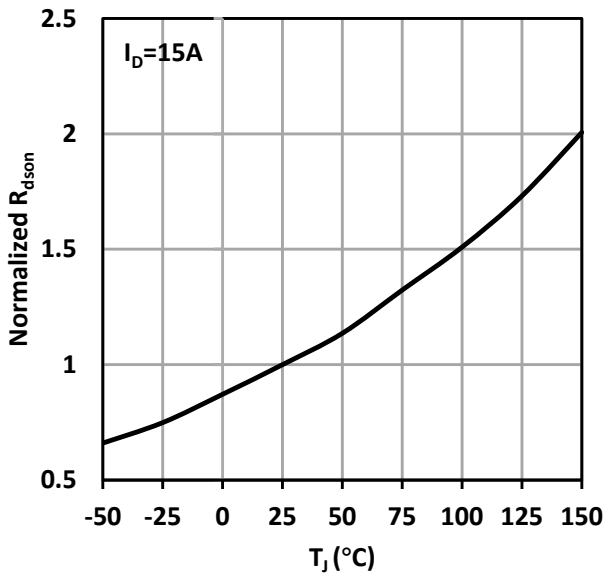



Figure 6 Typical Transfer Characteristics

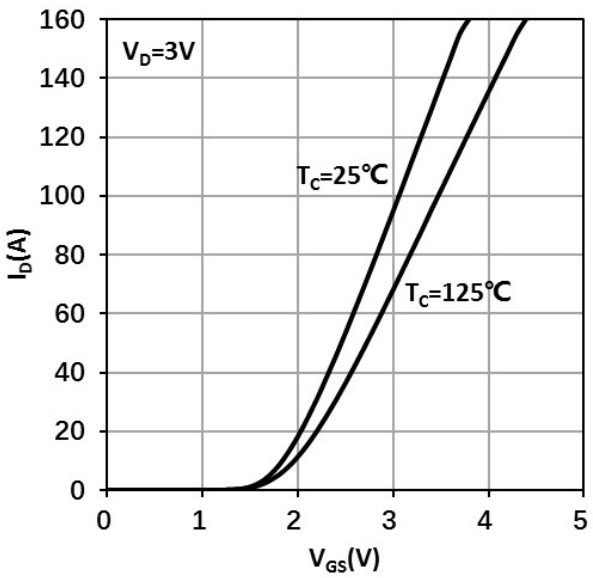



Figure 7 Typ. Reverse Drain-Source Characteristics ($V_{GS}$≤0, $T_J$ = 25 °C)

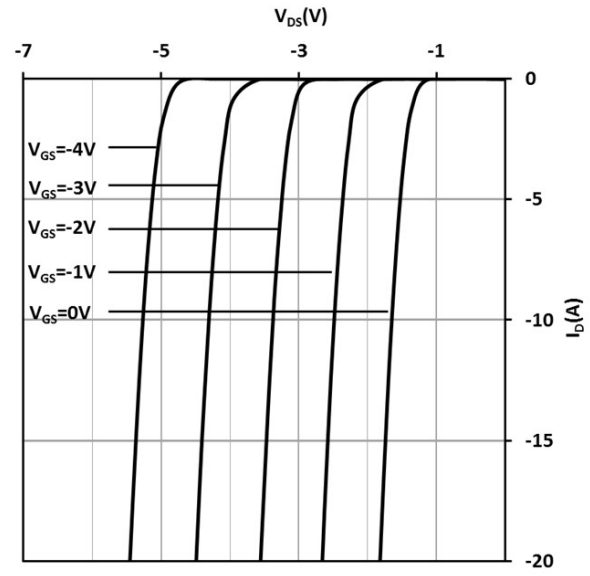



Figure 8 Typ. Reverse Drain-Source Characteristics ($V_{GS}$≥0, $T_J$ = 25 °C)

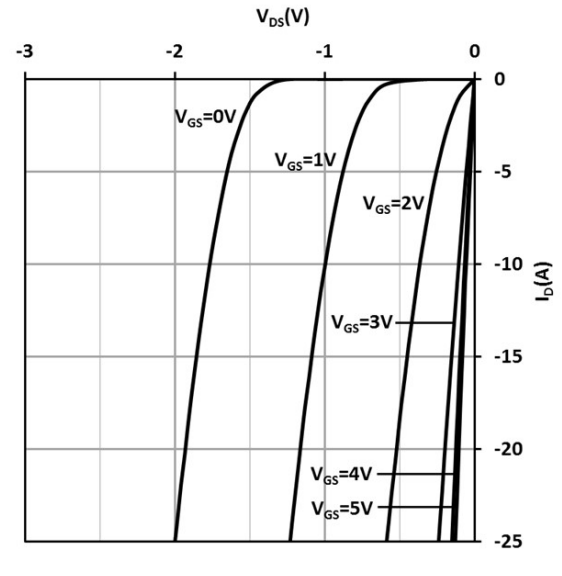


Figure 9 Typ. Reverse Drain-Source Characteristics ($V_{GS}$≤0, $T_J$ = 125 °C)

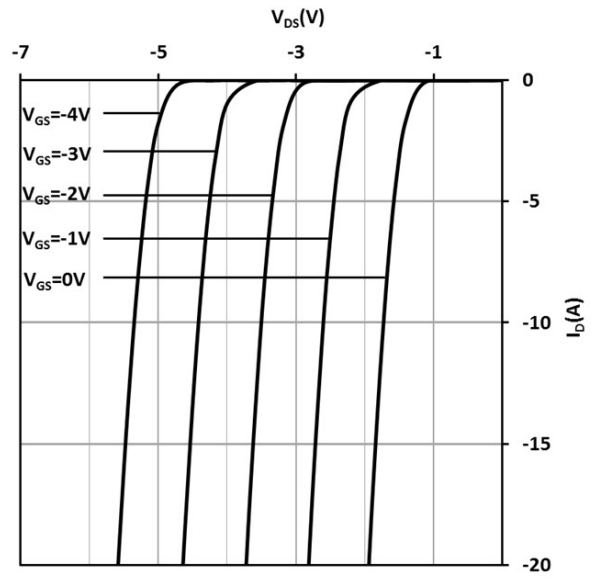



Figure 10 Typ. Reverse Drain-Source Characteristics ($V_{GS}$≥0, $T_J$ = 125 °C)

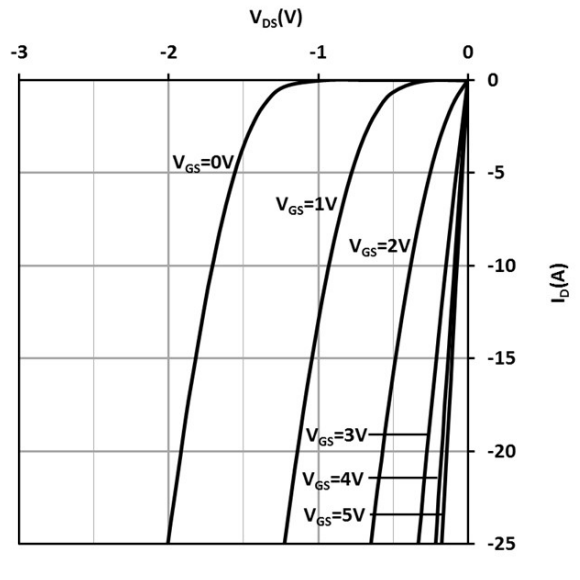



Figure 11 Typ. Capacitances Characteristics

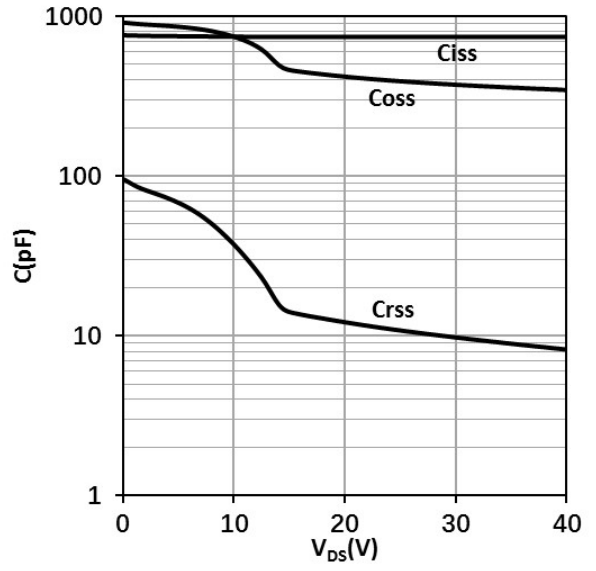



Figure 12 Typ. Gate Charge

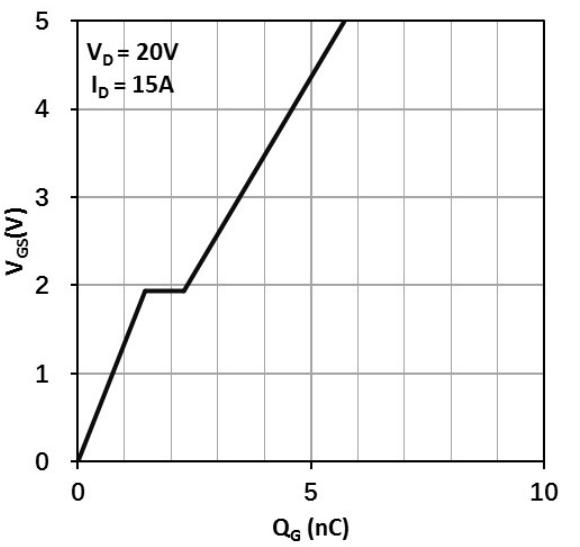


Figure 13 Normalized Threshold Voltage vs. Temp.

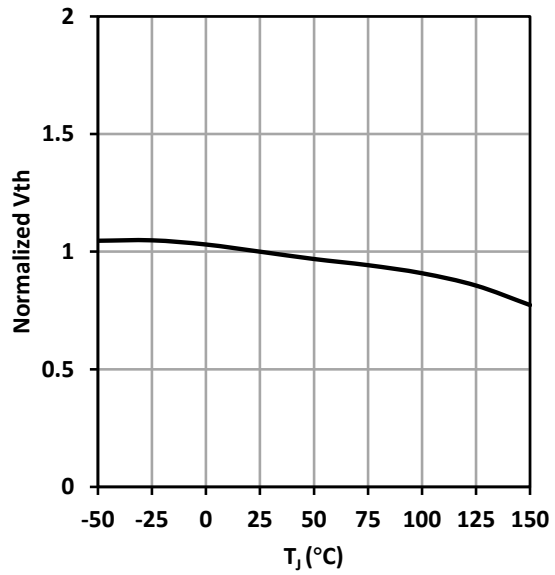



Figure 14 Output Charge

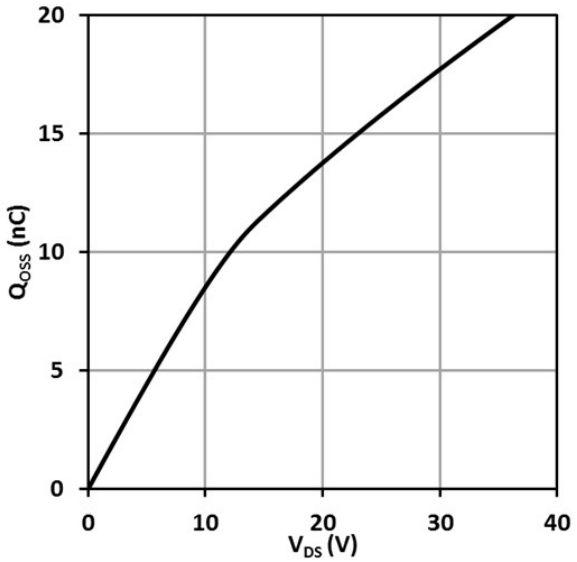



Figure 15 Output Capacitance Stored Energy

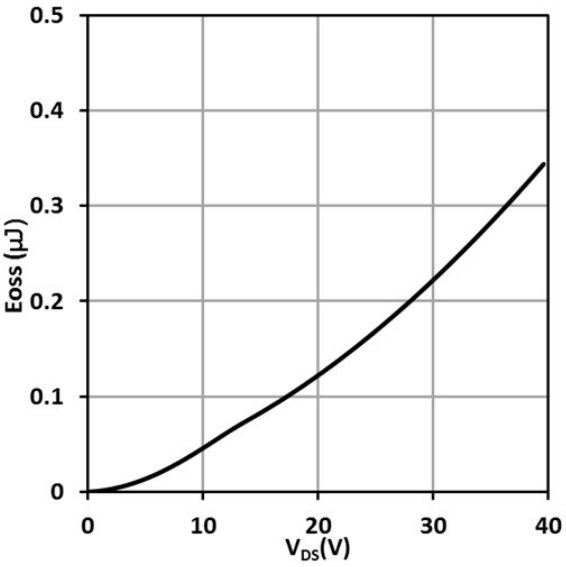



Figure 16 Power Dissipation

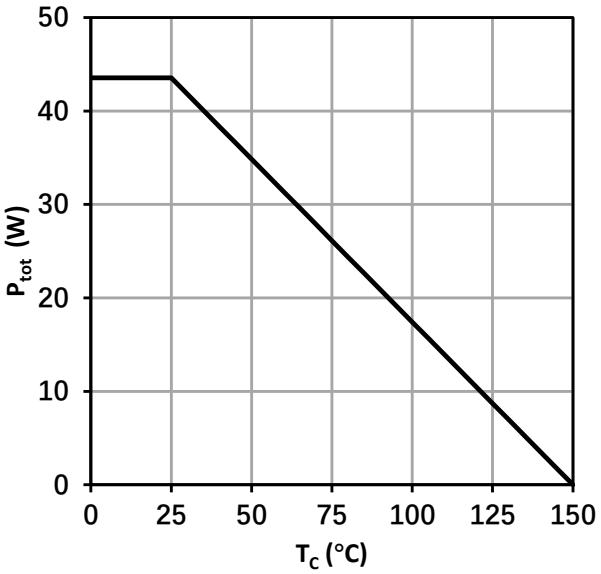


Figure 17 Safe Operating Area

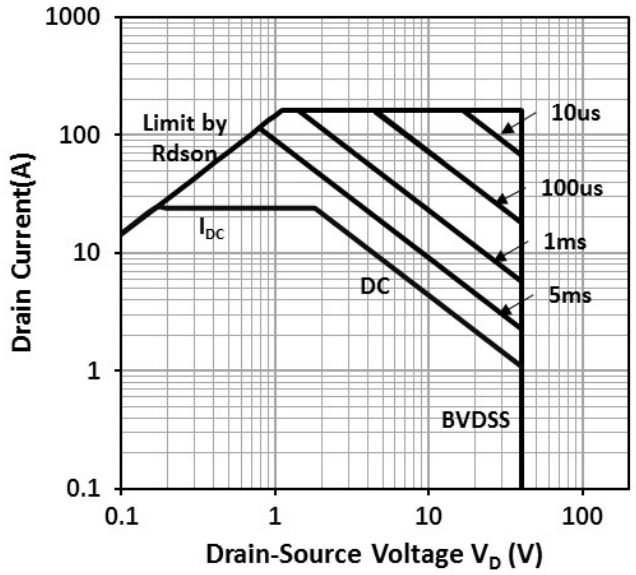
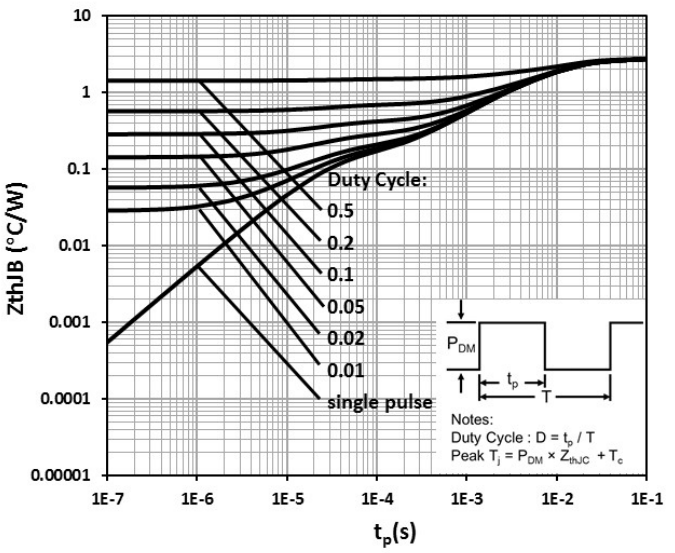
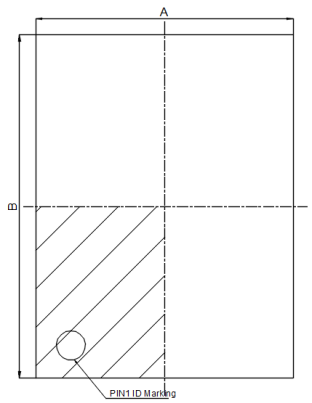



Figure 18 Max. Transient Thermal Impedance

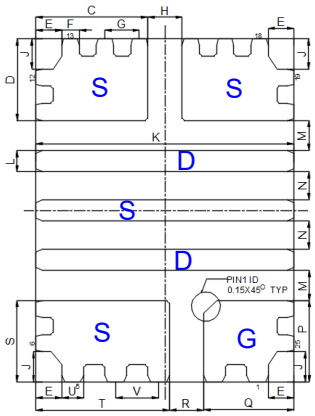


## 10. Package Outlines

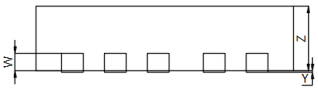
### Package Reference




**TOP VIEW**




**BOTTOM VIEW**

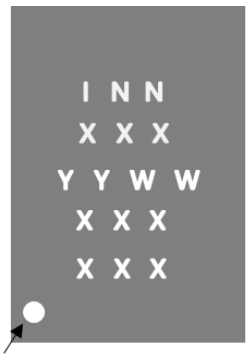



**SIDE VIEW**

NOTE:
1)ALL DIMENSION ARE IN MILLIMETERS.
2)BOTTOM VIEW IS FT TESTER SIDE VIEW.
3)LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4)COMPLIES WITH JEDEC MO-220.
5)DRAWING IS NOT TO SCALE.

| SYMBOL | MILLIMETER | | | NOTE |
|---|---|---|---|---|
| | MIN | NOM | MAX | |
| A | 2.9 | 3.0 | 3.1 | |
| B | 3.9 | 4.0 | 4.1 | |
| C | 1.2 | 1.3 | 1.4 | 2X |
| D | 0.85 | 0.95 | 1.05 | 2X |
| E | | 0.3 REF | | 4X |
| F | 0.15 | 0.2 | 0.25 | 14X |
| G | | 0.4 BASIC | | 8X |
| H | 0.35 | 0.4 | 0.45 | |
| J | | 0.35 REF | | 4X |
| K | 2.9 | 3.0 | 3.1 | 3X |
| L | 0.20 | 0.25 | 0.30 | 3X |
| M | 0.3 | 0.35 | 0.4 | 4X |
| N | 0.275 | 0.325 | 0.375 | 2X |
| P | 0.85 | 0.95 | 1.05 | |
| Q | 0.95 | 1.05 | 1.15 | |
| R | 0.35 | 0.4 | 0.45 | |
| S | 0.85 | 0.95 | 1.05 | |
| T | 1.45 | 1.55 | 1.65 | |
| U | 0.2 | 0.25 | 0.3 | 5X |
| V | | 0.5 BASIC | | 3X |
| W | | 0.203 REF | | |
| Y | 0 | 0.02 | 0.05 | |
| Z | 0.65 | 0.75 | 0.85 | |

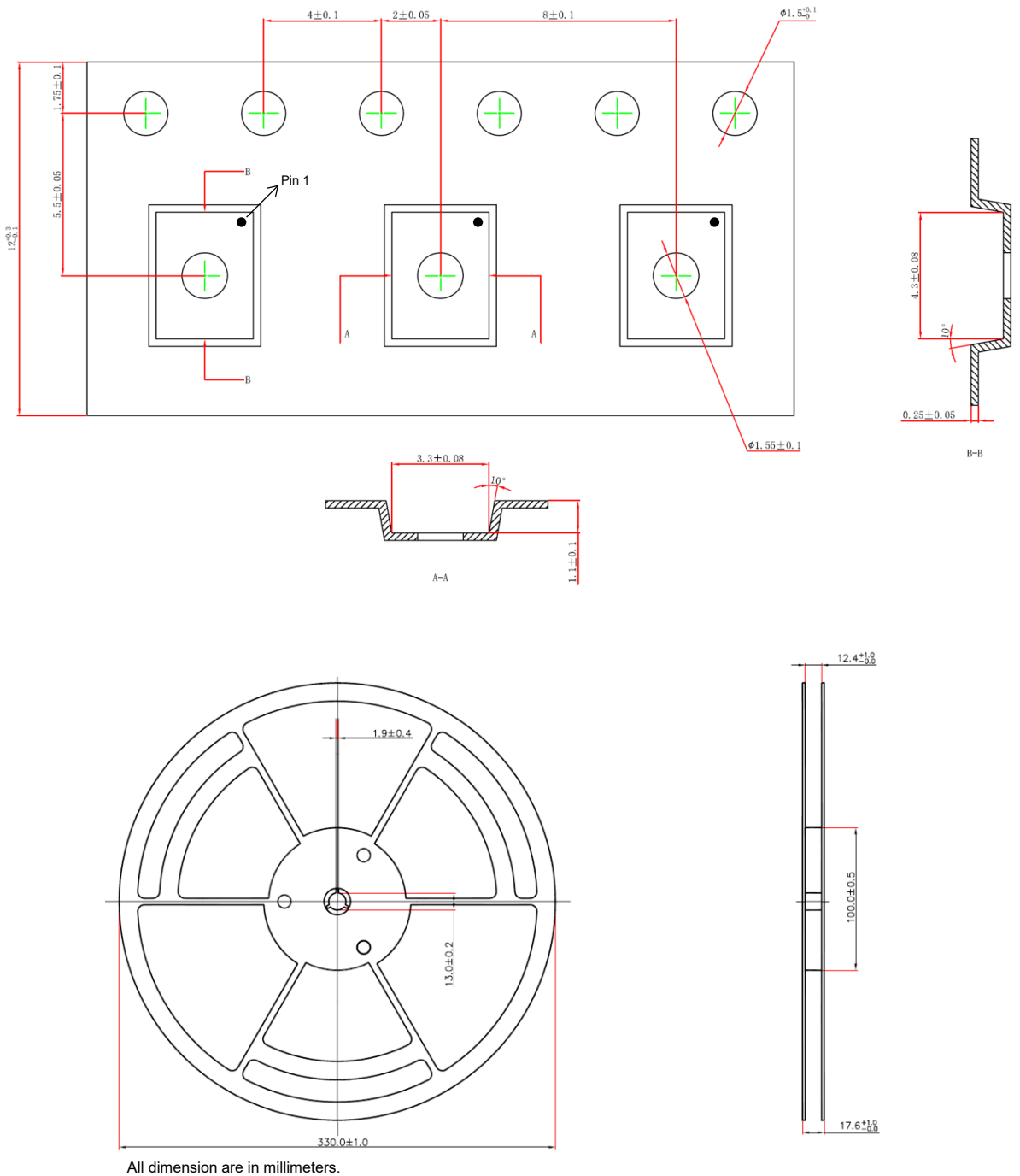
### Marking Reference:




Die Orientation Dot
&Gate Position

| Row | Description | Example |
|---|---|---|
| Row 1 | Company name | INN |
| Row 2 | Product code | XXX |
| Row 3 | Date code | YYWW |
| Row 4 | Lot No | XXX |
| Row 5 | Lot No | XXX |

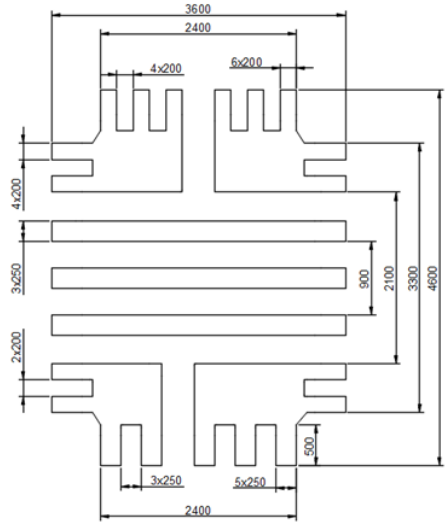
## 11. Reel Information




All dimension are in millimeters.

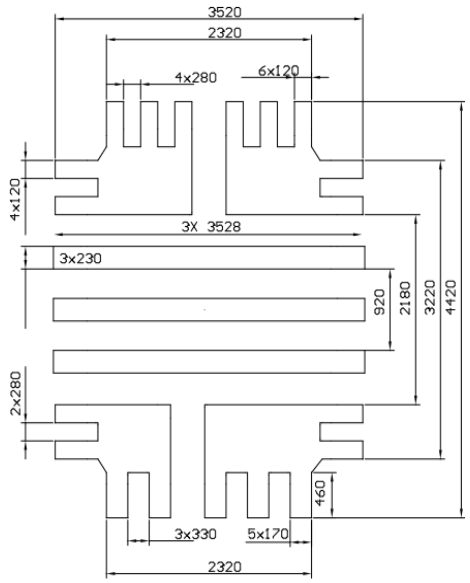
## 12. Land Pattern

### Recommended Land Pattern




TOP VIEW Unit: µm

### Recommended Stencil Drawing




TOP VIEW Unit: µm

## 13. Revision History

**Major changes since the last revision**

| Revision | Date | Description of changes |
|---|---|---|
| 1.0 | 2022-12-12 | 1.0 version release |
| 1.1 | 2022-12-22 | Update package marking information |
| 1.2 | 2023-07-21 | Tighten $I_{DSS}$ spec to 100uA from 200uA |
| 1.3 | 2023-10-07 | 1. Corrected typos<br>2. Update package rendering on page1<br>3. Add $Q_G$ max spec in Electric Characteristics |
| 1.31 | 2023-11-08 | Corrected typos |
| 1.32 | 2024-06-18 | 1. Corrected typos<br>2. Update Pin 1 position in Reel Information on page13 |

## Important Notice

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